SPECTRA 70

RADIO CORPORATION OF AMERICA • ELECTRONIC DATA PROCESSING

PROCESSOR

7055

MAINTENANCE MANUAL VOLUME I

RADIO CORPORATION OF AMERICA

70-55-101
March 1968

FOREWORD

The information contained in this manual is intended to augment the knowledge and training of the serviceman in order to conserve time and effort in the maintenance and servicing of the 70/55 Processor. To keep the manual current, revisions will be issued as additional information becomes available.

Record of Publication

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SECTION ONE

INTRODUCTION

1.1 GENERAL

The RCA Model 70/55 is a large scale, solid state system which satisfies the most sophisticated data processing, scientific, problem solving or communication system requirements. The internal logic is controlled by hardware generated status levels.

The 70/55 Processor may be any one of the model numbers listed in Table 1-1. The memory size (capacity in bytes) and number of racks required to accommodate these sizes are also given in this table. The method of operation is the same for the different models and is described in the Operation portion of this manual.

The 70/55 is a variable format, word organized processor, consisting of a Main Memory, Non-addressable Memory, Fast Memory, Program Control, and Input/Output Control.

Table 1-1. Spectra 70/55 Model Numbers

Model Number	Capacity (in bytes)	Rack Number Identification	Remarks
70/55E	65,536	40,41,42,45	40 = Power Supply 41 = Basic Processor 42 = Main Memory 43 = 2nd 256K Memory 44 = Power Supply Add On 45 = I/O, Direct Control
70/55F	131,072	40,41,42,45	
70/55G	262,144	40,41,42,45	
70/55H	524 228	40,41,42,43,44,45	

1.2 FUNCTIONAL

1.2.1 PROCESSOR STATES

The RCA 70/55 Processor has four processor states that provide control of the system and program interrupts. Programs may be executed in any one of these states, because each state is completely indpendent and has its own set of registers (except floating point register). The four processor states and their functions are as follows:

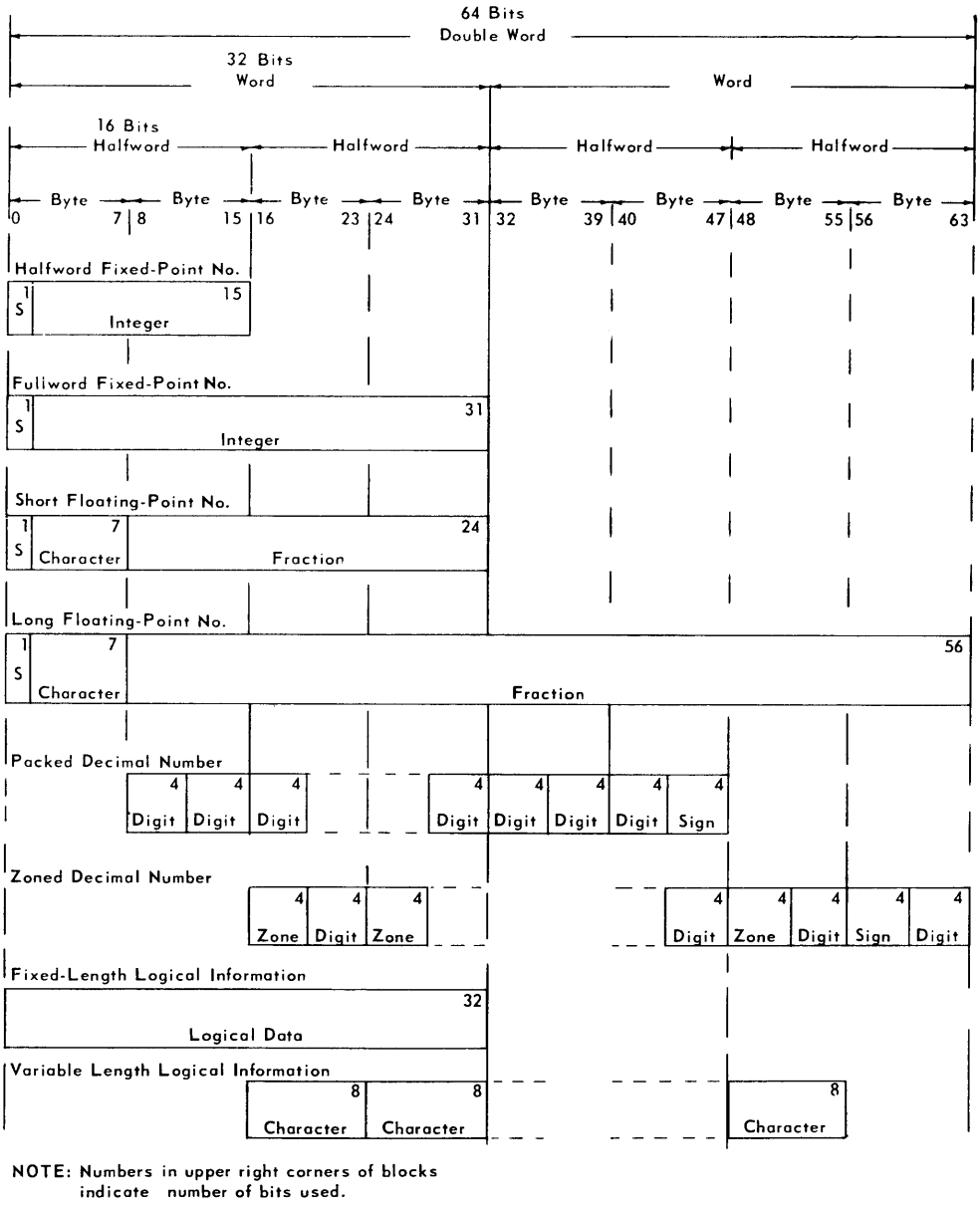
1. Processor State P_1 - normally interprets and executes the user's program. This processing state is the problem-oriented state.

2. Processor State P_2 - performs specific program tasks as dictated by the Interrupt Control State P_3.

3. Processor State P_3 - is automatically entered when an interrupt is recognized other than one caused by a machine check or power failure.

4. Processor State P_4 - is entered whenever a machine check or power failure occurs.

Upon detection of interrupt the hardware initiates Processor State 3 or 4. It is the programs responsibility to determine what action is to be taken in any processor state.



NOTE: Numbers in upper right corners of blocks indicate number of bits used.

Figure 1-1. Data Formats

1.2.2 ORGANIZATION OF DATA

The following definitions describe the various levels of data organization for the 70/55 Processor:

Bit - A bit is a single binary digit having the value of either zero or one.

Byte - A byte consists of eight information bits. Over an I/O interface a byte can also be accompanied by a parity bit.

Halfword - A halfword consists of two consecutive bytes beginning on a main memory location that is multiple of two.

Word - A word consists of four consecutive bytes beginning on a main memory location that is a multiple of four.

Doubleword - A doubleword consists of eight consecutive bytes beginning on a main memory location that is multiple of eight.

1.2.3 DATA FORMATS

The basic unit of information in the 70/55 Processor is a byte, which is the smallest addressable unit.

The internal code representation in the 70/55 is either the Extended Binary-Coded-Decimal Interchange Code (EBCDIC) or the USA Standard Code for Information Interchange (USASCII) as specified by program.

There are eight distinct formats for data in main memory as shown in Figure 1-1.

1.2.4 NUMBERING SYSTEMS

The hexadecimal numbering system is used to represent characters and addresses in the 70/55 Processor. The hexadecimal system has a base of 16. The first ten marks are represented by decimal numbers zero (0) through nine (9); marks eleven through fifteen are represented by the letters A through F. Table 1-2 illustrates the decimal, binary, and hexadecimal representations of numbers zero through fifteen.

1.2.5 INSTRUCTIONS

There are five basic instruction formats which express, in general terms, the operation to be performed. These instructions are:

1. RR = register ----- register operation.
2. RX = register ----- indexed storage operation.
3. RS = register ----- storage operation.
4. SI = storage ----- immediate operand operation.
5. SS = storage ----- storage operation.

Table 1-2. Basic Hexadecimal Marking System

Hexadecimal (Base 16)	Binary (Base 2)	Decimal (Base 10)
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
A	1010	10
B	1011	11
C	1100	12
D	1101	13
E	1110	14
F	1111	15

The detailed format of each instruction is shown in Figure 1-2, and the instruction sub-fields are defined as follows:

R_1, R_2, R_3 = 4 bit operand register specification
X_2 = 4 bit index register specification
B_1, B_2 = 4 bit base register specification
D_1, D_2 = 12 bit displacement
I_2 = 8 bit immediate operand
L_1, L_2 = 4 bit operand length specification
L = 8 bit operand length specification

1.2.6 ADDRESSING MAIN MEMORY

The effective storage address is computed from the following binary components:

1. Base (contents of the designated base register, B_1 or B_2)

2. Displacement (D_1, D_2)

3. Index (contents of the designated index register, X_2) for RX instructions

In computing the address, the base and index are treated as unsigned 24-bit positive binary integers in bits 8-31 of the designated register. The displacement is treated as a 12-bit positive binary integer. The effective address is computed by adding the components as binary numbers, ignoring overflow.

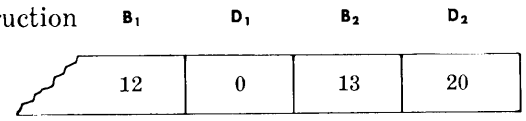
> NOTE: If register 0 is specified as the base register and/or the index register, then a zero quantity is to be added, regardless of the contents of register 0.

The following examples use decimal addresses for convenience:

EXAMPLE 1

Assume Reg. 12 2000
Reg. 13 0480

Instruction



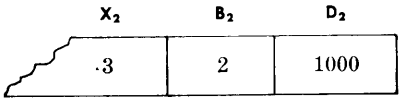
The effective address of B_1, D_1 is 2000

The effective address of B_2, D_2 is 0500

EXAMPLE 2

Assume Reg. 3 30010
Reg. 2 00200

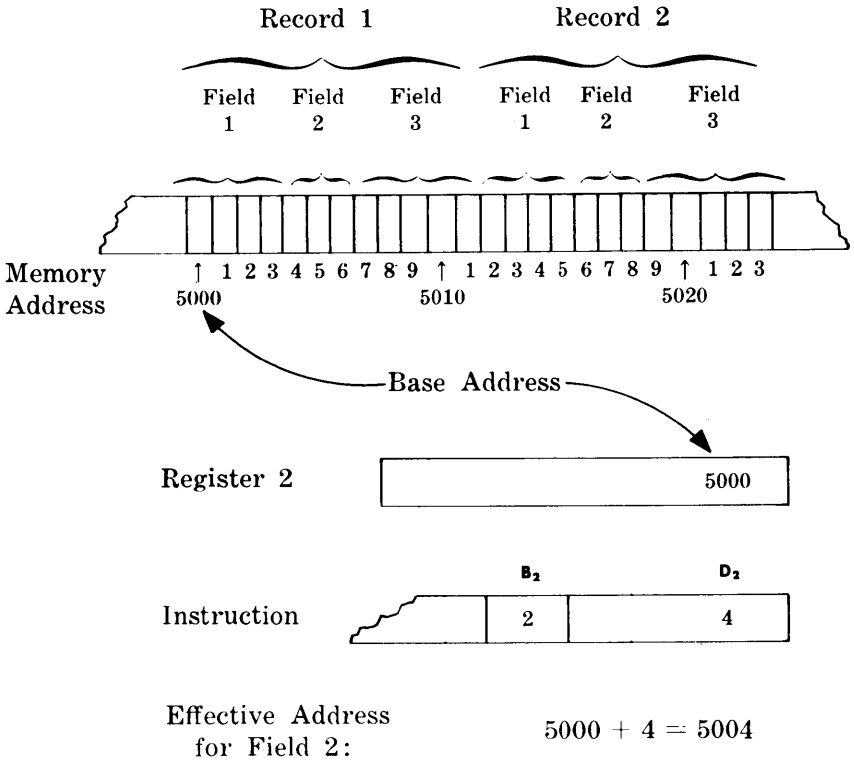
Instruction



The effective address of X_2, B_2 and D_2 is

$$30010 + 00200 + 1000 = 31210$$

EXAMPLE 3



Effective Address for Field 2: $5000 + 4 = 5004$

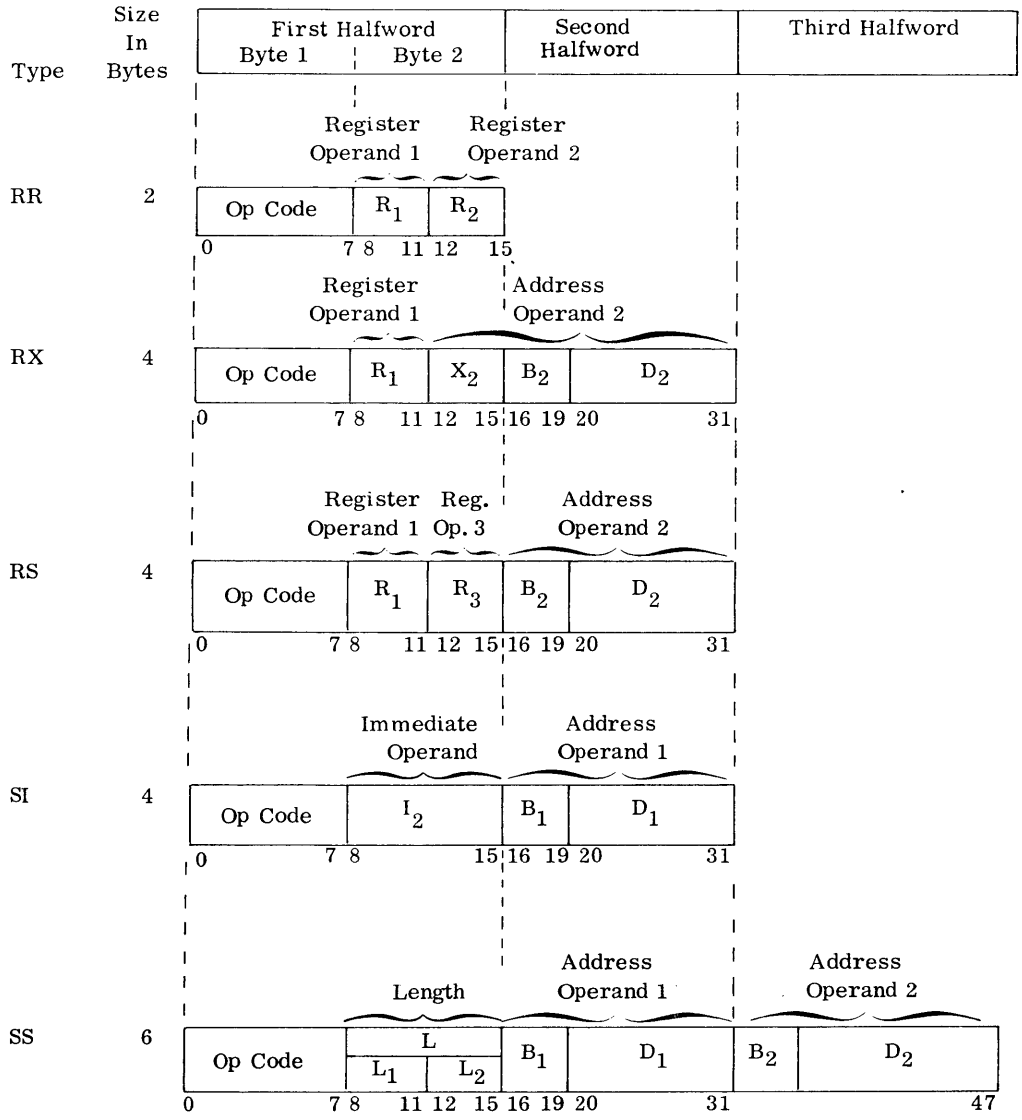
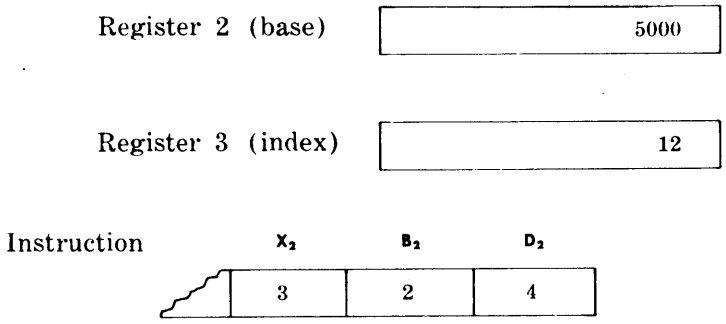


Figure 1-2. 70/55 Instruction Formats

To process Record 2, the contents of Register 2 are increased by 12, the size of Record 1. The instruction field in (example 3) would then refer to Field 2 of Record 2.

If the instruction is an index-type instruction, a second general-purpose register, called an index register, is also used to generate the address. In example 3, the index register (Register 3) would initially be cleared to zero. After the first record is processed, the contents of Register 3 are increased by the record size. Then the instructions using Registers 2 and 3 for addressing would refer to Record 2. An illustration of this follows:



Effective Address for Field 2,

Record 2: 5000 + 12 + 4 = 5016

1.2.7 INPUT/OUTPUT CHANNELS

The Model 70/55 Processor has two types of input/output channels, selector channels and a multiplexor channel.

Up to six selector channels can be attached to a Model 70/55 Processor. All selector channels and trunks are optional.

Each selector channel has up to four standard interface trunks and each standard interface trunk can be connected to the control electronics of an input/output device. A device control electronics controls one device (i.e., Card Reader, Printer), or a number of devices (i.e., Tape Controller: up to 16 Tape Stations).

Only one device can operate on a selector channel at one time. However, all selector channels can operate simultaneously with, and independently of, normal processor operation. The limitations of individual systems must be considered by the programmer.

The multiplexor channel is standard on the Model 70/55 Processors, and can address up to 256 devices.

The multiplexor channel has up to eight standard interface trunks, each of which can be connected to a device control electronics. This permits the multiplexor channel to operate devices on all eight trunks simultaneously. The limit as to the number of input/output devices that can be connected is determined by the device control electronics. A ninth trunk is provided on the multiplexor channel for exclusive use by the Model 70/97 Console.

Figure 1-3 depicts the logical connection of the I/O channels and I/O devices.

> NOTE: A maximum of 24 trunks may be connected in a 70/55 System.

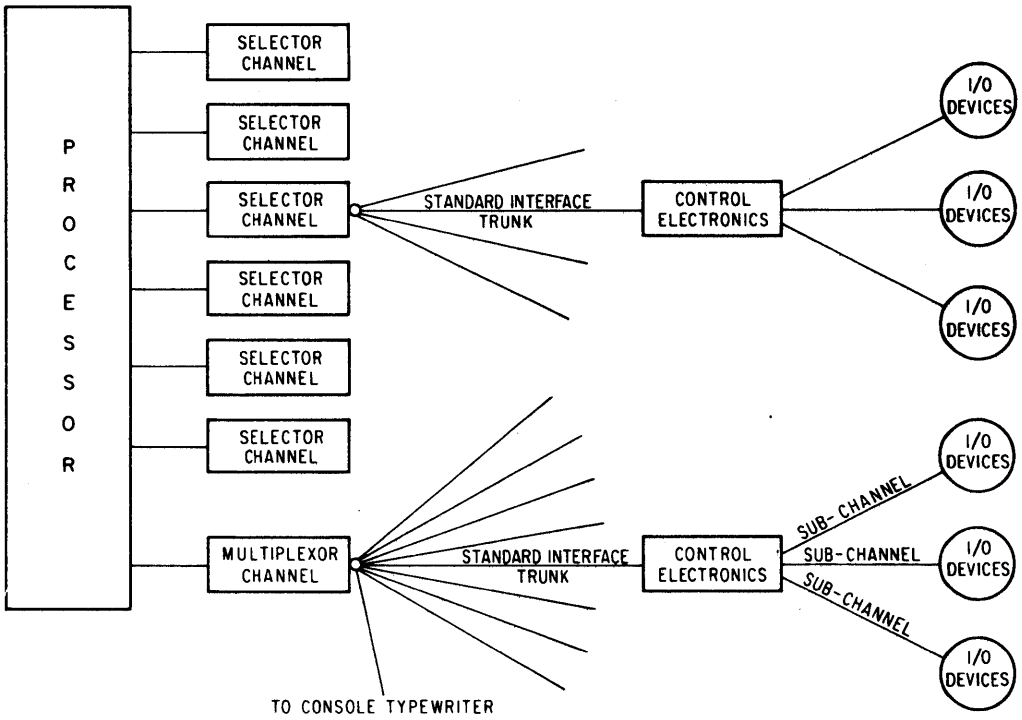


Figure 1-3. 70/55 Input/Output Flow

1.3 SUB-UNITS

1.3.1 BASIC PROCESSING UNIT

The Basic Processing Unit (BPU), in response to an internally stored program, can effect internal data transmission, perform arithmetic operations execute decisions and control instructions, and perform branching operations. In addition, the BPU can operate peripheral devices in either an input or an output mode.

1.3.2 MAIN MEMORY

The Main Memory consists of magnetic core storage and is available in the expandable sizes as indicated in Table 1-1. Memory-cycle time is 0.98 microseconds. This is the time to transfer four bytes from main memory to the memory register and to regenerate the bytes in storage. The processor normally operates on four 8-bit bytes at a time, although the minimum addressable data unit is one byte.

1.3.3 NON-ADDRESSABLE MEMORY

This memory is a portion of the main memory that cannot be addressed by program. A set of registers that services the devices attached to a multi-

plexor channel is contained in the non-addressable main memory. Non-addressable memory is in addition to the main memory capacity of the system.

1.3.4 FAST MEMORY

The Fast Memory is a ferrite core storage device (using two cores per bit), with a capacity of 128 four-byte words. The cycle time is 300 nanoseconds. Each word in a fast memory is uniquely addressed.

The following registers are contained in the fast memory of a 70/55 Processor.

1. Processor Utility Registers - All locations designated as processor utility registers are used by the processor for program control and cannot be used by the program.

2. General Registers - These locations are the general registers for each processor state. These registers are used by the program for base addressing, for indexing, or for storing operands.

3. Interrupt Mask Registers - An Interrupt Mask register for each processor state permits or inhibits 32 interrupt conditions.

	P_1	P_2	P_3	P_4	
Interrupt Mask	40	44	50	14	See Interrupt Flags

NOTE: The numbers indicate Maintenance Panel switch settings for addressing the word. Example; 4 on the Digiswitch and 0 on the gang switch will address the interrupt Mask Register for Processor State 1. See Register Selection and Display Controls, Figure 1-13.

4. Interrupt Status Registers - An Interrupt Status Register for each processor state stores interrupt identification information and operational control information. This register contains indications of the last state interrupted, the protection key, the decimal mode (USASCII or EBCDIC), the privileged mode bit and the supervisor call identification.

5. Program Counter - A Program Counter for each processor state contains the main memory address of the next instruction to be executed, the condition code and the instruction length code of the last instruction in which an interrupt occurred, and the program mask.

6. Floating-Point Registers - Four floating-point registers (each is two words long) are used in floating-point arithmetic.

	P_1	P_2	P_3	P_4	
Interrupt Status Register	41	45	51	15	

DR0		DR1		DR2		DR3	
ISI	0	KEY	A	0	0	CALL	
ISI	0	KEY	0	0	0		
ISI	0	KEY	0	0	0		
0	0	KEY	N	0	0		

	P_1	P_2	P_3	P_4	
P — Register	42	46	52	16	

DR0		DR1		DR2		DR3	
ILC	Sig Err	PROGRAM COUNTER					
ILC	Exp Und						
CC	Dec Ov						
CC	FP Ov						

7. Input/Output Channel Registers - A set of four registers for each selector channel controls input/output operation. A set of four registers for the multiplexor channel controls initiation and termination of input/output operations on the multiplexor channel.

8. Interrupt Flag Register - One Interrupt Flag register is provided. When an interrupt condition occurs, a bit associated with this condition is set in the Interrupt Flag register.

	MUX	SEL1	SEL2	SEL3	SEL4	SEL5	SEL6	I/O Channel Registers
Assembly and Status	25	35	65	75	A5	B5	F5	DR0 DR1 Assy DR2 DR3 (Standard Device Byte): Man. Req. / Dev. End; Int. Pend. / Sec. Ind.; Dev. Busy / Dev. Inop.; Cont. Busy / Stat. Mod.
CCR 1	24	34	64	74	A4	B4	F4	DR0: Command Code; DR1–DR3: Data Address of first byte or location of new CCW if command is a transfer in channel.
CCR 2	23	33	63	73	A3	B3	F3	DR0: CD, CC, SLI, SKIP; DR1: PCI, 0, IL, Prog. Chk., Prot. Chk.; DR1: Ch. Data, Ch. Contr'l, TIP, TI; DR2–DR3: Byte Count; Flags; Channel Status
C A R	22	32	62	72	A2	B2	F2	DR0: Device Number; DR1–DR3: Address of next CCW

Interrupt Flags (43)	DR0				DR1				DR2				DR3			
	Test Mode 7C	Sig. Err. 6C	Add. Err. 5C	Not Spec. 4C	MUX 3C	SEL. #3 2C	EXT. #6 1C	EXT. #2 C
	F.P. Ov. 78	Div. Err. 68	Op. Trap 58	Not Spec. 48	SEL. #6 38	SEL. #2 28	EXT. #5 18	EXT. #1 8
	Dec. Ov. 74	Exp. Ov. 64	Priv. Op. 54	Cons. Int. 44	SEL. #5 34	SEL. #1 24	EXT. #4 14	Mach. Check 4
	Exp. Under 70	Data Err. 60	Sup. Call 50	ETC 40	SEL. #4 30	Not Spec. 20	EXT. #3 10	Power Fail. 0

1.3.5 OPERATOR'S CONSOLE

The Model 70/97 Operator's Console is a free standing, self-contained unit which consists of two portions: the Console Typewriter and the Operator's Console/Display Panel, mounted together on a Console table. (See Figure 1-4.) The console panel provides the controls and indicators to enable system operation in conjunction with operating system programs. The operator has complete control of the system and communicates with the system via a set of control switches and the console typewriter.

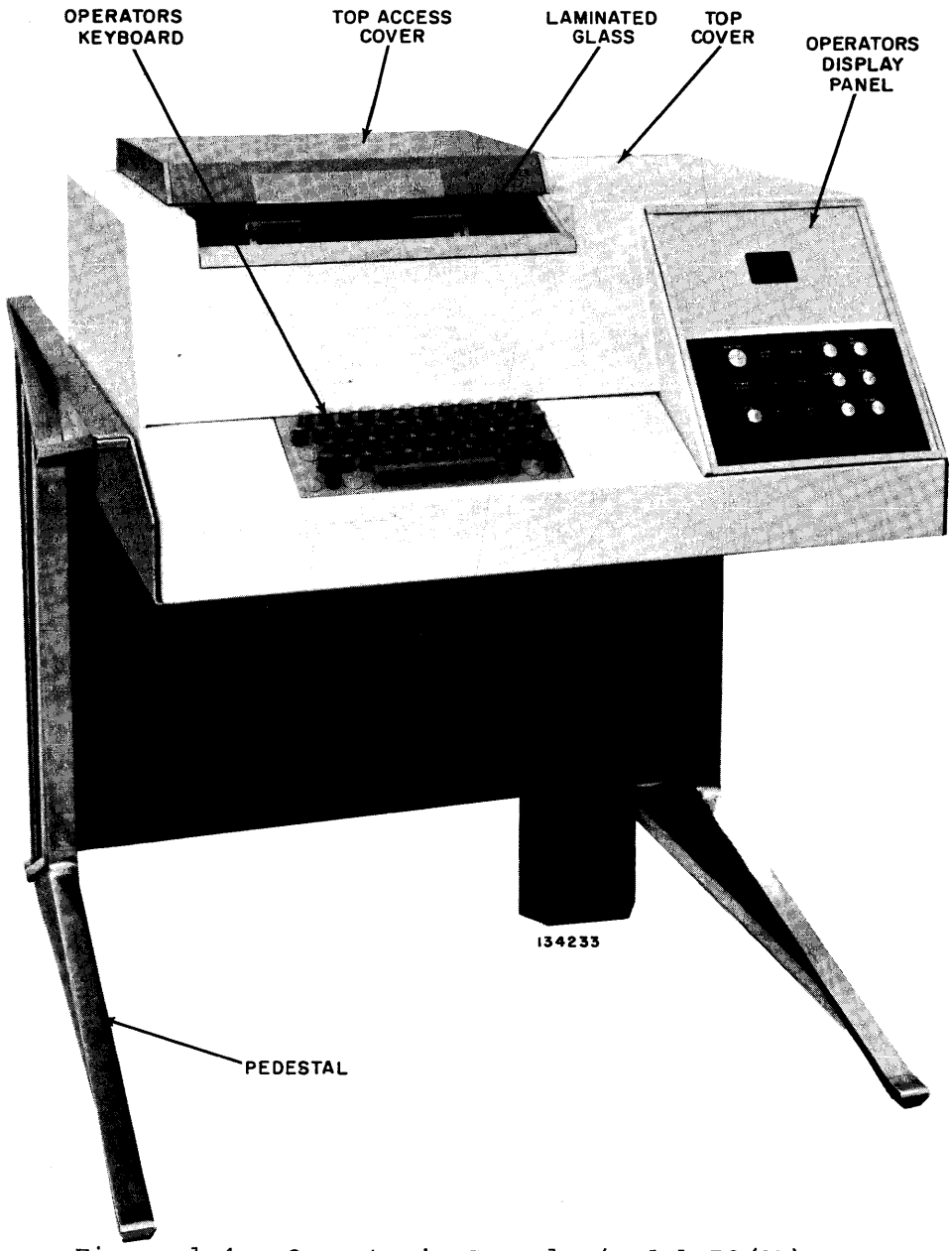


Figure 1-4. Operator's Console (Model 70/97)

1.3.6 MAINTENANCE PANEL

The Maintenance Panel is physically mounted on the power supply rack. It incorporates controls and indicators to enable system operation without the assistance of an operating system program for maintenance purposes. Refer to Table 1-4 for the description of the functions of the indicators and controls on this panel.

1.3.7 POWER SUPPLY

The 70/55 Processor Power Supply furnishes power to the Basic Processing Unit and to the High-Speed Memory in addition to the Operator's Console. Contained in the Power Supply rack are the Typewriter Control and Power Supply electronics. Refer below for description and functions of the Controls and Indicators provided on the Power Supply Control Panel and the AC Input Distribution Panel.

The Supplemental Power Supply (rack 44) is required to supply some of the voltages to the second memory (rack 43). In the Model 70/55 H system the memory storage capacity is 524,228 bytes. This requires two racks more than does the Model 70/55 E, F, and G systems. The memory logic and stacks are housed in the rack 43 and most of its power is supplied by the rack 44.

1.4 CONTROLS AND INDICATORS

The following describes the operational functions of the circuit breakers, pushbuttonsand indicators that comprise operator's controls for the 70/55 Processor.

1.4.1 POWER SUPPLY CONTROLS

The AC Input and the AC Distribution panels are located in the Power Supply cabinet and are shown in Figures 1-5 and 1-6. The circuit breaker switches provide AC power protection as indicated on the front panel.

MAIN - This on-off switch is the main circuit breaker for ac power. When this switch is ON, ac line voltage is available to the Processor Power Supply. (Located behind the hinged AC Input Panel.)

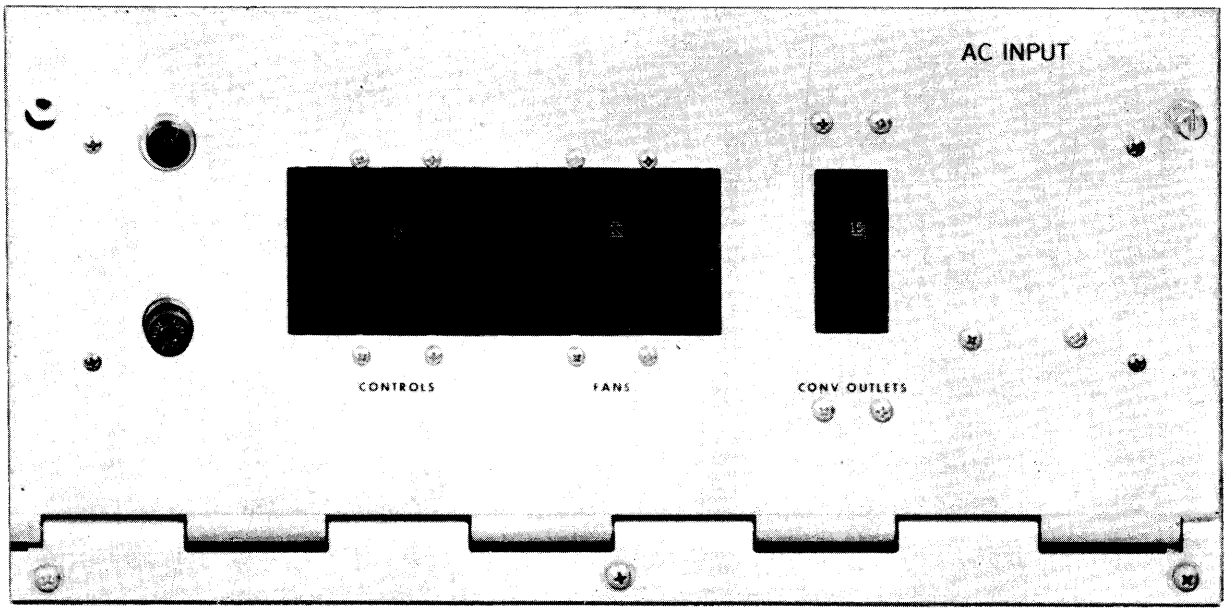
CONVENIENCE OUTLETS - This switch provides ac line voltage to the convenience outlets located in the power supply racks.

FANS - This switch provides ac line voltage to the fans located in the various processor racks.

CONTROLS - This switch provides ac line voltage protection to the transformer which supplies the Control, Regulator and Ramp circuitry.

-5; +30/+20/+10; +50/+5/-30 - These circuit breakers protect the individual power supply voltages as supplied throughout the processor.

The Power Supply Control Panel is located in the Power Supply rack as shown in Figures 1-6 and 1-7. Essentially this panel is utilized for maintenance purposes.



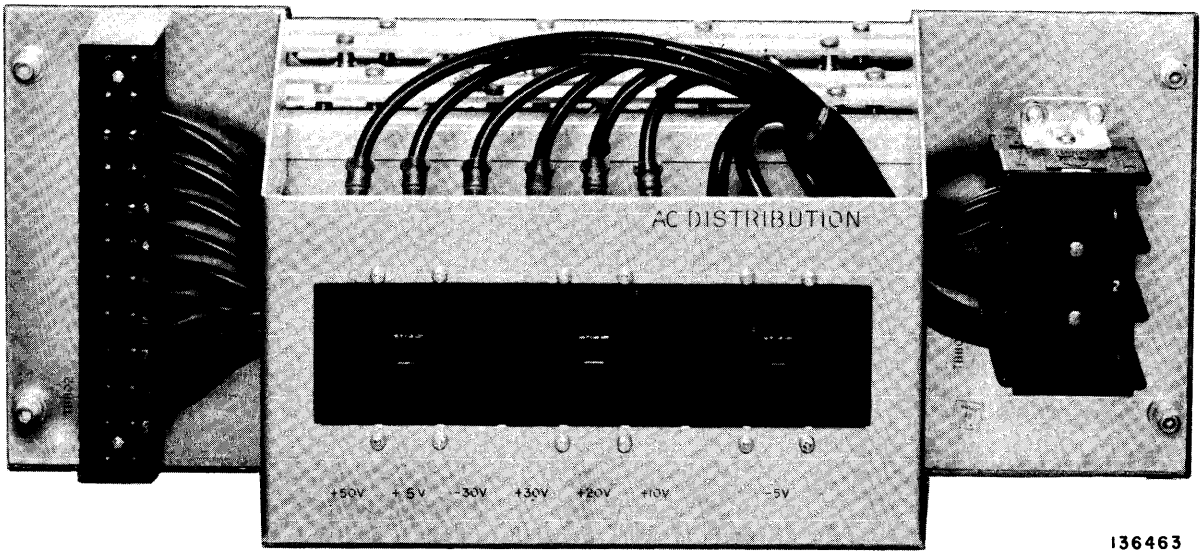


Figure 1-5. Power Supply Panels

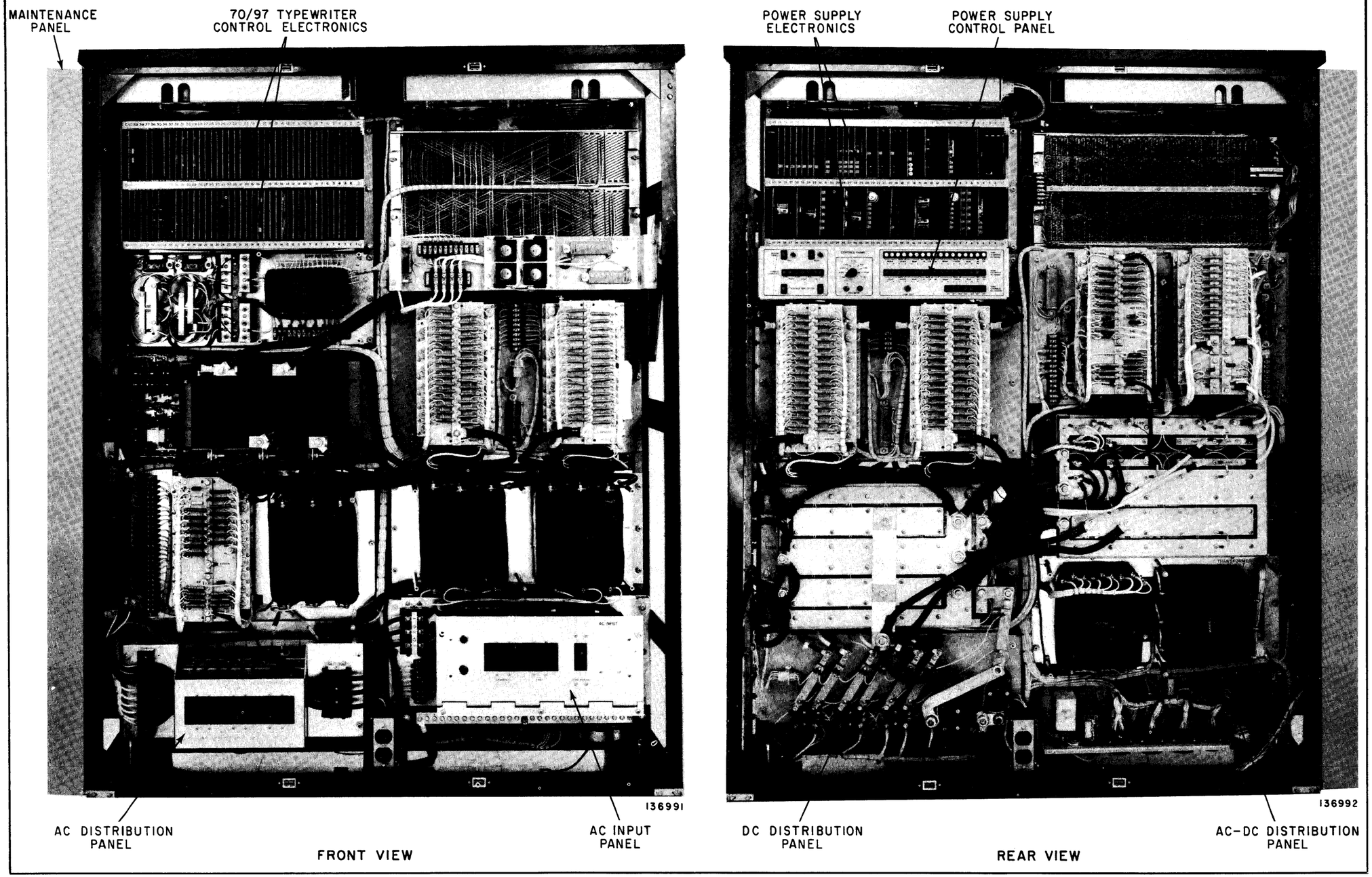


Figure 1-6. 70/55 Power Supply Assembly

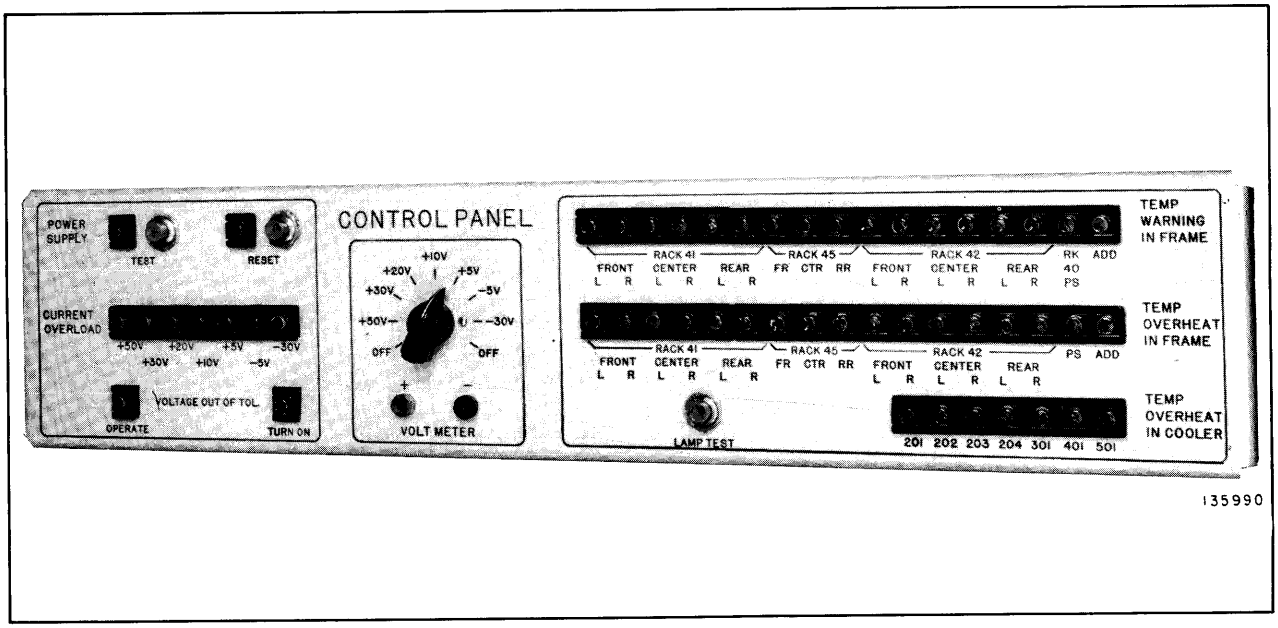


Figure 1-7. Power Supply Control Panel

TEST - This switch is used to turn on the DC power in the test mode. The DC power is isolated from the logic rack(s). Pressing the pushbutton will light its associated indicator.

RESET - Pressing this pushbutton will reset all of the power supply sensing functions. The indicator is lit after a fault is detected and will go off after the POWER SUPPLY is reset.

CURRENT OVERLOAD - These indicators will light whenever a current overload (as noted on the panel) is detected in the power supply input.

VOLTAGE OUT OF TOL - When the OPERATE and/or TURN ON indicators are displayed, the indication is that the protection circuits have detected a voltage out of tolerance.

VOLTMETER - This nine position rotary switch and its associated test jacks, are used for monitoring the output voltage as determined by the positioning of the switch.

TEMP. WARNING IN FRAME - When indicator is lit, the temperature is approaching the maximum safe limits. The location of the sensor is as identified by the markings on the panel.

TEMP. OVERHEAT IN FRAME AND TEMP. OVERHEAT IN COOLER - The indicator associated with the sensor when lit, indicates an overheating condition. The location of the sensor is as identified by the markings on the panel.

LAMP TEST - Pressing this button will cause all Control Panel lamps to light, thus enabling the identification of any defective bulb.

1.4.2 SUPPLEMENTAL POWER SUPPLY CONTROLS

The Supplemental (sometimes referred to as Add-On) Power Supply contains two control panels, as shown on Figures 1-8 and 1-9.

The AC Input and Distribution Panel contains a group of circuit breaker switches which provide AC power protection as indicated on the panel. All of these breakers must be ON in order for either power supply to operate.

The functions of the circuit breakers in the Supplemental Power Supply are exactly as those on the AC Input Panel and AC Distribution Panel described above (1.4.1).

The Supplemental Power Supply Control Panel is used for maintenance and/or trouble indication. Functionally, the controls and indicators are the same as those on the control panel of the Main Power Supply. The Temperature Warning and Temperature Overheat Indicators are marked Rack 43 (added Memory Rack).

Controls of the Main Power Supply and Supplemental Power Supplies are interlocked so that the sensing circuits will cause both power supplies to cycle as one.

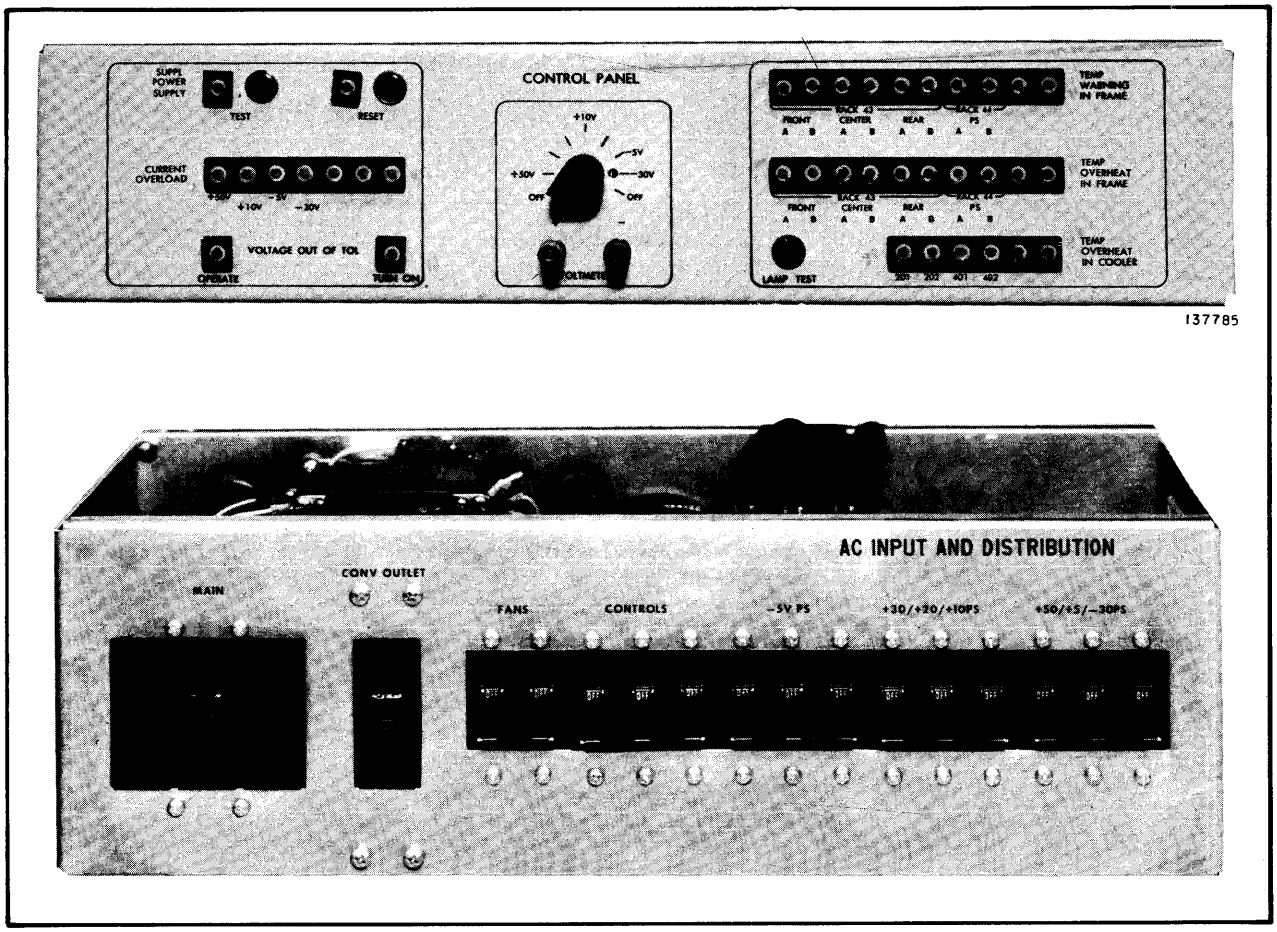
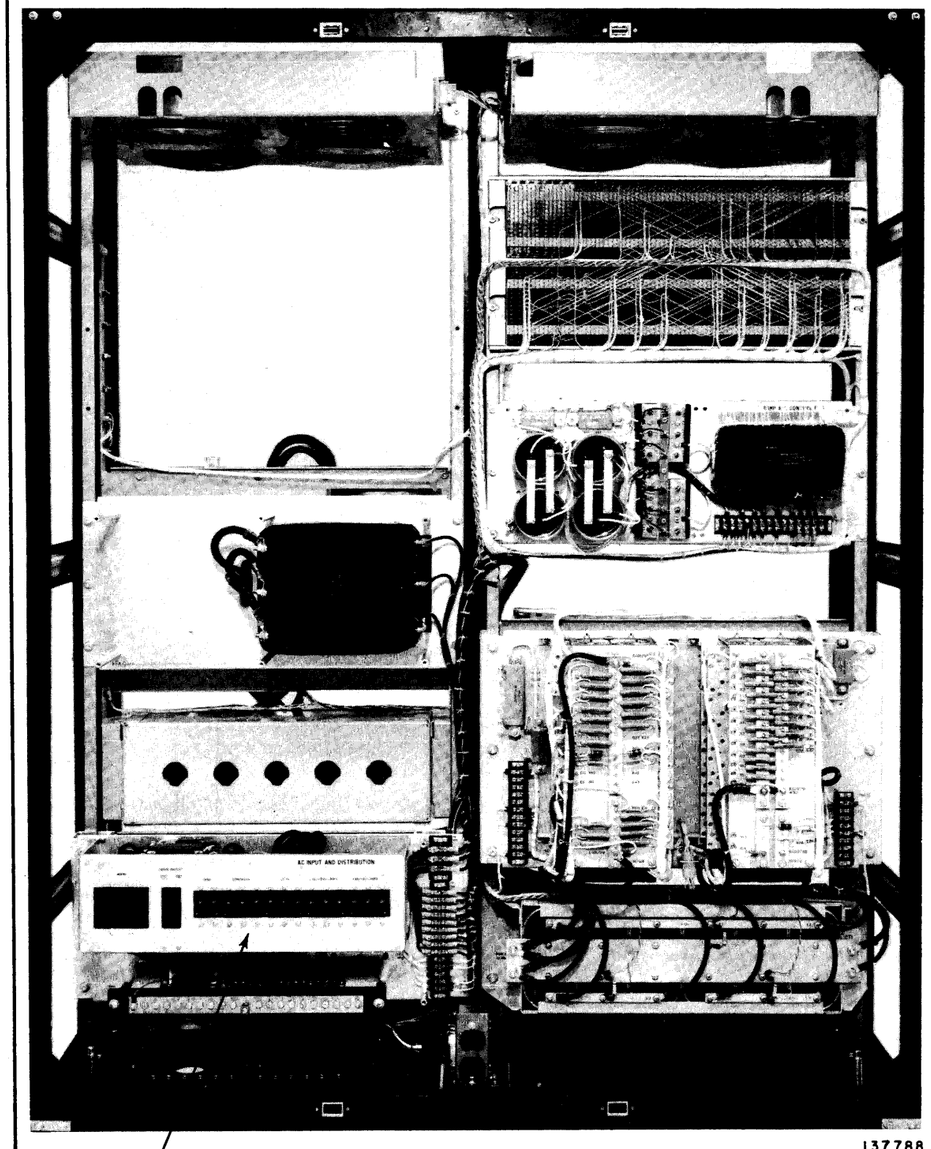


Figure 1-8. Add-On Power Supply Controls and Indicators



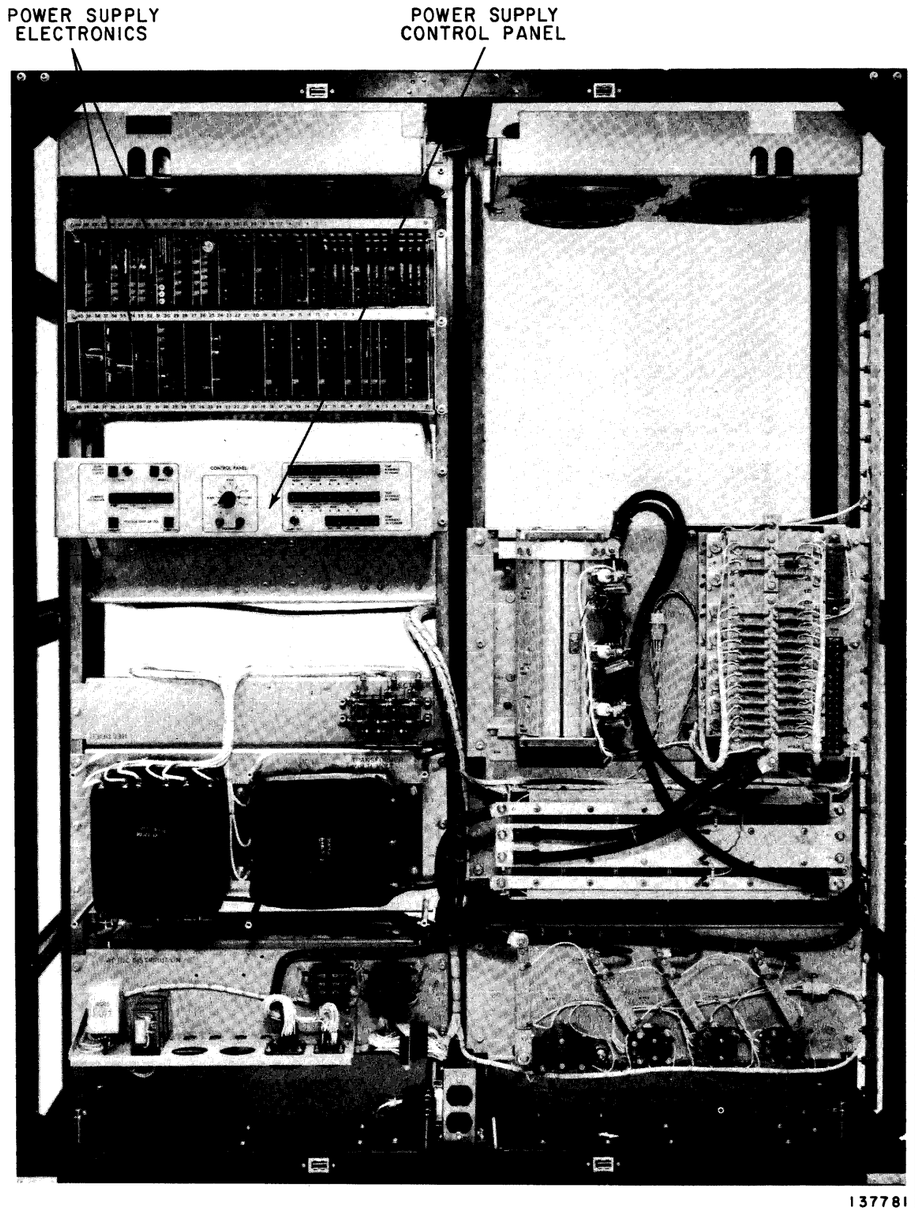


Figure 1-9. Add-On Power Supply Assembly

1.4.3 OPERATOR'S CONSOLE DISPLAY PANEL

By means of the three Digi-Switches and pushbuttons, an operator can perform an initial program load function from any input device; start and stop the computer; or interrupt the program in order to initiate communication with the software via the typewriter. The following listing describes the type and use of the various switches and indicators that comprise the Operator's Display Panel. (See Figure 1-10 and Table 1-3.)

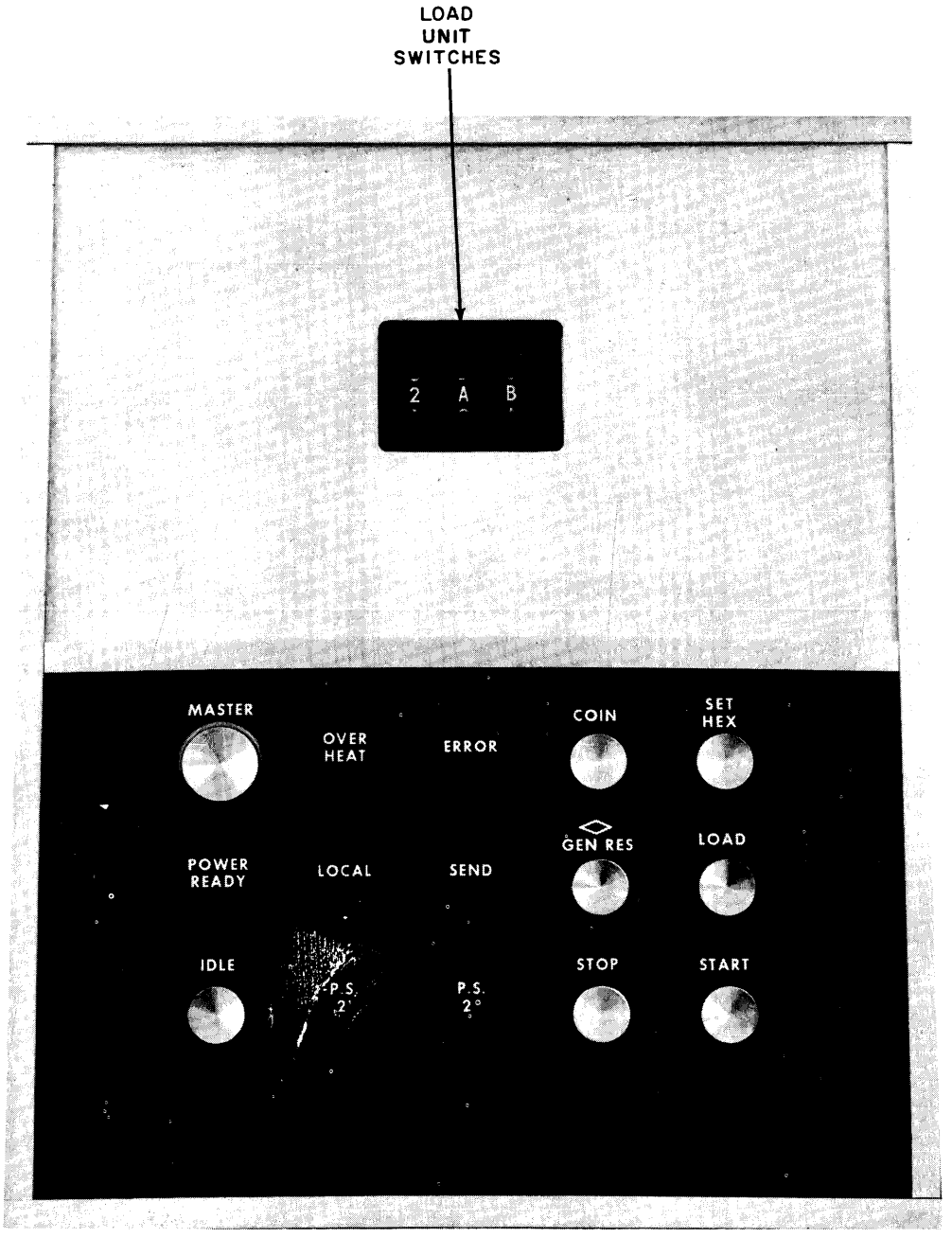


Figure 1-10. Model 70/97 Operator's Console Display Panel

Table 1-3. Operator's Console Panel (Indicators and Controls)

(Reference Fig. 1-10)

Panel Designation	Description and Function
Load Unit Switches (No markings on panel)	The three digi-switches provide for the entry of the I/O channel and device number for initial program load function and are used in conjunction with the LOAD switch. All three switches have sixteen positions labeled 0 through 9 and A through F. Each switch is used as follows: a. Switch 1 This (leftmost) switch provides the three bit channel address of which only positions 0 through 5 and 7 are used. b. Switch 2 This (center) switch provides the 4 high order bits of the device number. c. Switch 3 This (rightmost) switch provides the 4 low order bits of the device number
MASTER	This alternate action switch is used to enable the power supply control circuits and must be in the ON condition before the POWER ON switch at the Maintenance Panel can be activated. This switch can also be used as an emergency power off switch, in which case AC power is disconnected, by-passing the normal DC power off sequencing, and causing the power failure interrupt to be set in the processor. The indicator is turned on upon the pressing of this switch, and remains on, until the switch is pressed again to turn off power. Whenever this switch is in its OFF condition, the POWER ON on the Maintenance Panel is ineffective. This switch does not control AC power to the console typewriter (See Note 1).
POWER READY	This indicator is turned on to indicate that the processor DC power is on and that the processor is ready for operation. This occurs when the processor power sequencing is completed and remains on until power is removed from the processor, either at the completion of power off sequencing, or emergency power off procedures.
IDLE	This indicator is turned on when the Idle instruction is operating. (See Note 2.) The switch portion performs a lamp check of the Operator's Display Panel.
OVER HEAT	This indicator is turned on whenever the temperature in the processor exceeds its environmental design. (See Note 2.)

Table 1-3. Operator's Console Panel (Indicators and Controls)(Cont'd.)

(Reference Fig. 1-10)

<table>
<tr><th>Panel Designation</th><th>Description and Function</th></tr>
<tr><td>LOCAL</td><td>This indicator is turned on whenever the Console typewriter LOCAL-OFF-LINE switch is positioned to LOCAL, or when DC power is off in the processor. The LOCAL-OFF-LINE switch is located inside the Operator's Console Cabinet.</td></tr>
<tr><td>ERROR</td><td>This indicator is turned on when the following errors have been detected in the processor.

MPPE IOPE
MMPE
FMPE PEINT (During load operation)

The particular error which has been detected can be determined from the specific indicators on the Maintenance Panel.</td></tr>
<tr><td>SEND</td><td>When lit, indicates that the Processor is ready to receive input from the Console typewriter. The indicator is turned on whenever a read typewriter operation is initiated. The indicator is turned off when either the EOT key or the Error key on the keyboard is activated.</td></tr>
<tr><td>P.S. 2^1
P.S. 2^0</td><td>Displays the current program state when the processor is halted as follows:

<table><tr><th>P.S. 2^1</th><th>P.S. 2^0</th><th>Program State</th></tr><tr><td>0</td><td>0</td><td>4</td></tr><tr><td>0</td><td>1</td><td>3</td></tr><tr><td>1</td><td>0</td><td>2</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table>
(See Note 3)</td></tr>
<tr><td>COIN</td><td>When this momentary contact switch is pressed and released, the Console Interrupt Flag is set in the Processor, thus notifying the Operating System software of operator intervention via the Console Typewriter.</td></tr>
<tr><td>GEN RES</td><td>Pressing this momentary contact switch will reset the system conditions to a state which permits orderly start-up. (See Note 1.)</td></tr>
<tr><td>STOP</td><td>Pressing this momentary contact switch causes the processor to halt after completion of the current instruction being performed and any I/O operation currently in progress up to 10 seconds.</td></tr>
</table>

Table 1-3. Operator's Console Panel (Indicators and Controls)(Cont'd.)

(Reference Fig. 1-10)

Panel Designation	Description and Function
SET HEX	This alternate action switch when activated will set the Console typewriter electronics to operate in Hexadecimal mode. The operator must then use Hexadecimal coding (two digits per byte). The normal graphic characters cannot be used.
LOAD	When this switch is pressed, program/data from the input device designated by the Load Unit switches are loaded to main memory. The associated indicator and the RUN indicator are lit when the Load Switch is pressed. Upon successful completion of loading the Load indicator is turned off.
START	This momentary contact switch when pressed and then released will start the processor. The indicator is lit when the processor is running. (See Note No. 1.)

Notes: 1. This switch is duplicated on the 70/55 Maintenance Panel.
2. This indicator is duplicated on the 70/55 Maintenance Panel.
3. These indicators are duplicated on the Maintenance Panel.

1.4.3.1 Typewriter Keyboard

The following describes the functions of the keys on the Operator's Keyboard. Figure 1-11 illustrates the Keyboard layout.

RETURN - Pressing down on this keylever will cause the type box and printing carriages to return to the left-hand margin and the paper feed mechanism to advance. One or two lines will advance, depending on the position of the feed mechanism control.

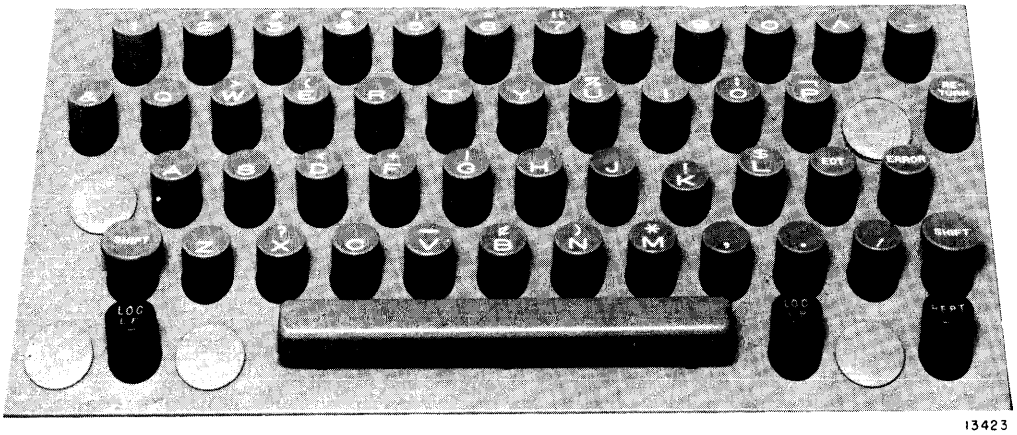


Figure 1-11. Model 70/97 Operator's Console Keyboard Layout

REPT (Repeat) - When this keylever is pressed simultaneously with another keylever or the space bar and held down, it will cause that character or function to repeat as long as the Repeat keylever is held down.

SHIFT - When pressed simultaneously with a character keylever, this keylever will cause the "upper case" character of the character keylever to be printed.

SPACE Bar - Pressing this bar will cause the typewriter to perform a print function on a blank space of the type box. This will cause a blank space on the paper, the size of one character. If the computer is reading from the typewriter a space character is sent to HSM.

ERROR - This keylever is used to terminate a Read Command when a typographic error is detected. Pressing down on this keylever, the SEND lamp will go out and the Read Command will terminate with an indication of a data error.

EOT (End of Transmission) - This keylever is used to terminate a Read Command upon completion of the message. When this keylever is pressed, the SEND lamp will turn off and the Read Command will be terminated.

LOC LF (Local Line Feed) - When this keylever is held pressed, paper will advance through the mechanism without the carriage return function. Paper is fed out continuously, not a line at a time as when pressing the RETURN keylever.

LOC CR (Local Carriage Return) - Pressing this keylever will cause the type box and printing carriages to return to the left-hand margin without feeding paper through the mechanism.

1.4.4 MAINTENANCE PANEL

Table 1-4 lists the various controls and indicators available on the Maintenance Panel. In addition, a brief description of the control and/or indicator is also given. The figure reference number contained in Table 1-4 is indicated on Figure 1-12. (Actually these reference numbers do not appear on the panel, they are supplied herein as an aid for orienting the switch and/or indicator.)

1.4.5 REGISTER SELECTION DISPLAY CONTROLS

Figure 1-13 shows the Register Selection and Display Controls of the 70/55 Processor. Figure 1-14 and the text that follows explains Data Display and Register Selection.

Various Processor Hardware Registers may be displayed on the Data Display Indicators. When the strip switch at the right is pressed (normal operating selection) the data/display indicators display DR (Fast Memory Data Register). To display any of the registers listed in Figure 1-14 press the appropriate register select switch (shown in Figure 1-13).

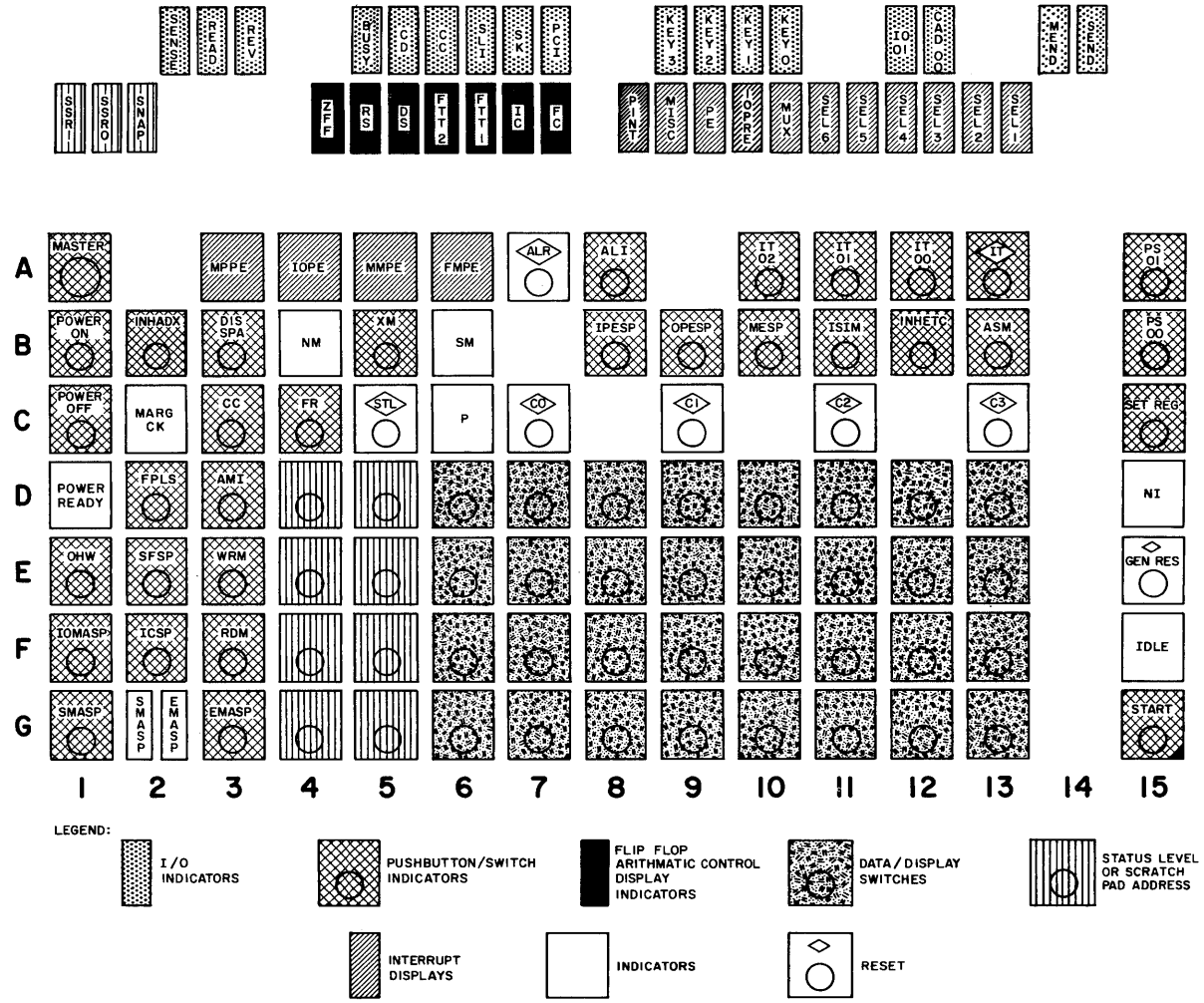


Figure 1-12. Model 70/55 Maintenance Panel Controls and Indicators

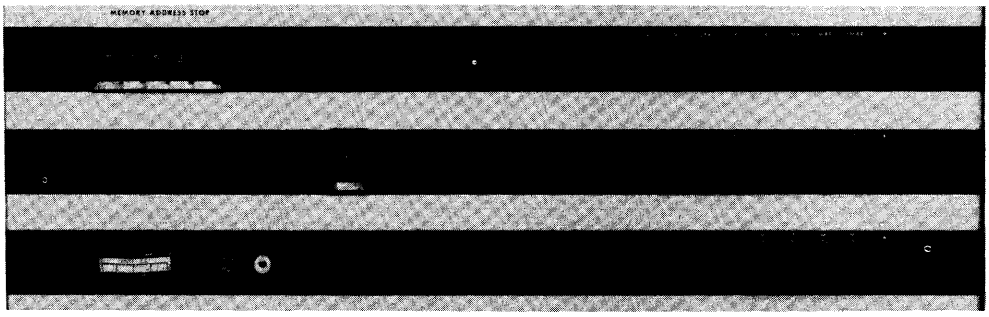


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Figure 1-13. Register Selection and Display Controls

Table 1-4. Model 70/55 Maintenance Panel (Indicators and Controls)

(Reference Fig. 1-12)

Figure Reference No.	Panel Designation	Description and Function
Top Row* I/O Indicators	SENSE	When a sense command is issued both of these indicators will light. When a WRITE or WRITE CONTROL command is issued, neither of these indicators will light.
	READ	Sense Command / Read Command
	REV	Reverse Command
	BUSY	Channel Busy
	CD	Chain Data Flag
	CC	Chain Command Flag
	SLI	Suppress Length Indicators Flag
	SK	Skip Flag
	PCI	Program Controlled Interrupt Flag
	KEY 3	I/O Key 3
	KEY 2	I/O Key 2
	KEY 1	I/O Key 1
	KEY 0	I/O Key 0
	IOCAD01	I/O Character Address
	IOCAD00	I/O Character Address
	MEND	Multiplexor End
	SEND	Selector End
2nd Row	SSR1	Snapshot Status Level Register 2^1
	SSR0	Snapshot Status Level Register 2^0
	SNAP	Snapshot Mode
	ZFF	Zero Flip-Flop
	RS	Result Sign
	DS	Digit Sign
	FTT2	First Time Through Storage
	FTT1	First Time Through
	IC	Initial Carry
	FC	Final Carry
	PINT	Program Interrupt Mode
	MISC	Misc. Int. — Any interrupt except Program Error, I/O terminate or Machine check.
	PE	Prog.Error Int. — Flag bit $2^{23}, 2^{24}, 2^{25}, 2^{26}, 2^{27}, 2^{28}, 2^{29}$ or 2^{30}
	IOPRE	IO Program Error Interrupt
	MUX	Multiplexor Interrupt
	SEL6	Selector 6 Interrupt
	SEL5	Selector 5 Interrupt
	SEL4	Selector 4 Interrupt
	SEL3	Selector 3 Interrupt
	SEL2	Selector 2 Interrupt
	SEL1	Selector 1 Interrupt

* Top Row indicators are shared by all seven channels. To display contents of a given channel, the channel number must be entered manually using the IT register (see A10 to A13).

Table 1-4. Model 70/55 Maintenance Panel (Indicators and Controls)(Cont'd.)

(Reference Fig. 1-12)

Figure Reference No.	Panel Designation	Description and Function
A 1	MASTER	This alternate action switch is used to enable the power supply control circuits and must be in the ON condition before the POWER ON switch can be activated. The switch can be used as an emergency off switch, in which case AC power is disconnected bypassing the normal DC power off sequencing and causing the power failure interrupt to be set in the processor. The indicator is turned on upon the pressing of this switch and remains on until the switch is pressed again to turn off power. Whenever this switch is in its OFF condition, the MASTER on the Operator's Display Panel is ineffective. NOTE: This switch is duplicated on the 70/97 Operator's Console Panel.
B 1	POWER ON	When this POWER ON momentary contact switch is pressed it will permit the DC voltage of the processor to be turned on. The indicator is turned on when the voltages start from zero and turns off when the voltages reach zero. IMPORTANT: This switch is ineffective until both MASTER switches are ON.
C 1	POWER OFF	This POWER OFF momentary contact switch and indicator is used to cause normal power off sequencing of the DC voltages in the Processor. The indicator comes on when the voltages reach zero and turns off when the DC voltages leave zero.
D 1	POWER READY	This indicator is turned on to indicate that the processor DC power is on and that the processor is ready for operation. This occurs when the processor power sequencing is completed and remains on until power is removed from the processor, either at the completion of power off sequencing, or emergency power off procedures.
E 1	OHW	This OVERHEAT WARNING indicator will light whenever the temperature in the Processor has exceeded its environmental design. The Pushbutton Switch serves to lamp check the Maintenance Panel. NOTE: This indicator is duplicated on the Operator's Display Panel.

Table 1-4. Model 70/55 Maintenance Panel (Indicators and Controls)(Cont'd.)

(Reference Fig. 1-12)

Figure Reference No.	Panel Designation	Description and Function
F 1	IOMASP	The I/O MEMORY ADDRESS STOP (alternate action switch) when set, causes the processor to stop at the word of the main memory address set in the memory address digi-switches during I/O servicing. This memory address equality is indicated by the EMASP indicator (G2b).
G 1	SMASP	The STATICIZING MEMORY ADDRESS STOP (alternate action switch) when set, will cause the processor to stop when the instruction located in the address set in the digi-switches is first accessed during staticizing. This memory address equality is indicated by the SMASP indicator (G2a).
B 2	INHADX	Inhibit Address Exception. This switch should only be used when cycling main memory, or clearing Memory Protect.
C 2	MARG CK	When MARGINAL CHECK indicator is lit it indicates that main memory is in the marginal check mode. When any position of the Memory Bank Selection switch is pressed, this indicator is turned on and remains on until the switch is reset.
D 2	FPLS	Setting the FIRST PROCESSING LEVEL (alternate action switch) will cause the processor to stop just before executing the first level of the next instruction staticized.
E 2	SFSP	The SINGLE FUNCTION STOP alternate action switch provides the means for manually stepping through an instruction, one status level at a time.
F 2	ICSP	This INSTRUCTION COMPLETE STOP alternate action switch when pressed will cause the processor to halt at the completion of the current instruction. Pressing this switch will turn on the indicator light and will generate ISIM. Pressing the START switch while ICSP is activated will cause the Processor to execute one instruction and stop. NOTE: This switch may be used to stop the Processor in the same manner as that of the STOP switch on the Operator's Display Panel.

Table 1-4. Model 70/55 Maintenance Panel (Indicators and Controls)(Cont'd.)

(Reference Fig. 1-12)

Figure Reference No.	Panel Designation	Description and Function
G 2a G 2b	SMASP EMASP	STATICIZING MEMORY ADDRESS STOP equality. EXECUTE MEMORY ADDRESS STOP equality.
A 3	MPPE	The MEMORY PROTECTION PARITY ERROR indicator when lit indicates that a parity error has been detected in accessing the memory protection key.
B 3	DIS SPA	The DISPLAY SCRATCH PAD ADDRESS alternate action switch operates in conjunction with D4, E4, F4, G4, D5, E5, F5 and G5 indicators. When B3 is reset (not lighted), the above indicators represent the hexadecimal number of the status level to be executed. When B3 is set, the above indicators represent the hexadecimal code of the scratch pad address selected by a status level. When B3 is set, D4, E4 and F4 have no meaning.
C 3	CC	The CONTINUOUS CYCLING alternate action switch is used to cycle memory. See "Cycling Memory" in the Operation Section.
D 3	AMI	When this ADDRESS MODIFICATION INHIBIT alternate action switch is set, a normal address incrementing is inhibited to allow repeated addressing of the memory location currently being accessed. Pressing the switch turns on the indicator.
E 3	WRM	When this WRITE MEMORY alternate action switch is set, data entered by means of the Data/Display switches are written to a specified memory location when the START switch is pressed. Pressing this switch turns on the indicator.
F 3	RDM	This READ MEMORY alternate action switch is used to read data from memory which will be displayed on the Data/Display switches.
G 3	EMASP	This EXECUTE MEMORY ADDRESS STOP alternate action switch provides the main memory address comparison during instruction executions. When this switch is set, the Processor will compare the address of each main memory location accessed during instruction execution (including I/O initiation and interrupt processing but excluding I/O servicing) with the address set in the Memory Address Stop Switches.

Table 1-4. Model 70/55 Maintenance Panel (Indicators and Controls) (Cont'd.)

(Reference Fig. 1-12)

Figure Reference No.	Panel Designation	Description and Function
G 3 (Cont'd.)	EMASP	The indicator is turned on when the switch is set. When equality is met, the separate EMASP equality indicator is turned on and the Processor is halted. NOTE: This switch may be set in combination with other MASP operate switches.
A 4	IOPE	The INPUT/OUTPUT PARITY ERROR indicator is turned on whenever the Processor detects a read parity error from an input device or if any I/O error occurs during a load operation.
B 4	NM	NORMAL MODE - The machine is processing normal mode status levels.
C 4	FR	This FUNCTION REPEAT alternate action switch when pressed will cause the repetition of a single status level to be performed by the Processor and will light the indicator.
D 4 E 4 F 4 G 4 D 5 E 5 F 5 G 5		These switch/indicators operate in conjunction with the DIS SPA (B3) switch. They select or indicate the status level or the Scratch Pad Address. These switches only set or reset the status level in the normal mode, NM (B4) must be lit.
A 5	MMPE	This MAIN MEMORY PARITY ERROR indicator is lit whenever a parity error has been detected in the main memory.
B 5	XM	When lit, the processor is operating in the multiplexor mode (X) (Multiplexor servicing). The switch enables the operator to display the Multiplexor status level register.
C 5	STL	Reset - operates with the DIS SPA switch to reset the status level or scratch pad address indicators. the NM status level will be reset regardless of the NM/XM/SM indicators.
A 6	FMPE	This FAST MEMORY PARITY ERROR indicator is lit whenever a parity error has been detected in the fast memory of the Processor.

Table 1-4. Model 70/55 Maintenance Panel (Indicators and Controls)(Cont'd.)

(Reference Fig. 1-12)

Figure Reference No.	Panel Designation	Description and Function
B 6	SM	When lit, the 70/55 is processing Selector status levels (servicing).
C 6	P	PARITY indicator for Main Memory Register and for Fast Memory location (odd parity). This indicator shows the correct Data Register parity only when reading from the Fast Memory or when displaying the Main Memory Register.
D6 - D13 E6 - E13 F6 - F13 G6 - G13	-	These (32) DATA/DISPLAY momentary contact switches are used to display or modify the contents of hardware registers, fast memory or main memory as selected by the appropriate switches. Selection of register or memory location to be displayed is determined by the applicable switches. Further description of data display and register selection can be found in Figure 1-14.
A 7	ALR	This ALARM RESET momentary switch is used to reset MPPE, MMPE, IOPE and FMPE indications on the processor.
C 7 C 9 C11 C13	C 0 C 1 C 3 C 4	RESET momentary contact switches are used for resetting the Data/Display indicators, i.e., one for each byte.
A 8	ALI	When this ALARM INHIBIT alternate switch is set, the processor will not execute actions normally performed as a result of machine errors. The error indicator(s) will be lit but in all other respects the error will be ignored. This switch does not inhibit error actions at the I/O control electronics.
B 8	IPESP	The PROGRAM ERROR IMMEDIATE STOP alternate action switch is used to halt the processor upon detection of a program error. This switch when set, turns on the indicator.
B 9	OPESP	When this PROGRAM ERROR ORDERLY STOP alternate action switch is set, subsequently detected program errors will cause the Processor to be halted after completion of the current instruction. I/O servicing (e.g., data transfer) may continue to completion. Pressing this switch turns on the indicator.

Table 1-4. Model 70/55 Maintenance Panel (Indicators and Controls) (Cont'd.)

(Reference Fig. 1-12)

<table>
<tr><th>Figure Reference No.</th><th>Panel Designation</th><th>Description and Function</th></tr>
<tr><td>B 9 (Cont'd.)</td><td>OPESP</td><td><u>NOTE</u>: A maximum of 10 seconds may elapse between detection of a program error and processor halt. Interrupts occurring during this time will not be taken.</td></tr>
<tr><td>A10
A11
A12
A13</td><td>IT02
IT01
IT00
IT</td><td>INITIATION AND TERMINATION switch/indicators can display the I/O Commands, Flags and Keys last used by the channel.
<table><tr><th>IT02</th><th>IT01</th><th>IT00</th><th></th></tr><tr><td>1</td><td>1</td><td>1</td><td>Selector Channel 6</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Selector Channel 5</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Selector Channel 4</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Selector Channel 3</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Selector Channel 2</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Selector Channel 1</td></tr><tr><td>0</td><td>0</td><td>0</td><td>Multiplexor Channel</td></tr></table>The IT02 - IT00 will display the last I/O channel if the machine comes to a normal stop.</td></tr>
<tr><td>B10</td><td>MESP</td><td>The MACHINE ERROR STOP alternate action switch is used to halt the Processor immediately upon detection of a machine error. Pressing this switch will turn on the indicator.</td></tr>
<tr><td>B11</td><td>ISIM</td><td>This INHIBIT SIMULTANEITY alternate action switch is used to perform normal processing and Input/Output servicing in a serial mode. When an I/O instruction is initiated, no further processing will take place until the termination of the input/output occurs. The switch must be set prior to the initiation of the I/O.</td></tr>
<tr><td>B12</td><td>INHETC</td><td>This switch inhibits decrementing of the Elapsed Time Clock.</td></tr>
<tr><td>B13</td><td>ASM</td><td>This ADDRESS SHADED MEMORY alternate action switch allows the addressing of non-addressable memory for display or modification. Pressing this switch causes the indicator to be lit.</td></tr>
</table>

Table 1-4. Model 70/55 Maintenance Panel (Indicators and Controls) (Cont'd.)

(Reference Fig. 1-12)

<table>
<tr><th>Figure Reference No.</th><th>Panel Designation</th><th>Description and Function</th></tr>
<tr><td>A15

B15</td><td>PS01

PS00</td><td>These two PROCESSOR STATE momentary switches when used permit the processor state to be changed when the Processor is halted. The indicators display the processor state. This indication is:

<table>
<tr><th>PS 2^1</th><th>PS 2^0</th><th>Processor State</th></tr>
<tr><td>0</td><td>0</td><td>4</td></tr>
<tr><td>0</td><td>1</td><td>3</td></tr>
<tr><td>1</td><td>0</td><td>2</td></tr>
<tr><td>1</td><td>1</td><td>1</td></tr>
</table>

Thus, to change from state 1 (11) to state 2 (10) press switch PS 2^0. GEN RES sets PS2^1 and PS2^0, pressing either pushbutton resets its corresponding indicator.</td></tr>
<tr><td>C15</td><td>SET REG</td><td>This switch is used in conjunction with the register selector strip switches. See Operation section for its use.</td></tr>
<tr><td>D15</td><td>NI</td><td>The NON INTERRUPTABLE indicator when lit, means that a status level is in process which cannot be interrupted by I/O servicing.</td></tr>
<tr><td>E15</td><td>GEN RES</td><td>This GENERAL RESET momentary contact switch when pressed will reset the system conditions to a state enabling an orderly start-up.

NOTE: This switch is duplicated on the Operator's Display Panel.</td></tr>
<tr><td>F15</td><td>IDLE</td><td>This indicator is turned on when the Idle instruction is operating.

NOTE: This indicator is duplicated on the Operator's Display Panel.</td></tr>
<tr><td>G15</td><td>START</td><td>Pressing and releasing this START momentary contact switch will start the Processor. The indicator is also lit at the same time, and will remain lit until the Processor is halted. The indicator is also turned on whenever a Load operation, from the Operator's Display Panel, has been initiated.

NOTE: This indicator is duplicated on the Operator's Display Panel.</td></tr>
</table>

Table 1-4. Model 70/55 Maintenance Panel (Indicators and Controls) (Continued)

Schematic No.	Panel Name	Source/ Destination	Description and Function
SDS806	-	217B3F,806B4B	D13
SDS807	-	218B7E,803B7C	D17
SDS808	-	218B3F,803B4B	D21
SDS809	-	219B7D,805B7C	D25
SDS810	-	219B3F,805B4B	D29
SDS903	-	215A8A,804A8A	D00
SDS904	-	216A8A,804A5A	D04
SDS905	-	217B8D,806B8C	D08
SDS906	-	217B5E,806B5B	D12
SDS907	-	218B8D,803B8B	D16
SDS908	-	218B4E,803B5B	D20
SDS909	-	219B8D,805B8B	D24
SDS910	-	219B4E,805B5B	D28
			These (32) DATA/DISPLAY momentary contact switches are used to display or modify the contents of hardware registers, fast memory or main memory as selected by the appropriate switches. Selection of register or memory location to be displayed is determined by the applicable switches. Further description of data display and register selection can be found in Figure 1-14.
S511	STL	386C6,290D8B	Status Level Register Reset Reset - operates with the DIS SPA switch to reset the status level or scratch pad address indicators. The NM status level will be reset regardless of the NM/XM/SM indicators.

Table 1-4. Model 70/55 Maintenance Panel (Indicators and Controls) (Continued)

Schematic No.	Panel Name	Source/ Destination	Description and Function
SDS512	FR	387D8,290D8B	Function Repeat This alternate action switch when pressed will cause the repetition of a single status level to be performed by the Processor and will light the indicator.
SDS611	-	290A4B,C4A, 301B6F	STL/SPA Register (STL3)
SDS612	-	290A7A,C7A	STL/SPA Register (STL7)
SDS711	-	290A3B,C3A, 301B5D	STL/SPA Register (STL2)
SDS712	-	290A7B,C6A	STL Register (STL6)
SDS811	-	290A2C,C2A 301B4E	STL/SPA Register (STL1)
SDS812	-	290A6B,C6B	STL Register (STL5)
SDS911	-	290A2D,C2B, 301B3D	STL/SPA Register (STL0)
SDS912	-	290A5B,C2B, 301B8C	STL Register (STL4) These switch/indicators operate in conjunction with the DIS SPA (B3) switch. They select or indicate the status level or the Scratch Pad Address. These switches only set or reset the status level in the normal mode, NM (B4) must be lit.
SDS513	CC	387D8,253B7B	Continuous Cycle This alternate action switch is used to cycle memory. See "Cycling Memory" in the Operation Section.
DS514	MARG.CK	387B4	Marginal Check Indicator It indicates that main memory is in the marginal check mode. When any position of the Memory Bank Selection switch is pressed, this indicator is turned on and remains on until the switch is reset.

Register Select Switches	P	C0		C1		C2		C3
FMAR Fast Memory Address Register								FMAR03
							FMAR06	FMAR02
							FMAR05	FMAR01
							FMAR04	FMAR00
MAR Main Memory Address Register					MAR15	MAR11	MAR07	MAR03
				MAR18	MAR14	MAR10	MAR06	MAR02
				MAR17	MAR13	MAR09	MAR05	MAR01
				MAR16	MAR12	MAR08	MAR04	MAR00
MR - Main Memory	x 31	x 27	x 23	x 19	x 15	x 11	x 07	x 03
URx- Utility Register	x 30	x 26	x 22	x 18	x 14	x 10	x 06	x 02
IRx- Intermediate Register	x 29	x 25	x 21	x 17	x 13	x 09	x 05	x 01
	x 28	x 24	x 20	x 16	x 12	x 08	x 04	x 00
OPR Operation Code Register	ILC-1	xPMR03	UCAD02	DCAD02	xOPR07	xOPR03	xGPM03	xGPL03
	ILC-2	xPMR02	UCAD01	DCAD01	xOPR06	xOPR02	xGPM02	xGPL02
	xCCR01	xPMR01	UCAD00	DCAD00	xOPR05	xOPR01	xGPM01	xGPL01
	xCCR00	xPMR00			xOPR04	xOPR00	xGPM00	xGPL00
N N Counter		x N03	xKR03	x A				GPR03
	x N06	x N02	xKR02		MDR02	FC		GPR02
	x N05	x N01	xKR01		MDR01	IC		GPR01
	x N04	x N00	xKR00	xNPRIV	MDR00			GPR00
STAT	PSTLR7	PSTLR3	STLR7	STLR3	FTT2	RS	CFF8	CFF4
	PSTLR6	PSTLR2	STLR6	STLR2	FTT1	CFF11	CFF7	CFF3
	PSTLR5	PSTLR1	STLR5	STLR1	ZFF	CFF10	CFF6	CFF2
	PSTLR4	PSTLR0	STLR4	STLR0	DS		CFF5	CFF1

x Can be modified through Register Select Switch & Set Register Function

Figure 1-14. Register Selection and Display

1. FMAR Fast Memory Address (Display only)

2. MAR Main Memory Address (Display only)

3. MR Main Memory Data (Display only)

4. UR Utility Register

5. IR Intermediate Register

6. OPR Operation Code Register - which displays the following:

ILC-1 ILC-2	Instruction Length Counter (Display only)
CCR01 CCR00	Condition Code Register
PMR03 PMR02 PMR01 PMR00	Program Mask Register
UCAD02——►UCAD00	UR Character Address Character Address (C0, C1, C2, C3) (Display only) Digit Address (Left/Right) (Most/Least)
DCAD02——►DCAD00	DR Character Address (Display only) Character Address (C0, C1, C2, C3) Digit Address (Left/Right) (Most/Least)
OPR07——►OPR00	Operation Code Register
GPM03——►GPM00	General Purpose Register (Most Significant Digit)
GPL03——►GPL00	General Purpose Register (Least Significant Digit) GPM contains R1, after staticizing GPL contains R2, after staticizing

7. N N Counter which displays the following:

N06——►N00	N Counter
KR03——►KR00	Key Register
A	USASCII Bit
N PRIV	Non Privilege Bit
MDR02——►MDR00	Multiply & Divide Register
FC	Final Carry Indicator (Display only)
IC	Initial Carry Indicator (Display only)
GPR03——►GPR00	General Purpose Register (Display only)

8. STAT Status Level Register which displays the following:
(Display only)

PSTLR7——►PSTLR0	Pre-Status Level Register (Display only)
STLR7——►STLR0	Status Level Register (Display only)

FTT2		First Time Through Two
FTT1		First Time Through One
ZFF		Zero Flip Flop
DS		Digit Sign
RS		Results Sign
CFF11	⟶ CFF1	Control Flip Flops

Hardware registers, with exception of MR and UR, as noted on Figure 1-14 may be changed in the following manner:

1. Press the appropriate register select switch.
2. Reset the character(s) to be changed in the data/display indicators.
3. Set the new data into the data/display switches.
4. Press the set register switch (C15).

To change data in the UR;

1. Press the UR selector switch.
2. Press all indicators which are to remain lit (even though they are already lit).
3. Modify those indicators that are to be modified by:
   a. Reset the byte to be modified.
   b. Set in the new information.
4. Press the set register switch.

1.5 FEATURES

1.5.1 INTERRUPT

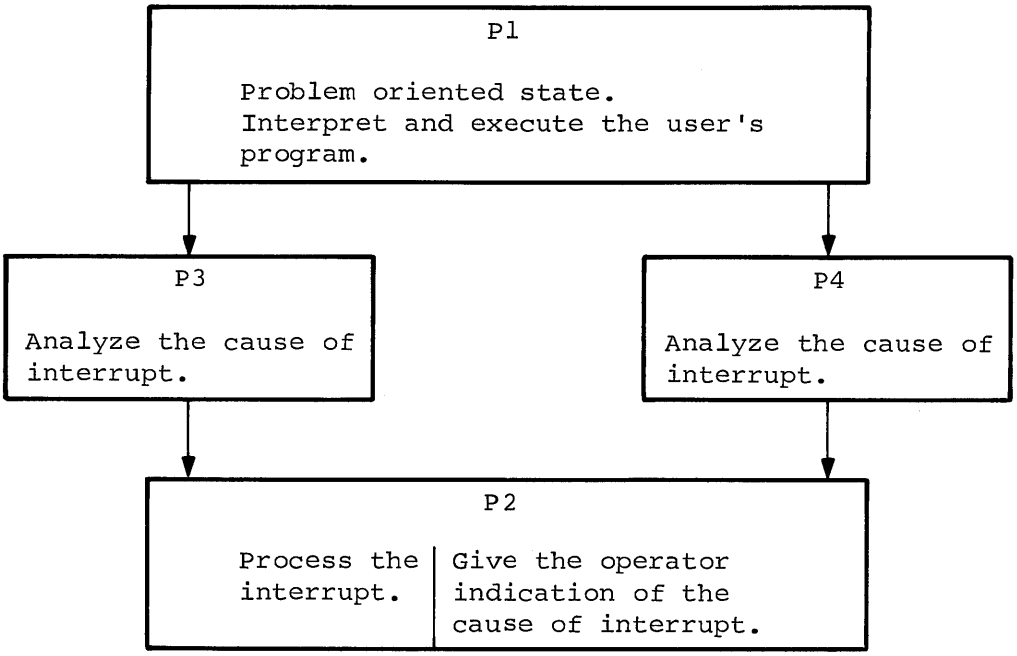
The model 70/55 Processor has four distinct processor states to provide extremely fast interrupt servicing. Combined with the program systems control, these processor states provide efficient interrupt handling.

Upon detection of interrupt the hardware initiates Processor States 3 or 4. It is the program's responsibility to determine what action is to be taken in any processor state.

Since each processing state has its own General-Purpose registers, Interrupt Status register, and Interrupt Mask register, the need for storing and reloading registers during interrupt processing is virtually eliminated.

Automatic interrupts occur as a result of errors in data or instruction specifications, input/output operations, external signals, equipment malfunctions, or arithmetic errors. The instruction being executed at the time of interrupt may be completed, suppressed, or terminated depending on the cause of the interrupt.

As an example the Processor States may be used as follows:



Register addressing in each of the processor states is given in Table 1-5.

Table 1-5. FM Register Addressing

Register Number Hexadecimal	Processor States Scratch Pad Registers – Digi-switch and Strip Switch Settings							
	P_1		P_2		P_3		P_4	
0	GR	C0	GR	80	IMR, P_1 State	40	Processor Utility	00
1	GR	C1	GR	81	ISR, P_1 State	41	Processor Utility	01
2	GR	C2	GR	82	P counter, P_1 State	42	Processor Utility	02
3	GR	C3	GR	83	Interrupt Flag Register	43	Processor Utility	03
4	GR	C4	GR	84	IMR, P_2 State	44	Processor Utility	04
5	GR	C5	GR	85	ISR, P_2 State	45	Processor Utility	05
6	GR	C6	GR	86	P counter, P_2 State	46	Processor Utility	06
7	GR	C7	GR	87	GR	47	Processor Utility	07
8	GR	D0	GR	90	IMR, P_3 State	50	GR	10
9	GR	D1	GR	91	ISR, P_3 State	51	GR	11
A	GR	D2	GR	92	P counter, P_3 State	52	GR	12
B	GR	D3	GR	93	GR	53	GR	13
C	GR	D4	GR	94	GR	54	IMR, P_4 State	14
D	GR	D5	GR	95	GR	55	ISR, P_4 State	15
E	GR	D6	GR	96	GR	56	P counter, P_4 State	16
F	GR	D7	GR	97	GR/Weight	57	GR/Weight	17

GR = General Register
IMR = Interrupt Mask Register
ISR = Interrupt Status Register

Most interrupts may be inhibited or permitted in any state by the program. A Manual Request interrupt is held off during a 9C (Start Device) instruction. If an interrupt occurs and is permitted, conditions existing in the interrupted state will be automatically stored. Control is then passed to the Interrupt Control State (P_3) or Machine Condition State (P_4) depending upon the cause of the interrupt. The priority of the interrupt is established and an analysis is made to determine the proper linkage to the Interrupt Response State (P_2) so that the interrupt may be processed. This is a software function, usually handled by an executive routine.

If several interrupts occur at the same time, the one having the highest priority will be processed. The remaining interrupts will be processed in turn depending upon their priority.

Table 1-6 summarizes all of the interrupt conditions, their respective priorities, the interrupt state which each initiates, and a brief description of the cause of interrupt.

Table 1-6. 70/55 Interrupt Conditions

Priority	Condition	State Initiated	Explanation
1	Power Failure	4	Power failure in processor or memory.
2	Machine Check	4	Parity error or equipment malfunction.
3	External Signal 1	3	Signal received on one of the six external lines associated with the direct-control feature.
4	External Signal 2	3	
5	External Signal 3	3	
6	External Signal 4	3	
7	External Signal 5	3	
8	External Signal 6	3	
9	Not Specified		
10	Selector 1	3	A device on the associated selector or multiplexor channel requires servicing.
11	Selector 2	3	
12	Selector 3	3	
13	Selector 4	3	
14	Selector 5	3	
15	Selector 6	3	
16	Multiplexor	3	
17	Elapsed Time Clock	3	Elapsed time count has expired.
18	Console Request	3	Manual request for interrupt by the operator.
19	Not Specified		
20	Not Specified		
21	Supervisor Call	3	Result of execution of Supervisor Call instruction to utilize programmed routines.
22	Privileged Operation	3	Privileged instruction attempted in non-privileged mode.
23	Op-Code Trap	3	Op Code attempted which is invalid for this processor.
24	Address Error	3	Invalid address, specification, or memory protect violation.
25	Data Error	3	Sign of operand incorrect in decimal arithmetic and editing, or incorrect field overlap.
26	Exponent Overflow	3	Result characteristic of floating-point operation is greater than 127.
27	Divide Error	3	Rules pertaining to Divide instruction have been violated.
28	Significance Error	3	Result of floating-point or subtract has zero fraction.
29	Exponent Underflow	3	Result characteristic of floating-point operation is less than zero.
30	Decimal Overflow	3	Result field is too small to contain the result of a decimal operation.
31	Fixed-Point Overflow	3	High-order carry or high-order significant bits lost in fixed-point operation.
32	Test Mode	3	Allows program control over processor during program testing.

1.5.2 ACCURACY CONTROL

The following accuracy controls are incorporated within the 70/55 Processor:

1. Each word (four bytes) read out of HSM is checked for odd parity.
2. Each data byte read in from a peripheral device is automatically checked for odd parity.
3. Each word read out of FM is automatically checked for odd parity.
4. Each pair of four bit keys read out of the Memory Protect Memory (optional) is automatically checked for odd parity.

NOTES:

1. If a Memory Protect parity error occurs, the Processor will stop.
2. If a HSM or DR parity error occurs, the interrupt routine will be initiated. However, if a HSM or DR parity error occurs when the machine is in Processor State 4, the Processor will stop.

1.5.3 OPTIONAL FEATURES

A variety of optional features are available to enhance the operation of the 70/55 Processor. These features provide specific functions and are incorporated into the electronic controls of the processor. The functions are described briefly below:

Feature 5001-55 Memory Protect, protects the information in the Main Memory from being destroyed by either Programming or by an input device.

Feature 5002-55 Elapsed Time Clock, incorporates real time control operation within the Processor.

Feature 5003-55 Direct Control, provides the means for the transfer of control and information between Processors.

Feature 5019-55 Elapsed Time Clock, provides an elapsed-time count in decrements of 1 millisecond.

Feature 5020 - This feature provides two Selector Channels and up to 15 input/output trunks (9 Multiplexor and 6 Selector Channels).

Feature 5022 - This feature provides four Selector Channels and up to 20 input/output trunks (9 Multiplexor and 11 Selector Channels).

Feature 5024 - This feature provides six Selector Channels and up to 24 input/output trunks (9 Multiplexor and 15 Selector Channels).

1.6 OPERATION

1.6.1 PREPARATION FOR OPERATION

Prior to undertaking the normal operating procedures, the following should be performed.

Inspect the Operator's Console Typewriter to see that there is a sufficient supply of paper and examine the condition of the inked ribbon.

Prior to the application of power to the Maintenance Console Panel and to the Operator's Console, make certain that the AC Distribution Panel circuit breaker switches are all in their ON condition.

1.6.2 NORMAL OPERATION

To apply power to the Processor:

1. Both MASTER switches (Operator's Console and Maintenance Panel) must be in their ON position to enable DC power control circuits. Press MASTER switch on the Operator's Console, the indicator will light. Press MASTER switch on the Maintenance Panel, its indicator will light. The MASTER switches may be used for emergency POWER OFF switches if it becomes necessary to do so.

2. Hold one hand over the fans in each equipment rack and make certain that they are operating. Examine filters and clean if necessary.

3. Press the POWER ON switch on the Maintenance Panel. The indicator will light upon the completion of the power-up sequence cycle, thus indicating the DC power has been applied. The POWER OFF indicator at the Maintenance Panel will be turned off and the POWER READY indicator on the Operator's Console will be turned on.

4. Press and hold down the IDLE pushbutton on the Operator's Console. This provides a lamp check for the console. Ascertain that all indicators on the console are lit.

5. Press and hold down the OHW pushbutton on the Maintenance Panel. This will provide a lamp check for all indicators and controls on the Maintenance Panel. Ascertain that all indicators and controls on the Maintenance Panel (except POWER OFF and OHW), are lit.

6. Press the GEN RES switch on either the Operator's Display Panel or the Maintenance Panel. The Processor is now conditioned for operation.

To remove power:

1. Press the POWER OFF switch on the Maintenance Panel. The DC power will cycle down and when the DC power is removed, the POWER ON indicator will go off and the POWER OFF indicator will light.

2. Press the MASTER switch to remove power.

1.6.2.1 Initial Program Loading

Initial Program Loading is accomplished from the Operator's Console in the following manner:

1. Initial Program Loading from Operator's Console.

   NOTE: It is assumed that the processor power is ready and the Maintenance Panel and Register Select switches are reset.

   a. Establish required conditions at input device.

   b. Press GEN RES switch to clear the processor to establish the required condition for start-up.

   c. Enter the channel and device number of loading device to the Load Unit Switches.

   d. Press LOAD switch. (One record, card or block will be read from input device to main memory starting at address zero.) After completion of the read, instructions are executed starting at location zero.

   e. When loading has been completed successfully, it will be indicated by the LOAD indicator light being turned off. The START (Run Indicator) will remain lit, (Program Running).

   f. In the event that in the process of loading, the loading is terminated due to an error condition the START (Run Indicator) will be turned off and the LOAD indicator will stay lit. In addition, the processor detected errors (MPPE, MMPE, FMPE, IOPE, or the Channel Interrupt) indicators on the Maintenance Panel and the ERROR indicator on the Operator's Display Panel will be lighted.

   g. To re-attempt an Initial Load function repeat from step a.

2. Read/Write Main Memory via the Maintenance Panel.

   The procedures for reading and displaying the contents of a Main Memory location using the Maintenance Panel is described as follows:

   NOTE: It is assumed that the processor is halted.

   To read a single word address in Main Memory.

   a. Set RDM Switch.

b. Write the Memory Address into Fast Memory Loc (31) Bits 2^{18} to 2^{2}.

c. Press Start. The full word will be displayed in the Data/ Display Indicators.

d. To read the next Memory Address press START again.

> NOTES: Location 31 in the Fast Memory will be updated by a full word address automatically unless AMI is set. In this case AMI must be reset and START PRESSED twice to obtain the next word from the memory
>
> Bits 2^{0} and 2^{1} of location 31 in F.M. have no meaning since RDM/WRM functions always obtain a full word from the memory (i.e., full word address 00, 04, 08, OC, etc.)

To write a single word address in Main Memory.

a. Set WRM Switch.

b. Write the Memory Address into F.M. Location 31, Bits 2^{18} to 2^{2}.

c. Reset Data/Display Indicators.

d. Enter data to be written to Main Memory into Data/Display Indicators.

e. Press Start.

When the Write is complete the Main Memory Address written into will be displayed in the Data/Display Indicators.

f. To write data into the next word address repeat steps c, d, and e.

To write and then read the same memory location.

a. Set AMI

b. Follow steps a through e for write.

c. Reset WRM Switch and set RDM Switch.

d. Press Start.

> NOTE: When both WRM & RDM Switches are set RDM takes precedence.

3. RDM/WRM Shaded Memory

   Process is similar to above except ASM must be set.

4. Read Fast Memory

   The procedures for reading a Fast Memory location using the Maintenance Panel is as follows:

   > NOTE: It is assumed that the processor is halted and that the Maintenance Panel switches are reset.

   a. Dial the hexadecimal value of the high order 4 bits of the desired Fast Memory Address in the Digi-Switch of the Fast Memory Address switch group.

   b. Press the switch position corresponding to the low order 3 bits of the desired Fast Memory address in the gang switch of the Fast Memory switch group.

   c. A word (32 bits) of the addressed Fast Memory location with its parity bit is displayed in the Data/Display switches.

5. Write Fast Memory

   The procedures for writing into a Fast Memory location using the Maintenance Panel is as follows:

   > NOTE: It is assumed that the processor is halted and the Maintenance Panel switches are reset.

   a. Dial the hexadecimal value of the high order 4 bits of the desired Fast Memory address in the Digi-Switch of the Fast Memory Address switch group.

   b. Press the switch position corresponding to the low order 3 bits of the desired Fast Memory Address in the gang switch of the Fast Memory Address switch group.

   c. Enter data via the Data/Display switches.

   d. Press the reset position of the Fast Memory Address gang switch to write.

6. Program Execution

   To execute a program that has been previosuly loaded into the Memory, perform the following:

a. Press the GEN RES pushbutton.

b. Place the starting address in FM location for program counter. For program state P1; digi-switch position 4 and gang switch position 2.

c. Press the START pushbutton.

7. Single Instruction Execution

A single instruction of a given program may be individually staticized and executed as follows:

a. Follow and observe steps a. and b. of the Program Execution, given above.

b. Press the ICSP (Instruction Complete Stop) pushbutton.

Press the START pushbutton. The selected instruction will be executed and the Processor will halt after a ten second delay which allows for I/O termination. Successively pressing the START pushbutton will cause additional instructions in sequence, to be executed. However, there is no ten second delay on any of the subsequent instructions executed (after the initially selected instruction).

8. Manual Instruction Set-up

Single instructions can be inserted and executed by observing the following:

a. Press the GEN RES pushbutton.

b. Enter the instruction into the desired Main Memory locations. (Refer to Write to Main Memory.)

c. Place the instruction address in the Fast Memory location for program counter P1.

d. Press the GEN RES pushbutton.

e. Press the ICSP pushbutton.

f. Press the START pushbutton to execute the instruction.

9. Error Detection and Interpretation

There are four error display indicators on the Maintenance Panel and one on the Operator's Display Panel.

The error display indicators on the Maintenance Panel are IOPE, MPPE, MMPE, and FMPE.

The error indicator on the Operator's Display Panel is identified as ERROR. To turn off these indicators press the alarm reset or GEN RES pushbuttons.

The IOPE indicator is lit whenever a character containing incorrect parity is received from a peripheral device; or during a Load operation whenever a specified device cannot be initiated. This error will also light the ERROR indicator. If this error is detected during a Load operation the processor will stop.

The MPPE indicator is lit whenever a character containing incorrect parity is read out of the Memory Protect Memory. This error will also light the ERROR indicator. When this error is detected the processor will stop.

NOTE: The Memory Protect Memory is an optional feature.

The MMPE indicator is lit when a character containing incorrect parity is read out of the Main Memory. This error also lights the ERROR indicator. If this error occurs when the processor is in Processor State 4, during Interrupt Processing, or when the MESP switch is set the machine will stop.

The FMPE indicator is lit when the data read out of the Fast Memory has detected incorrect parity. This error also lights the ERROR indicator and if this error occurs when the machine is in Processor State 4 or during Interrupt Processing, or when the MESP switch is set the machine will stop.

The ERROR indicator is also lit if a Program Error is detected while performing a Load Operation. If this occurs the machine will stop.

1.6.3 SPECIAL OPERATIONS

Tables 1-7 and 1-8 are furnished as reference material when performing special operations:

1.6.3.1 Manual Initiation of I/O

To execute a manual I/O instruction in the 70/55, the following information must be written into the Main Memory.

1. The instruction
2. Channel Address Word (always in location 48_{16})
3. Channel Command Word 1
4. Channel Command Word 2

For example, a block of 16 bytes of data is to be read into Memory location 00000 from device number 3 on Selector Channel two. The following program can be put in any available Main Memory location but for this example will start at 100_{16}.

Memory Address	Coded Instruction	Description
100	9C000203	Start Device
104	80000000	Idle
108	05000000	CCW1
10C	00000010	CCW2
48	00000108	CAW

1. Set the P1 Program Counter to 100 (FM 42). See Note.
2. Set the P3 Program Counter to 104 (FM 52).
3. Set the 2^{10} bit in the P1 Interrupt Mask Register. This bit allows the servicing of a Selector Channel 2 interrupt. This register is FM 40.
4. Press the GEN RES switch.
5. Press the START switch.

The I/O device should perform the read, terminate and idle in program state 3. To stop, press the FPLS switch.

The FM may now be examined to see that the instruction was completed correctly. In this case, the CAR (FM 62), CCR2 (FM 63), CCR1 (FM 64) and the SDB (FM 65) will show the Selector 2 Register settings.

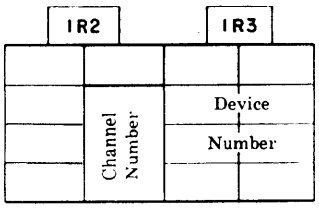
> NOTE: The FM addresses shown in this description are digi-switch and push-button switch selections.

1.6.3.2 I/O Operation Information

The I/O Instruction format (SI) is as follows:

OP		I_2						
9C	SDV	0	0					
9E	HDV	0	0	(B_1)	$+D_1=$			
9D	TDV	0	0	Channel	and			
9F	CKC	0	0	Device				

After staticizing the instruction examination of the IR will show the channel and device number as follows:



Contents of the three channel words are as follows:

CAW	K	0		Address of CCW				
HSM	E	0						
LOC	Y	0						
48_{16}		0						
CCW1	Command Code		Address of First Data Byte or Address of Next CCW if Command is XFER in Channel					
CCW2	CD	PCI	0	0				
	CC	0	0	0		Byte Count		
	SLI	0	0	0				
	SKIP	0	0	0				

COMMAND CODE	OPERATION
MMMM0001	SENSE
MMMB0010	READ REVERSE
MMMB0011	WRITE
MMMB0100	WRITE ERASE
MMMB0101	READ
MMMM0111	WRITE CONTROL
MMMM1001	TRANSFER IN CHANNEL

M (Modifier) — Indicates variations of the operation. Definition is provided in the Applicable I/O Device Manuals.

B — Burst Mode Bit.

Interpretation of the Condition Code Register at termination of an I/O Command follows:

CC	START DEVICE	HALT DEVICE	TEST DEVICE	CHECK CHANNEL
0	Operation Initiated	Operation not Terminated, Channel or Sub-Channel not Busy or Manual Request Interrupt Pending	Device Available	Channel Available
1	Operation not Initiated, Check CSB and SDB or Manual Request Interrupt Pending	Operation not Terminated, Check CSB and SDB	Device not Available, Check CSB and SDB or Manual Request Interrupt Pending	Term. Interrupt Pending in Selector Channel
2	Operation not Initiated, Channel or Sub-Channel Busy or Term Interrupt Pending	Operation was Terminated	Device not Available, Channel or Sub-Channel Busy	Selector Busy or MUX in Burst Mode Busy
3	Channel or Sub-Channel Inoperable	Not Terminated, Channel or Sub-Channel Inoperable	Device not Available, Channel or Sub-Channel Inoperable	Channel Inoperable

To Read/Write to Shaded Memory in conjunction with a particular device on the Multiplexor the following table shows addressing of the CAR, CCR1 and CCR2 for that device.

C2		C3	
Y	0	X_2	X_1
Y	0	X_2	X_1
X_2	0	X_1	0
X_2	0	X_1	0

Where YY is a hardware generated constant & $\overbrace{X_2X_2X_2X_2}^{\text{Hex Digit}}\ \overbrace{X_1X_1X_1X_1}^{\text{Hex Digit}}$ is the MUX device number.

When: YY = 01 Shaded Memory Address is the CCR2

YY = 10 Shaded Memory Address is the CCR1

YY = 11 Shaded Memory Address is the CAR

EXAMPLE: To read the CAR CCR2 or CCR1 for MUX device $(64)_{16}$. The Shaded Main Memory Address would be:

	C2								C3							
	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	Y	Y	X_2	X_2	0	0	0	0	X_2	X_2	X_1	X_1	X_1	X_1	0	0
CCR2	0	1	0	1	0	0	0	0	1	0	0	1	0	0	0	0
CCR1	1	0	0	1	0	0	0	0	1	0	0	1	0	0	0	0
CAR	1	1	0	1	0	0	0	0	1	0	0	1	0	0	0	0

1.6.3.3 Cycling Main Memory

To preset, clear or read Main Memory:

1. Set MESP Switch
2. Set ICSP Switch
3. Set CC Switch (Continuous Cycling)
4. Set INHADX Switch if continuous cycling is desired.

5. Press GEN RES Switch

6. Press STL Reset Switch

7. Set DIS SPA Switch

8. Set SPA Display equal to $(0D)_{16}$

9. Reset DIS SPA Switch

10. Set STL Display equal to $(25)_{16}$

11. Set "N" Counter (Least) equal to $(01)_{16}$

12. Set OPR equal to $(D0)_{16}$ for Write or $(D8)_{16}$ for Read, also set GPM and GPL $\neq 0$

13. Write data, to be written into Main Memory into Fast Memory location $(01)_{16}$

    In the case of a Read, F.M. LOC (01) will contain the data from the previous read.

14. Write the Main Memory starting address into F.M. Location $(07)_{16}$ - usually zero.

15. Press Start.

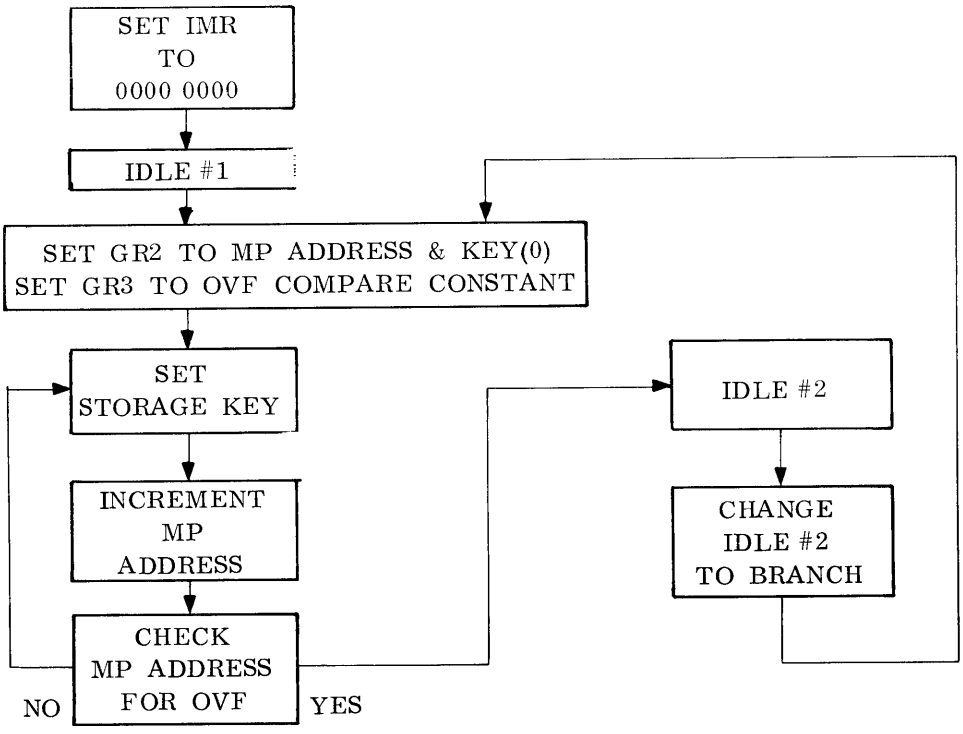
> NOTES: The Processor will stop when the whole memory has been cycled once, except when AMI switch or INHADX is set. In the AMI case only one word address will be read/written and SFSP Switch must be set to stop the machine. If INHADX is set the machine will cycle continuously.
>
> If a Main Memory Parity Error (MMPE) is detected, during a read the machine will stop and the memory address in error will be located in MAR (Reg. Select Switch) and the data in MR.
>
> To recycle the machine after a MMPE, steps 5 through 14 must be repeated.

1.6.3.4 Cycling Memory Protect Memory

On the 70/55 Processors which have the optional memory protect feature, the operators should know how to fill the memory protect memory with all zeros in order to correct a parity error. It would be useful for operators to punch the following program on a standard 80 column card and keep it handy for clearing the memory protect memory.

ROUTINE TO CLEAR MP STACK TO ZEROS

Address	Instruction	Remarks
0000	D800 0020 002C	Clear IMR to Zeros
0006	8000 0000	Idle #1
000A	D801 0062 002C	Set GR2 & GR3
0010	0822	Set Storage Key
0012	4A20 002A	Increment MP Address
0016	1923	Compare. Set CC1 if $\overline{\text{OVF}}$
0018	4740 0010	Branch Cond. if CC1 is set
001C	8000 0000	Idle #2
0020	D203 001C 0026	Replace Idle #2 with Unconditional Branch
0026	47F0 000A	Unconditional Branch
002A	0800	1/2 word K for Increment Bit
002C	0000 0000	K for GR2
0030	0008 0000	K for GR3



Flow Chart of the Clear Memory Protect Routine

To execute the Clear Memory Protect Memory Routine:

1. Load the Program at Location 0000.
2. Set INHADX Switch.
3. At Idle #1; press FPLS, GRES, Set ALI and press START.
4. At Idle #2; press FPLS, GRES, Reset ALI and press START.

	FORMAT	MSD 0	MSD 1	MSD 2	MSD 3	MSD 4	MSD 5	MSD 6
BRANCHING AND STATUS SWITCHING	RR	0 ———	———	———	———	SPM SET PROGRAM MASK	BALR BRANCH AND LINK	BCTR BRANCH ON COUNT
FIXED POINT FW AND LOGICAL	RR	1 LPR LOAD POSITIVE	LNR LOAD NEGATIVE	LTR LOAD AND TEST	LCR LOAD COMPLEMENT	NR AND	CLR COMPARE LOGICAL	OR OR
FLOATING POINT LONG	RR	2 LPDR LOAD POSITIVE (LONG)	LNDR LOAD NEGATIVE (LONG)	LTDR LOAD AND TEST (LONG)	LCDR LOAD COMPLEMENT (LONG)	HDR HALVE (LONG)	———	———
FLOATING POINT SHORT	RR	3 LPER LOAD POSITIVE (SHORT)	LNER LOAD NEGATIVE (SHORT)	LTER LOAD AND TEST (SHORT)	LCER LOAD COMPLEMENT (SHORT)	HER HALVE (SHORT)	———	———
FIXED POINT HALFWORD AND BRANCHING	RX	4 STH STORE HALFWORD	LA LOAD ADDRESS	STC STORE CHARACTER	IC INSERT CHARACTER	EX EXECUTE	BAL BRANCH AND LINK	BCT BRANCH ON ACCOUNT
FIXED POINT FW AND LOGICAL	RX	5 ST STORE WORD	———	———	———	N AND	CL COMPARE LOGICAL	O OR
FLOATING POINT LONG	RX	6 STD STORE (LONG)	———	———	———	———	———	———
FLOATING POINT SHORT	RX	7 STE STORE (SHORT)	———	———	———	———	———	———
BRANCHING, STATUS SWITCHING AND SHIFTING	RS	8 IDL IDLE	———	PC PROGRAM CONTROL	DIG DIAGNOSE	WRD WRITE DIRECT	RDD READ DIRECT	BXH BRANCH ON INDEX HIGH
LOGICAL AND I/O	RS/SI	9 STM STORE MULTIPLE	TM TEST UNDER MASK	MVI MOVE	———	NI AND	CLI COMPARE LOGICAL	OI OR
	SI	A ———	———	———	———	———	———	———
	SI	B ———	———	———	———	———	———	———
	SS	C ———	———	———	———	———	———	———
LOGICAL	SS	D SSP STORE SCRATCH-PAD	MVN MOVE NUMERICS	MVC MOVE	MVZ MOVE ZONES	NC AND	CLC COMPARE LOGICAL	OC OR
	SS	E ———	———	———	———	———	———	———
DECIMAL	SS	F ———	MVO MOVE WITH OFFSET	PACK PACK	UNPK UNPACK	———	———	———

INSTRUCTION FORMAT

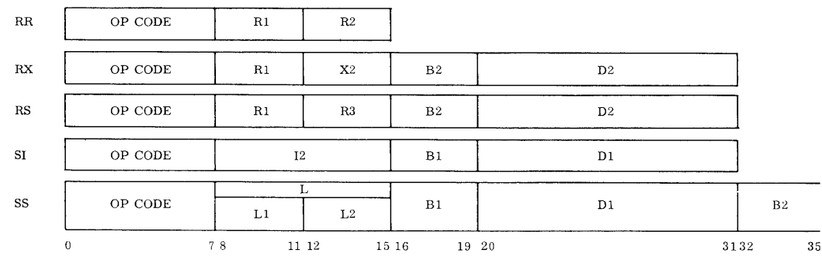


Table 1-7. Table of Instructions

LSD	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
				SPM SET PROGRAM MASK	BALR BRANCH AND LINK	BCTR BRANCH ON COUNT	BCR BRANCH ON CONDITION	SSK SET STORAGE KEY	ISK INSERT STORAGE KEY	SVC SUPERVISOR CALL					
	LOAD NEGATIVE	LTR LOAD AND TEST	LCR LOAD COMPLEMENT	NR AND	CLR COMPARE LOGICAL	OR OR	XR EXCLUSIVE OR	LR LOAD WORD	CR COMPARE WORD	AR ADD WORD	SR SUBTRACT WORD	MR MULTIPLY WORD	DR DIVIDE	ALR ADD LOGICAL	SLR SUBTRACT LOGICAL
	LOAD NEGATIVE (LONG)	LTDR LOAD AND TEST (LONG)	LCDR LOAD COMPLEMENT (LONG)	HDR HALVE (LONG)				LDR LOAD (LONG)	CDR COMPARE (LONG)	ADR ADD NORMALIZED (LONG)	SDR SUBTRACT NORMALIZED (LONG)	MDR MULTIPLY (LONG)	DDR DIVIDE (LONG)	AWR ADD UNNORMALIZED (LONG)	SWR SUBTRACT UNNORMALIZED (LONG)
	LOAD NEGATIVE (SHORT)	LTER LOAD AND TEST (SHORT)	LCER LOAD COMPLEMENT (SHORT)	HER HALVE (SHORT)				LER LOAD (SHORT)	CER COMPARE (SHORT)	AER ADD NORMALIZED (SHORT)	SER SUBTRACT NORMALIZED (SHORT)	MER MULTIPLY (SHORT)	DER DIVIDE (SHORT)	AUR ADD UNNORMALIZED (SHORT)	SUR SUBTRACT UNNORMALIZED (SHORT)
	LOAD ADDRESS	STC STORE CHARACTER	IC INSERT CHARACTER	EX EXECUTE	BAL BRANCH AND LINK	BCT BRANCH ON ACCOUNT	BC BRANCH ON CONDITION	LH LOAD HALFWORD	CH COMPARE HALFWORD	AH ADD HALFWORD	SH SUBTRACT HALFWORD	MH MULTIPLY HALFWORD		CVD CONVERT TO DECIMAL	CVB CONVERT TO BINARY
				N AND	CL COMPARE LOGICAL	O OR	X EXCLUSIVE OR	L LOAD WORD	C COMPARE WORD	A ADD WORD	S SUBTRACT WORD	M MULTIPLY WORD	D DIVIDE	AL ADD LOGICAL	SL SUBTRACT LOGICAL
								LD LOAD (LONG)	CD COMPARE (LONG)	AD ADD NORMALIZED (LONG)	SD SUBTRACT NORMALIZED (LONG)	MD MULTIPLY (LONG)	DD DIVIDE (LONG)	AW ADD UNNORMALIZED (LONG)	SW SUBTRACT UNNORMALIZED (LONG)
								LE LOAD (SHORT)	CE COMPARE (SHORT)	AE ADD NORMALIZED (SHORT)	SE SUBTRACT NORMALIZED (SHORT)	ME MULTIPLY (SHORT)	DE DIVIDE (SHORT)	AU ADD UNNORMALIZED (SHORT)	SU SUBTRACT UNNORMALIZED (SHORT)
		PC PROGRAM CONTROL	DIG DIAGNOSE	WRD WRITE DIRECT	RDD READ DIRECT	BXH BRANCH ON INDEX HIGH	BXLE BRANCH ON INDEX LOW OR EQUAL	SRL SHIFT RIGHT SINGLE LOGICAL	SLL SHIFT LEFT SINGLE LOGICAL	SRA SHIFT RIGHT SINGLE	SLA SHIFT LEFT SINGLE	SRDL SHIFT RIGHT DOUBLE LOGICAL	SLDL SHIFT LEFT DOUBLE LOGICAL	SRDA SHIFT RIGHT DOUBLE	SLDA SHIFT LEFT DOUBLE
	TEST UNDER MASK	MVI MOVE		NI AND	CLI COMPARE LOGICAL	OI OR	XI EXCLUSIVE OR	LM LOAD MULTIPLE				SDV START DEVICE	TDV TEST DEVICE	HDV HALT DEVICE	CKC CHECK CHANNEL
	MOVE NUMERICS	MVC MOVE	MVZ MOVE ZONES	NC AND	CLC COMPARE LOGICAL	OC OR	XC EXCLUSIVE OR	LSP LOAD SCRATCH-PAD				TR TRANSLATE	TRT TRANSLATE AND TEST	ED EDIT	EDMK EDIT AND MARK
	MOVE WITH OFFSET	PACK PACK	UNPK UNPACK					ZAP ZERO AND ADD	CP COMPARE DECIMAL	AP ADD DECIMAL	SP SUBTRACT DECIMAL	MP MULTIPLY DECIMAL	DP DIVIDE DECIMAL		

N FORMAT

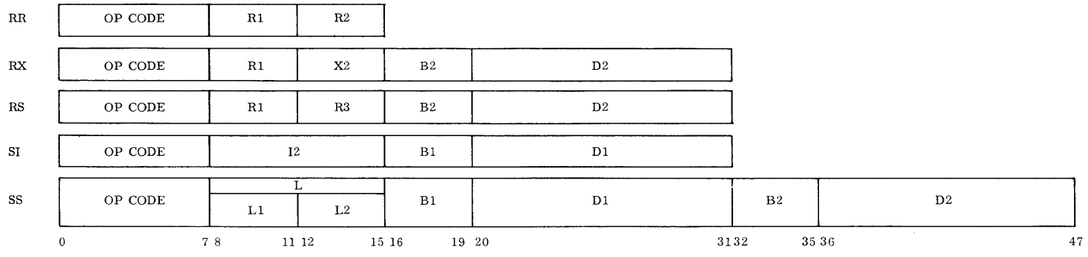


Table 1-8. F.M. Layout and Register Assignments

DIGI-SWITCH (DESIGNATION)	GANG SWITCH 7	6	5	4	3	2	1	0
F	7F UTILITY NO. 3	7E UTILITY NO. 2	7D ASSEMBLY STATUS REGISTER	7C CHANNEL COMMAND REGISTER I	7B CHANNEL COMMAND REGISTER II	7A CHANNEL ADDRESS REGISTER	79 PROCESSOR UTILITY NO. 19	78 PROCESSOR UTILITY NO. 18
			← I/O CHANNEL REGISTERS - SELECTOR NO. 6 →					
E	77 ← FLOATING POINT REGISTER NO. 6 →	76	75 ← FLOATING POINT REGISTER NO. 4 →	74	73 ← FLOATING POINT REGISTER NO. 2 →	72	71 ← FLOATING POINT REGISTER NO. 0 →	70
D	6F GENERAL PURPOSE REGISTER NO. 15 P1	6E GENERAL PURPOSE REGISTER NO. 14 P1	6D GENERAL PURPOSE REGISTER NO. 13 P1	6C GENERAL PURPOSE REGISTER NO. 12 P1	6B GENERAL PURPOSE REGISTER NO. 11 P1	6A GENERAL PURPOSE REGISTER NO. 10 P1	69 GENERAL PURPOSE REGISTER NO. 9 P1	68 GENERAL PURPOSE REGISTER NO. 8 P1
C	67 GENERAL PURPOSE REGISTER NO. 7 P1	66 GENERAL PURPOSE REGISTER NO. 6 P1	65 GENERAL PURPOSE REGISTER NO. 5 P1	64 GENERAL PURPOSE REGISTER NO. 4 P1	63 GENERAL PURPOSE REGISTER NO. 3 P1	62 GENERAL PURPOSE REGISTER NO. 2 P1	61 GENERAL PURPOSE REGISTER NO. 1 P1	60 GENERAL PURPOSE REGISTER NO. 0 P1
B	5F UTILITY NO. 3	5E UTILITY NO. 2	5D ASSEMBLY STATUS REGISTER	5C CHANNEL COMMAND REGISTER I	5B CHANNEL COMMAND REGISTER II	5A CHANNEL ADDRESS REGISTER	59 PROCESSOR UTILITY NO. 17	58 PROCESSOR UTILITY NO. 16
			← I/O CHANNEL REGISTERS - SELECTOR NO. 5 →					
A	57 UTILITY NO. 3	56 UTILITY NO. 2	55 ASSEMBLY STATUS REGISTER	54 CHANNEL COMMAND REGISTER I	53 CHANNEL COMMAND REGISTER II	52 CHANNEL ADDRESS REGISTER	51 PROCESSOR UTILITY NO. 15	50 PROCESSOR UTILITY NO. 14
			← I/O CHANNEL REGISTERS - SELECTOR NO. 4 →					
9	4F GENERAL PURPOSE REGISTER NO. 15 P2	4E GENERAL PURPOSE REGISTER NO. 14 P2	4D GENERAL PURPOSE REGISTER NO. 13 P2	4C GENERAL PURPOSE REGISTER NO. 12 P2	4B GENERAL PURPOSE REGISTER NO. 11 P2	4A GENERAL PURPOSE REGISTER NO. 10 P2	49 GENERAL PURPOSE REGISTER NO. 9 P2	48 GENERAL PURPOSE REGISTER NO. 8 P2
8	47 GENERAL PURPOSE REGISTER NO. 7 P2	46 GENERAL PURPOSE REGISTER NO. 6 P2	45 GENERAL PURPOSE REGISTER NO. 5 P2	44 GENERAL PURPOSE REGISTER NO. 4 P2	43 GENERAL PURPOSE REGISTER NO. 3 P2	42 GENERAL PURPOSE REGISTER NO. 2 P2	41 GENERAL PURPOSE REGISTER NO. 1 P2	40 GENERAL PURPOSE REGISTER NO. 0 P2
7	3F UTILITY NO. 3	3E UTILITY NO. 2	3D ASSEMBLY STATUS REGISTER	3C CHANNEL COMMAND REGISTER I	3B CHANNEL COMMAND REGISTER II	3A CHANNEL ADDRESS REGISTER	39 PROCESSOR UTILITY NO. 13	38 PROCESSOR UTILITY NO. 12
			← I/O CHANNEL REGISTERS - SELECTOR NO. 3 →					
6	37 UTILITY NO. 3	36 UTILITY NO. 2	35 ASSEMBLY STATUS REGISTER	34 CHANNEL COMMAND REGISTER I	33 CHANNEL COMMAND REGISTER II	32 CHANNEL ADDRESS REGISTER	31 PROCESSOR UTILITY NO. 11	30 PROCESSOR UTILITY NO. 10
			← I/O CHANNEL REGISTERS - SELECTOR NO. 2 →					
5	2F GENERAL PURPOSE REGISTER NO. 15 (WEIGHT) P3	2E GENERAL PURPOSE REGISTER NO. 14 P3	2D GENERAL PURPOSE REGISTER NO. 13 P3	2C GENERAL PURPOSE REGISTER NO. 12 P3	2B GENERAL PURPOSE REGISTER NO. 11 P3	2A PROGRAM COUNTER P3	29 INTERRUPT STATUS REGISTER P3	28 INTERRUPT MASK REGISTER P3
4	27 GENERAL PURPOSE REGISTER NO. 7 P3	26 PROGRAM COUNTER P2	25 INTERRUPT STATUS REGISTER P2	24 INTERRUPT MASK REGISTER P2	23 INTERRUPT FLAG REGISTER	22 PROGRAM COUNTER P1	21 INTERRUPT STATUS REGISTER P1	20 INTERRUPT MASK REGISTER P1
3	1F UTILITY NO. 3	1E UTILITY NO. 2	1D ASSEMBLY STATUS REGISTER	1C CHANNEL COMMAND REGISTER I	1B CHANNEL COMMAND REGISTER II	1A CHANNEL ADDRESS REGISTER	19 RDM/WRM	18 PROCESSOR UTILITY NO. 8
			← I/O CHANNEL REGISTERS - SELECTOR NO. 1 →					
2	17 UTILITY NO. 3 A/SR	16 UTILITY NO. 2 CAR-MUX INIT.	15 STATUS REGISTER	14 CHANNEL COMMAND REGISTER I	13 CHANNEL COMMAND REGISTER II	12 CHANNEL ADDRESS REGISTER	11 UTILITY NO. 1 CCR2-MUX INIT.	10 PROCESSOR UTILITY NO. 7 CCR1-MUX INIT.
			← I/O CHANNEL REGISTERS - MULTIPLEXOR TERMINATION →					
1	0F GENERAL PURPOSE REGISTER NO. 15 (WEIGHT) P4	0E PROGRAM COUNTER P4	0D INTERRUPT STATUS REGISTER P4	0C INTERRUPT MASK REGISTER P4	0B GENERAL PURPOSE REGISTER NO. 11 P4	0A GENERAL PURPOSE REGISTER NO. 10 P4	09 GENERAL PURPOSE REGISTER NO. 9 P4	08 GENERAL PURPOSE REGISTER NO. 8 P4
0	07 D2A	06 D1A	05 PROCESSOR UTILITY NO. 6	04 PROCESSOR UTILITY NO. 5	03 PROCESSOR UTILITY NO. 4	02 PROCESSOR UTILITY NO. 3	01 PROCESSOR UTILITY NO. 2	00 PROCESSOR UTILITY NO. 1

NUMBER IN UPPER LEFT-HAND CORNER IS HEXADECIMAL ADDRESS

SECTION TWO

INSTALLATION

2.1 SET-UP INSTRUCTIONS

Perform the following checks and procedures prior to the installation of a Spectra 70/55 Processor System at a field site.

1. Check the site temperature and humidity to determine that they are as specified in the Spectra 70 Installation Planning Guide (70-00-011).

2. Check to determine that adequate power lines have been provided and that no other equipment is connected to the lines; connection of other equipment to the lines could interfere with system performance.

3. Mark the main circuit breakers and power switches for the power lines to indicate which breaker and switch supplies power to what device.

4. Examine the areas beneath the raised flooring for obstructions in the cable runs.

5. Ensure that openings in the raised flooring are adequate for cable access.

6. Ensure that the customer is completely aware of the weight of the equipment and that the strength of the raised flooring is adequate; equipment weight and other important factors are specified in the Spectra 70 Installation Planning Guide.

7. Check that the floor is correctly marked for the location of each rack and cutouts are provided in the floor as detailed on Installation Plan 3630059.

8. Check that the flooring has been prepared to receive the Bus Bar Assembly.

2.2 INSTALLATION INSTRUCTIONS (BUS BAR ASSEMBLY)

The complete assembly is shipped disassembled into three separate items (two short, horizontal arms and one long, vertical arm) that must be joined at the site. (See RCA Drawing 3630172 and Figure 2-1.)

Each of the three items consists of two pre-assembled bus bars, connectors, and cables. The bars and cable connectors are encased in metal ducts. The cables, which are pre-connected to the bars, extend through grommets in the duct walls ready for connection to the individual racks.

Install and join the three arm assemblies in the following sequence:

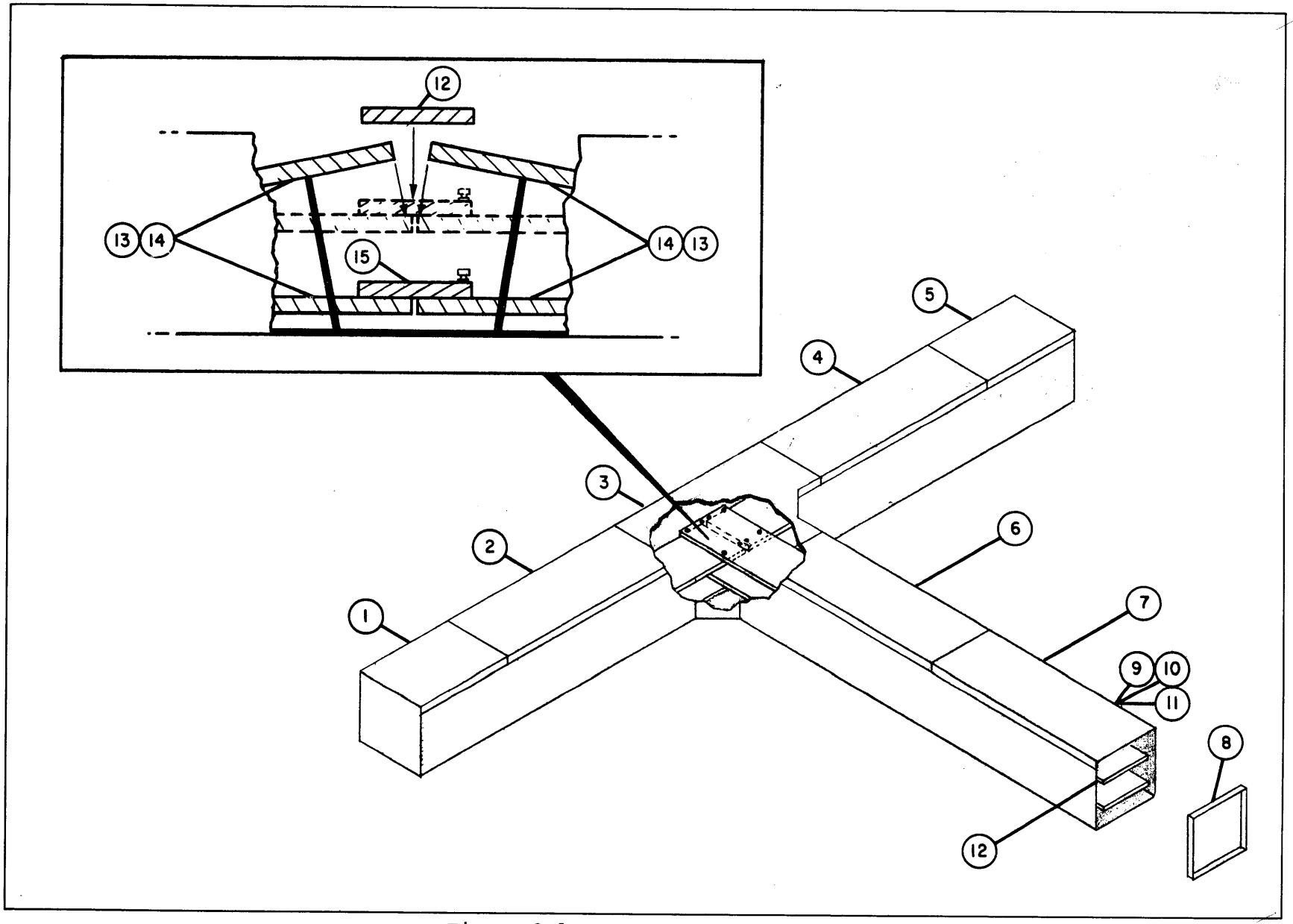


Figure 2-1. Bus Bar Assembly

NOTE: Remove the top covers of the ducts (Items 1 through 7 in Figure 2-1), and the end wall (Item 8) of the vertical arm before lowering the arm assemblies into the flooring.

1. Lower the vertical arm into the flooring.

2. Disconnect the cables (Items 9, 10, and 11) from the top bus bar (Item 12) of the vertical arm.

3. Lower the two horizontal arms, one at a time, into the flooring at right angles to the vertical arm.

4. Slide each horizontal arm toward the vertical arm until both top and bottom bus bars (Items 13 and 14) are underneath the top and bottom bus bars (Items 12 and 15) of the vertical arm.

5. Slide the top bus bar of the vertical arm backward, on its insulators, approximately 12 inches.

6. Prop up both top horizontal bars to expose the bottom three bars (two horizontal and one vertical).

7. Align the three bottom bars in T-formation and apply joint compound (RCA Drawing 3681897-1) to the joining surfaces of the bars; insert and tighten the eight socket head holding screws to lock the bars in position.

8. Remove the props and lower the top horizontal bus bars into position.

9. Slide the top vertical bus bar forward until the end is over, and aligned with, the horizontal bars.

10. Apply the joint compound, as in Step 7, and insert and tighten the eight socket head holding screws, which locks the complete assembly in T-formation.

11. Connect the three cables that were disconnected at the beginning of the procedure.

12. Replace the end wall in the vertical arm; invert the end wall when replacing it in the duct for easier insertion.

13. Replace the remaining duct covers and fasten them securely.

2.3 INSTALLATION INSTRUCTIONS (MECHANICAL)

Install the system according to the preferred layout (see RCA Drawing 3630182 and Figure 2-2.)

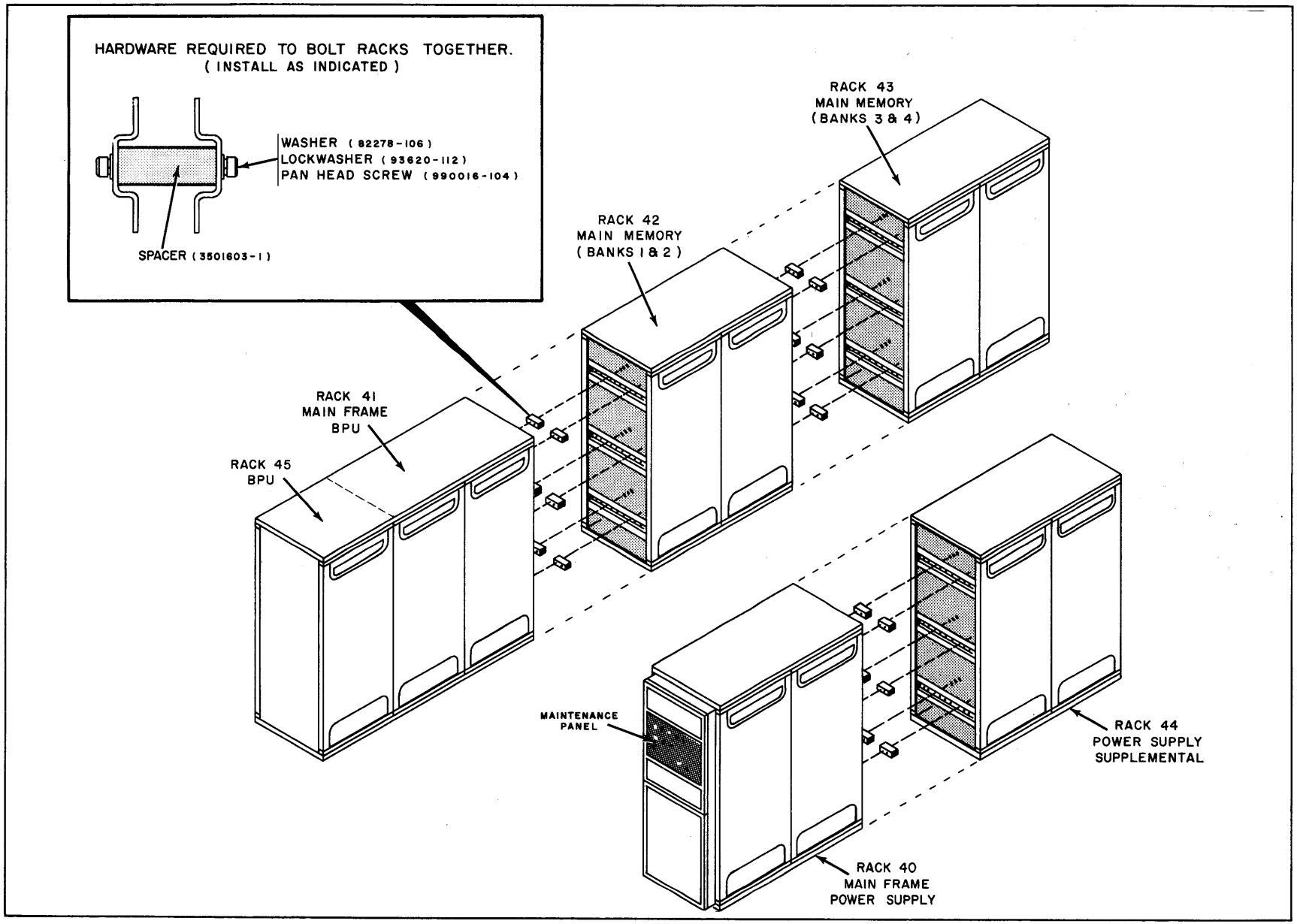


Figure 2-2. Bolting Racks Together

NOTE: Depending on the type of raised flooring, it is sometimes desirable to run the cables under the floor before replacing the racks in their designated locations. This should only be done, however, if sufficient room is available to place the cable ends underneath the flooring before placing the racks.

1. Remove the racks from the pallets and position them in the designated floor locations.

2. Following placement of the racks, check the front and top of each rack for uniform alignment.

3. If leveling is needed for top alignment, adjust the Scrujacks in each rack until the bottom of the frame is 1/4 inch from the floor.

4. Bolt the racks together according to Figure 2-2; it is necessary that all blocks be installed and tightened securely.

5. Check the vertical position (height) of all rack doors; doors must close without binding at top or bottom; if necessary, raise or lower a door by turning the hinge pin counterclockwise or clockwise. (See Figure 2-3.)

6. Check all rack doors for sag; if necessary, adjust by loosening the hinge bracket screws and repositioning the bracket. (See Figure 2-3.)

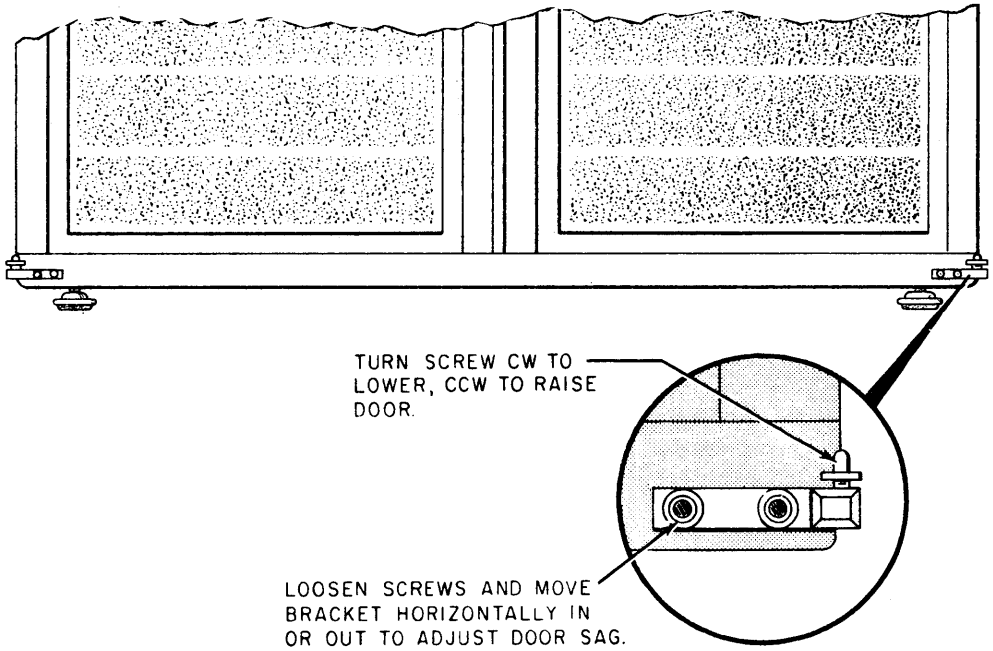


Figure 2-3. Adjusting the Rack Doors

2.4 INSTALLATION INSTRUCTIONS (ELECTRICAL)

Electrical installation of the system consists of power supply-to-rack cabling and inter-rack cabling (rack-to-rack and inter-rack), and final pre-operational check and tests.

2.4.1 POWER SUPPLY-TO-RACK(s) CABLING

Two power supply sources, Rack 40 (Main Frame) and Rack 44 (Supplemental), are provided, with cables, in the system. The cables must be connected to Racks 41, 42, 43, and 45 as shown in Figure 2-4 and as in Table 2-1.

DC power is brought into the system under the floor from the power supply, and attaches to the DC distribution blocks located near the floor level in the front and center of the racks. The distribution blocks are wired to the voltage buses located in the four corners and in the center behind the fixed-platter section. AC/DC power is brought into the processor through an MS Type 32-7 connector (J103) located below the fixed-platter section. The AC power supplies the fans and the convenience outlets. The MS connector also handles the processor thermostat signals and other miscellaneous signals related to power.

The platters are connected to the voltage buses by short jumpers from the voltage buses to the platters. The voltage levels are marked on the voltage bus and on the platters.

Initial cable connections must be made as shown in Figure 2-4 and must be made in the following sequence. (Ensure that cables connected to J103 of of Racks 41, 42, 43, and 45 are keyed as shown in Table 2-2.)

Initial Cabling Sequence

1. Check the -5V and Gnd. wires of the Bus Bar Assembly with an ohmmeter to determine whether they are correctly labeled. Perform the check as follows:

   a. In sequence, connect the leads of the ohmmeter between each of the -5V wires; resistance must be near Zero if the wires are correctly labeled.

   b. In sequence, connect the ohmmeter between each of the Gnd. wires; resistance must be near Zero if the wires are correctly labeled.

   c. In sequence, connect the ohmmeter between each of the -5V and Gnd.wires; resistance must be at Infinity if the wires are correctly labeled.

   d. Place correct labels on any mislabeled wires; cables should be clamped with clamps where provided so that fire shield covers can be installed.

2. Connect the -5V and Gnd. Bus Bar Assembly wires to the DC Distribution Block A and B in Rack 41.

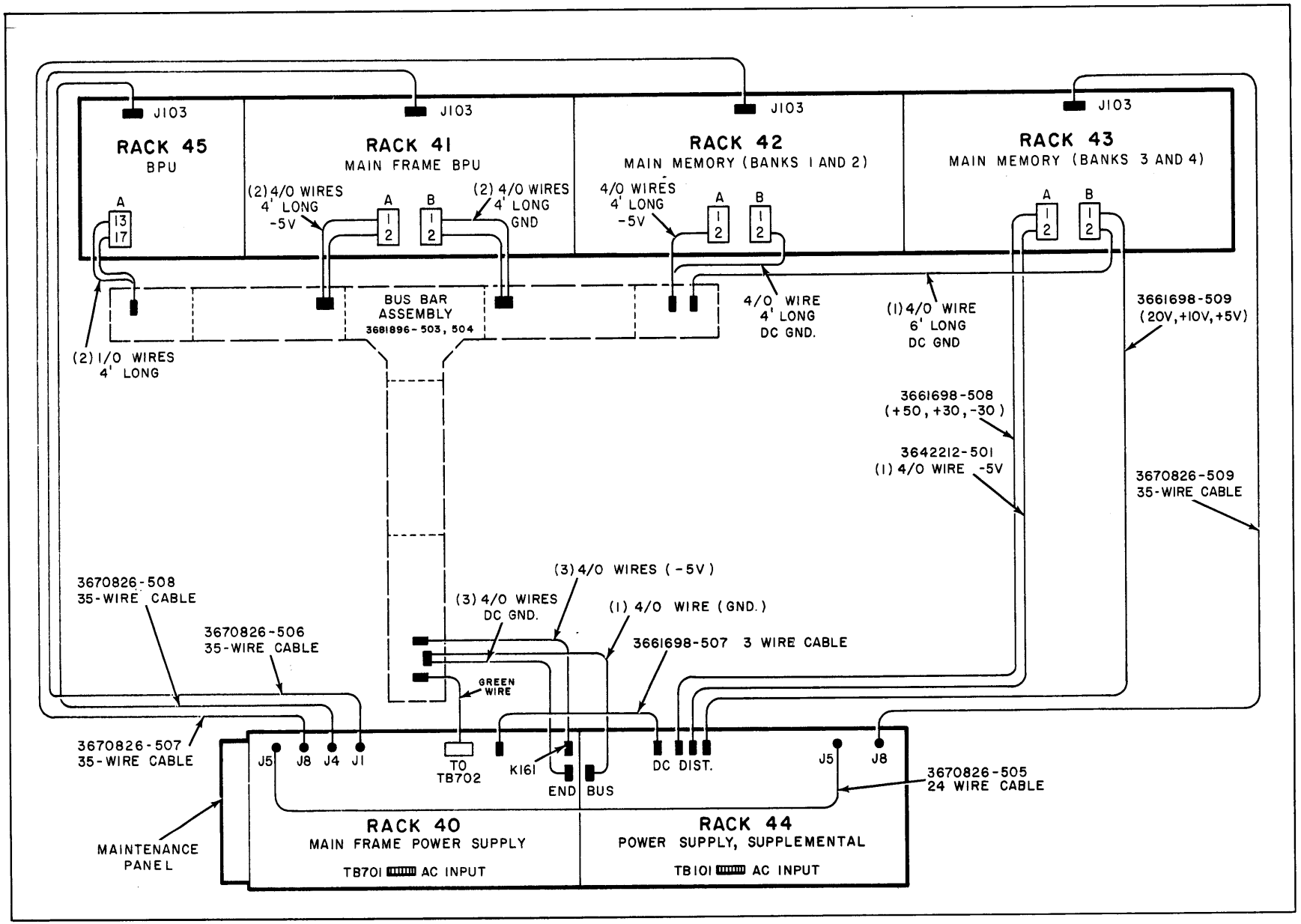


Figure 2-4. Power Supply to Main Frame Cabling

Table 2-1. Cable Routing Schedule

From	Cable	To
Maintenance Panel J4	3661495-505	BPU-J40 Rk. 41
Maintenance Panel J3	3661495-505	BPU-J53 Rk. 41
Maintenance Panel J2	3505444-505	Memory J14 Rk. 42
Maintenance Panel J5	3661495-505	BPU-J52 Rk. 41
Maintenance Panel J6	3661495-505	BPU-J44 Rk. 41
Maintenance Panel J7	3661495-505	BPU-J37 Rk. 41
Maintenance Panel J8	3505444-505	Memory J13 Rk. 42
Operator Console J2	3662104-501	BPU-J46 Rk. 41
Control Electronics	3661495-505	BPU-J49 Rk. 41
Operator Console J1	3661378-501	Maintenance Panel J1
Power Supply J1 Rk. 40	3670826-506	BPU-J103 Rk. 41
Power Supply J8 Rk. 40	3670826-507	Memory J103 Rk. 42
Power Supply J4 Rk. 40	3670826-508	BPU-J103 Rk. 45
Power Supply J8 Rk. 44	~~3670826-509~~	Memory J103 Rk. 43
Power Supply J5 Rk. 40	~~3670826-505~~	Supplemental P.S. J5 Rk. 44
Power Supply K158-B2,K158-A2, K160-A2 Rk. 40	3661698-501	BPU +50,+30,-30V Rk. 41
Power Supply K159-B2,K159-A2, K160-B2 Rk. 40	3661698-502	BPU +20,+10,+5V Rk. 41
Power Supply K158-B2,K158-A2, K160-A2 Rk. 40	3661698-503	Memory +50,+30,-30V Rk. 42
Power Supply K159-B2,K159-A2, K160-B2 Rk. 40	3661698-504	Memory +20,+10,+5V Rk. 42
Power Supply K158-B2,K158-A2, K160-A2 Rk. 40	3661698-505	BPU +50,+30,-30V Rk. 45
Power Supply K159-B2,K159-A2, K160-A2 Rk. 40	3661698-506	BPU +20,+10,+5V Rk. 45
Pwr.Sup. DC Grd.-5 Bus Rk.40	3681896-501	Rk.41,42,45 -Gnd.-5V
Power Supply K158-A1,K159-B1, K160-B1 Rk. 40	~~3661698-507~~	Power Supply K158-A2,K159-B2, K160-B2 Rk. 44
Power Supply K158-B1,K158-A1, K160-A1 Rk. 44	~~3661698-508~~	Memory +50,+30,-30 Rk. 43
Power Supply K159-B1,K158-A1, K160-B1 Rk. 44	~~3661698-509~~	Memory +20,+10,+5 Rk. 43
Power Supply TB702 Rk. 40	3671077-502	BPU-E1 Rk. 41
Power Supply TB702 Rk. 40	3671077-502	BPU-E1 Rk. 45
Power Supply TB702 Rk. 40	3671077-502	Memory E1 Rk. 42
Power Supply TB702 Rk. 40	3671077-504	Operators Console E4
Power Supply TB103 Rk. 44	~~3671077-502~~	Memory E1 Rk. 43
Power Supply K161-A1 Rk. 44	~~3642212-501~~	Memory -5V Rk. 43

Table 2-2. Cable Keys

From	To	Cable Drawing	Cable Key	J103 Key
Rack 40	Rack 41	3670826-506	Normal	Normal
Rack 40	Rack 42	3670826-507	W	W
Rack 40	Rack 45	3670826-508	X	X
Rack 44	Rack 43	3670826-509	Z	Z
Rack 44	Rack 40	3670826-505	Normal	Normal

Drähte vom MP → BS CE klemmleiste

3. Connect the two -5V and two Gnd. Bus Bar Assembly wires to Distribution Block A in Rack 45. ✓

4. Connect the two -5V and Gnd. Bus Bar Assembly wires to Distribution Blocks A and B in Rack 42; connect the six-foot DC Ground wire to Distribution Block B in Rack 43. ✓

> NOTE: In systems which do not have a Rack 43 and Rack 44 the connectors at the ends of the six foot ground wires must be taped heavily, then left under the raised floor. ✓

5. Connect the three -5V Bus Bar Assembly wires to K161 in Rack 40.

6. Connect the six-foot Ground wire of the Bus Bar Assembly to the Ground Bus in Rack 44. See note under step 4.

7. Connect the three Ground wires of the Bus Bar Assembly to the Ground Bus in Rack 40. ✓

8. Connect the green wire of the Bus Bar Assembly to TB702 in Rack 40. ✓

9. Connect J1 in Rack 40 to J103 in Rack 41, and J4 in Rack 40 to J103 in Rack 45. ✓

10. Connect J8 in Rack 40 to J103 in Rack 42, J5 in Rack 40 to J5 in Rack 44, and J8 in Rack 44 to J103 in Rack 43. ✓

11. Connect the jumper cable (RCA Dwg. 3661698-507) between Rack 40 (K158-A1, K159-B1, K160-B1) and Rack 44 (K158-A2, K159-B2, K160-B2).

12. Connect the remaining cables according to Table 2-1 (Maintenance Panel, Operator Console, Control Electronics, and remaining power supply cables); do not connect AC power until all cabling is completed. ✓

2.4.2 DRESSING AND TYING CABLES

Dress the cables when Maintenance Panel-to-Rack cabling is completed. All system cables should be positioned outside of the harness cables to prevent interference in closing the hinged frame.

2.4.3 POWER SUPPLY CHECK AND TEST

Connect the AC power cables to TB701 in Rack 40 and TB101 in Rack 44 after all power supply cables have been connected to Racks 41, 42, 43, and 45; clamp cables, where provided, and install all fire shield covers.

Check the power supply as follows:

1. Place the site circuit breaker, or breakers, and the power supply (AC) circuit breakers in both racks in the ON position, all fans in both racks should be operating.

2. Press the MASTER switches on both the Maintenance Panel (Rack 40) and Operating Console.

3. Press the TEST switch on the Control Panel (Rack 40).

4. Press the LAMP CHECK switch on the Maintenance Panel and Rack 40 and Rack 44 Control Panels; all lamps should light at each location.

5. Check all DC voltages with a precision voltmeter (1%) at the inputs to K158 through K162 in both racks.

6. If all DC voltage levels are approximately right, press the POWER OFF switch.

7. Repeat Steps 1 through 6 (except Step 3) for Rack 44.

8. Press the POWER ON switch and check the ramp-up in both racks with the precision voltmeter and the rotary switch on each Control Panel.

9. With power on, each voltage should ramp-up in 10 to 15 seconds in each rack.

If difficulty is encountered during the test, refer to Section 8, Power Supply, for possible remedial steps.

2.4.4 INTER-RACK CABLING (HARNESS/PLATTER ASSEMBLIES)

CAUTION

DO NOT attempt to insert internal cabling in the racks without first making certain that the Site AC circuit breaker (or breakers, if two are installed) is in the OFF position.

2.4.4.1 Harness Cables

Three types of harness cables are supplied with the system. They are: harnesses that carry signals between platters and the 75-pin connectors; harnesses that carry signals between platters; and harnesses that carry signals between platters in different racks without going under the floor. The harnesses that interconnect platters are of twisted triplet wire (RCA Drawing 8541633-1). The harnesses attached to the 75-pin connectors are twisted pair wires (RCA Dwg. 8541634-1). When the twisted pair is used, the red wire is the signal wire and the yellow wire is used for ground. When the twisted triplet is used, the red wire is the signal wire and the yellow and white wires are terminated in the same crimp and connected to ground. In some cases, however, the yellow wire is used for a signal that is the complement of the signal on the red wire.

2.4.4.2 Harness Connectors

Two types of harness connectors are used. The Interface, 75-pin, connectors (RCA Dwg. 8542395) are located at the bottom of the 48-inch rack and along the ends and bottom of the 24-inch rack. The harness connectors that are a part of the platter are RCA Dwg. 8549008, which mate with the harness board (RCA Dwg. 3671419-501).

2.4.5 INTER-RACK CABLE CONNECTIONS

All internal cable connections, with the exception of Cables 72, 73, 74, 75, 101, and 102, were factory-installed. Cables 72, 73, 74, 75, 101, and 102 must be connected at the site between Racks 42 and 43. Connect the cables according to RCA Dwg. 3683321 and Table 2-3. Table 2-3 lists the routing drawing numbers. These drawings contain the platter and connector locations and sketches indicating the cable routing.

2.4.6 PLATTERS

Platters incorporated in the 70/55 H system are multi-layered circuit boards. The platter concept reduces the number of backpanel wiring errors and makes possible the replacement of important segments of a processor.

Generally, signal-connecting wires are printed on the two surface planes of the platter. The wires are printed horizontally on one plane and vertically on the opposite plane. The three or four internal copper planes of the platter are used for voltage distribution and signal ground.

In addition to the circuit wiring, the platter assembly (Figure 2-5) also contains:

1. Plug-in receptacles for logic plug-ins (RCA Dwg. 8549008).

2. Modules containing circuit terminating resistors.

3. Cable connectors for inter-platter and inter-rack cabling.

4. Terminal connectors for wiring to voltage buses.

Harness connectors, TR modules, and plug-in receptacle locations can be expressed by a five-character code (Figure 2-5). The first three characters (001 to 015) is a row number, the second character is A or B designating a platter zone and the third character shows the column (A to Z). These codes are silk-screened on the platters.

A pin location can be found in one of two ways, by Alpha-numeric notation or by X and Y coordinates.

1. Alpha-numeric notation: first locate the connector or receptacle, as shown in the previous paragraph, then locate the pin number of that connector. (See Figure 2-6a.) This numbering is common to harness connectors and plug-in connectors.

Table 2-3. 70/55 Cable/Harness Drawings

Cable No.	Assembly Drawing	Routing Drawing	See Legend
1	3671600-501	3662526	B
2	3671601-501	3662527	B
3	3671602-501	3662520	B
4	3671603-501	3662525	B
5	3671604-501	3662527	B
6	3671605-501	3662517	B
7	3671606-501	3662518	B
8	3671607-501	3662516	B
9	3671608-501	3662517	B
10	3671609-501	3662520	B
11	3671610-501	3662527	B
12	3671611-501	3662527	B
13	3671612-501	3662518	B
14	3671613-501	3662517	B
15	3671614-501	3662518	B
16	3671615-501	3662527	B
17	3671616-501	3662521	B
18	3671617-501	3662518	B
19	3671618-501	3662516	B
20	3671619-501	3662514	B
21	3671620-501	3662518	B
22	3671621-501	3662522	B
23	3671622-501	3662521	B
24	3671623-501	3662515	B
25	3671624-501	3662522	B
26	3671625-501	3662520	B
27	3671626-501	3662515	B
28	3671627-501	3662522	B
29	3671628-501	3662515	B
30	3671629-501	3662523	B
31	3671630-501	3662518	B
32	3671631-501	3662520	B
33	3671632-501	3662518	B
34	3671633-501	3662517	B
35	3671634-501	3662515	B
36	3671635-501	3662522	B
37	3671636-501	3662515	B
38	3671637-501	3662516	B
39	3671638-501	3662520	B
40	3671639-501	3662523	B

Cable No.	Assembly Drawing	Routing Drawing	See Legend
41	3671640-501	3662525	B
42	3671641-501	3662519	B
43	3671642-501	3662523	B
44	-	-	-
45	-	-	-
46	3671645-501	3662524	B
47	3671646-501	3662519	B
48	3671647-501	3662523	B
49	3683275-501	3662517	B
50	3683275-502	3662515	B
51	3671649-501	3662519	B
52	3683276-501	3662514	B
53	3683276-502	3662518	B
54	3683276-503	3662518	B
55	3683275-503	3662524	B
56	3683275-504	3662519	B
57	3683217-501	3662515	B
58	3671649-502	3662524	B
59	3683276-504	3662518	B
60	3683275-505	3662518	B
61	3683275-506	3662523	B
62	3683276-505	3662518	B
63	3683275-507	3662514	B
64	3683217-502	3662514	B
65	3683217-503	3662519	B
66	3683217-504	3662524	B
67	3683275-508	3662514	B
68	3683275-509	3662523	B
69	3683275-510	3662514	B
70	3683275-511	3662519	B
71	3683275-512	3662525	B
72 *	3683277-501	3662534	B
73 *	3683277-502	3662534	B
74 *	3683277-503	3662534	B
75 *	3683278-501	3662534	B
76	3683218-501	3662530	B
77	3671654-501	3662530	B
78	3683277-504	3662530	B
79	3671655-501	3662531	B
80	3683218-502	3662531	B

Table 2-3. 70/55 Cable/Harness Drawings (Cont'd.)

Cable No.	Assembly Drawing	Routing Drawing	See Legend
81	3683218-503	3662531	B
82	3683277-505	3662531	B
83	3683277-506	3662531	B
84	3683218-504	3662532	B
85	3671656-501	3662532	B
86	3683277-507	3662532	B
87	3671657-501	3662532	B
88	3683277-508	3662533	B
89	3683277-509	3662533	B
90	3683278-502	3662090	B
91	3683277-510	3662090	B
92	3671658-501	3662090	B
93	3683278-503	3662090	B
94	3683278-504	3662091	O
95	3683278-505	3662091	O
96	3683278-506	3662091	O
97	3683277-511	3662091	O
98	3683218-505	3662087	B
99	3671649-503	3662087	B
100	3683217-505	3662087	B
101*	3683279-501	3662524	B
102*	3671660-501	3662520	B
103	3671661-501	3662527	B
104	3671662-501	3662528	B
105	-	-	-
106	3671663-501	3662528	B
107	3671663-502	3662528	B
108	3683219-501	3662528	B
109	3671665-501	3662529	B
110	3671666-501	3662529	B
111	3683219-502	3662529	B
112	3683219-503	3662529	B
113	3671666-502	3662530	B
114	3683280-501	3662098	24"B
115	3683281-501	3662098	24"O
116	3683281-502	3662098	24"O
117	3683280-502	3662098	24"O
118	3671669-501	3662099	24"O
119	3683281-503	3662099	24"O
120	3683282-501	3662098	24"O
121	3683280-503	3662098	24"B
122	3683280-504	3662099	24"O
123	3683281-504	3662099	24"O
124	3683282-502	3662098	24"O
125	3683280-505	3662098	24"O
126	3683280-506	3662099	24"O
127	3683281-505	3662099	24"O
128	3683282-503	3662099	24"O
129	3683280-507	3662099	24"O
130	3671671-501	3662092	B
131	3671672-501	3662092	B
132	3671673-501	3662092	B
133	3671674-501	3662093	B
134	3671674-502	3662093	B
135	3671675-501	3662093	B
136	3671676-501	3662092	m2
137	3671677-501	3662092	m2
138	3671678-501	3662092	m2
139	3671679-501	3662093	m2
140	3671679-502	3662093	m2
141	3671680-501	3662093	m2
142	3683221-501	3662094	m2
143	3683221-502	3662095	m3,4
144	3683221-503	3662095	m3,4
145	-	-	-
146	-	-	-
147	-	-	-
148	3671684-501	3662096	m3,4
149	3671685-501	3662096	m3,4
150	3671686-501	3662096	m3,4
151	3671687-501	3662097	m3,4
152	3671687-502	3662097	m3,4
153	3671688-501	3662097	m3,4
154	3671689-501	3662096	m3,4
155	3671690-501	3662096	m3,4
156	3671691-501	3662096	m3,4
157	3671692-501	3662097	m3,4
158	3671692-502	3662097	m3,4
159	3671693-501	3662097	m3,4
160	3682995-501	3662087	B

Table 2-3. 70/55 Cable/Harness Drawings (Cont'd.)

Cable No.	Assembly Drawing	Routing Drawing	See Legend
161	3682993-501	3662087	B
162	3682994-501	3662087	B
163	3671697-501	3662087	B
164	3682995-502	3662087	B
165	3682993-502	3662086	B
166	3682993-503	3662086	B
167	3682995-503	3662086	B
168	3682995-504	3662086	B
169	3682993-504	3662088	B
170	3682994-502	3662088	B
171	3682995-505	3662088	B
172	3682993-505	3662088	B
173	3682993-506	3662088	B
174	3682993-507	3682089	B
175	3682995-506	3662089	B
176	3682994-503	3662089	B
177	3682993-508	3662089	B
178	3682995-507	3662089	B
179	3682995-508	3662089	B
180	3683335-501	3662098	O
181	3683281-506	3662098	O
182	3683281-507	3662099	O
183	3683335-502	3662099	O
184	3683335-503	3662098	O
185	3683281-508	3662099	O

* These cables are not factory-installed and must be connected at the site installation.

LEGEND:

B = Basic System
O = Optional
24" = Rack 45
m2 = Second Memory Bank
m3 = Third Memory Bank
m4 = Fourth Memory Bank

Table 2-4. Platter Drawings

Platter	Revision Level Control	Assembly Parts List
MP A/55	3681800	3681694
SEL A1A/55	3681801	3681691
SEL A2A/55	3681802	3681692
SEL B1A/55	3681803	3681693
INT 9IA/55	3681804	3681695-501
INT 9IA/55	3681804	3681695-502
MM 4CA/55	3681805	3682276
MM 5CA/55	3681806	3682275
MM 3CA/55	3681807	3682277
FM A/55	3681808	3681141
BPU 1CA/55	3681809	3682279
BPU 2CA/55	3681810	3682280
BPU 3CA/55	3681811	3682281
BPU 4CA/55	3681812	3682282
BPU 5CA/55	3681813	3682283
BPU 6CA/55	3681814	3682284
BPU 7CA/55	3681815	3682285
BPU 8CA/55	3681816	3682286
BPU 9CA/55	3681817	3682287
BPU 1BA/55	3681818	3682288
BPU 1DA/55	3681819	3682289
BPU 1MA/55	3681820	3682278
BPU 2DA/55	3681821	3682290
BPU 2MA/55	3681822	3682291
DC/55	3681625	3682303
MM1SL/55	3682986	3682992
MM1SR/55	3682987	3682991

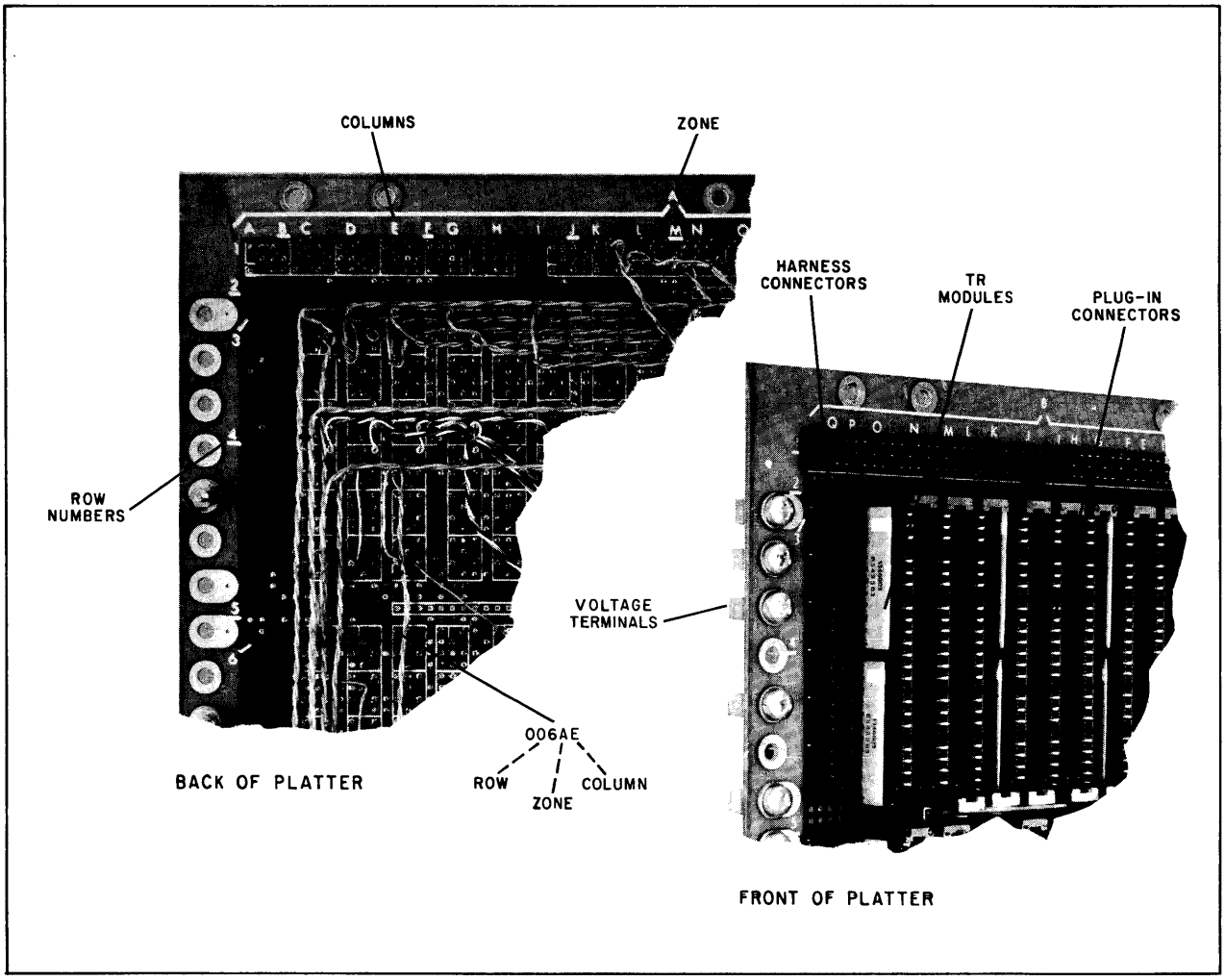


Figure 2-5. Platter Details

2. X and Y coordinates: pins can be designated by two three-digit numbers. The first number (X coordinate) shows the count across the platter. Pin 001 is in the upper left corner of the wiring side. The second three-digit number (Y coordinate) shows the pin count-down from the top.

2.4.6.1 Platter Locations

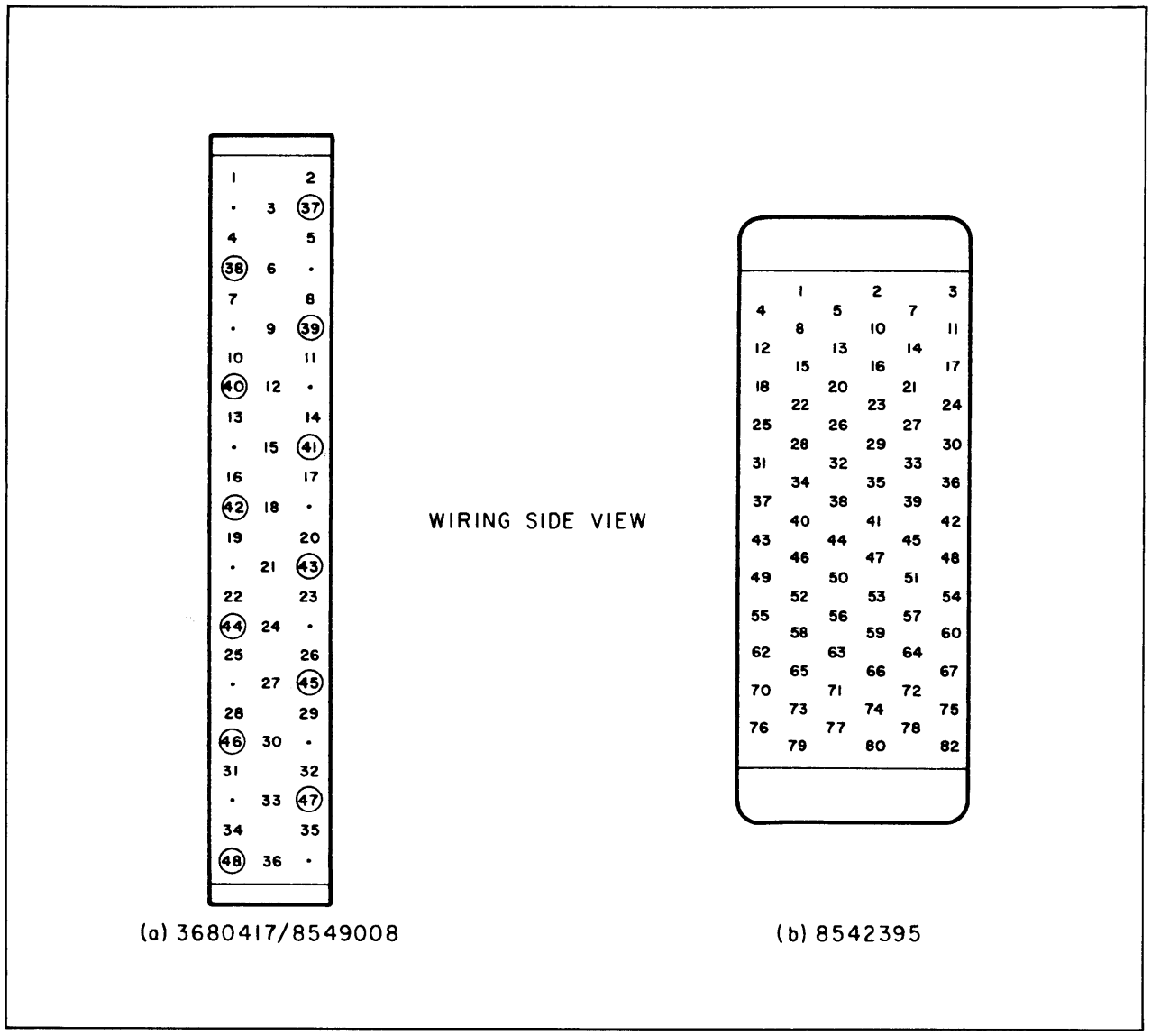
Figure 2-7 shows the platter locations in the 70/55 H system.

2.4.6.2 Platter Drawings

Table 2-4 lists the platter drawings used in the 70/55 H Processor; Figure 2-8 illustrates a typical platter layout.

2.4.7 PLATTER SIGNAL DISTRIBUTION

Signals enter and leave each platter only through the harness connectors. The signals are then distributed to the various plug-in logic connectors by means of the platter printed circuits. The logic connectors in turn connect



(a) 3680417/8549008 (b) 8542395

Figure 2-6. Connector Pin Numbering

to the plug-in boards with the logic circuits. In cases where the conductor density exceeds that available in the platter, signals are carried by discrete point-to-point wiring. This wiring is either single wire (orange), twisted pair (blu/yel), or twisted triplet (blk, blu/wht), and is terminated by wire wrap to the connector pins.

The discrete wire schedule is called out on the assembly drawing of each platter. For convenience, these drawings are listed in Table 2-4. The schedule gives the sequence of installation, the wire wrap (DA3 is orange A wire, PA4/PA6 is twisted triplet blk/blu/wht TTA wire), the terminations, the turn pins, the wire length, and the signal name. (The turn pin gives the routing of the wire; from the first termination, the wire is brought to the first turn pin in a straight run then is bent around the turn pin and run straight to the next turn pin, and so on to the final termination.)

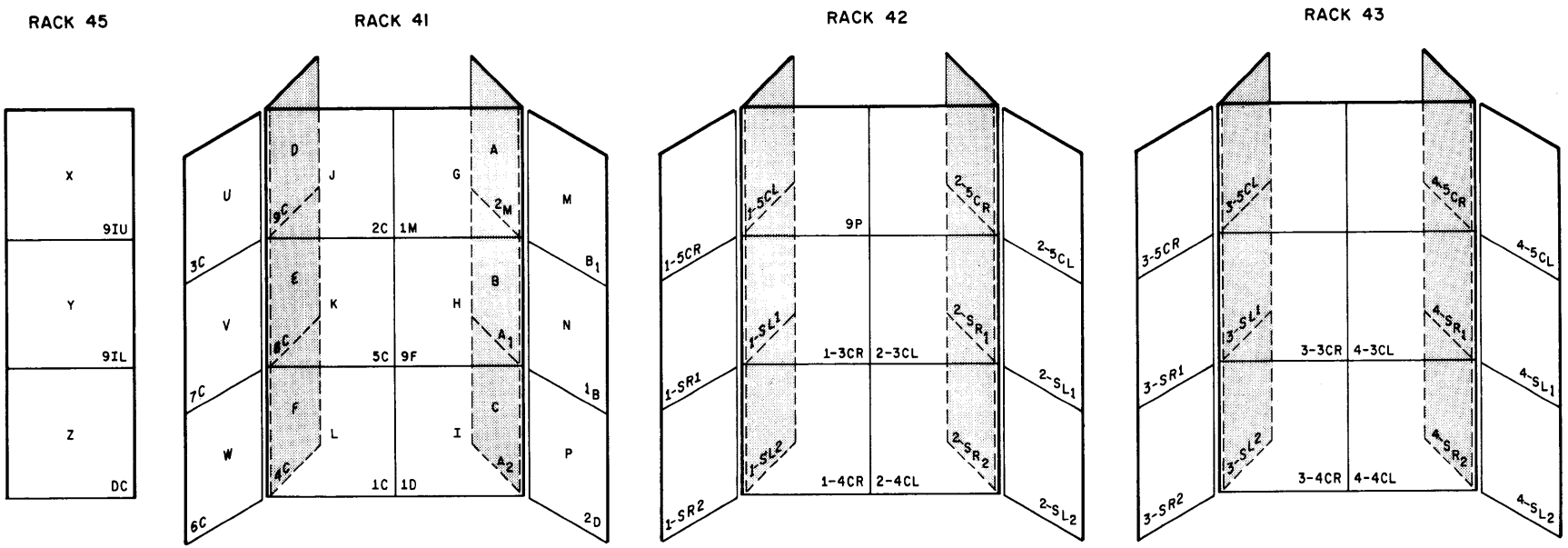


Figure 2-7. 70/55 Platter Locations

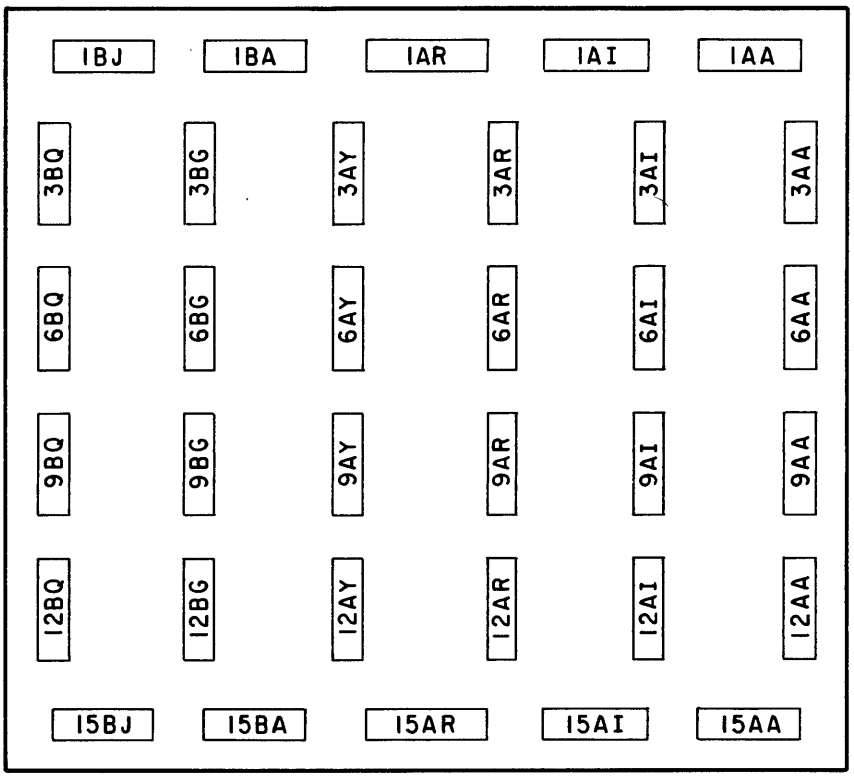


Figure 2-8. Typical Platter Connector Layout (Plug-in Side)

2.4.8 INTERFACE CABLING

Interface cables are used for communication between the processor and other equipment and are supplied as part of the peripheral equipment. With the exception of one cable, attached to the 70/97 Operator's Console (Table 2-1), they are identical except for the termination clamps. The interface cables are attached to the 75-pin connectors contained in the processor. These connections are listed in Table 2-5.

2.5 SYSTEM CHECK

Perform a system check, after all cabling has been completed, in the following sequence.

2.5.1 FANS

1. Turn on power as directed in the power supply check procedure.

2. Check that all fans are operating properly in all racks; if a fan assembly needs replacing, make the replacement according to the procedure outlined in Section Four.

Table 2-5. 75-Pin Interface Connectors

Trunk	Right Angle Connector	Straight (180°) Connector	Features
MPXR 9	Rack 41 - J49		Standard
" 8	" 41 - J51		
" 7	" 41 - J48		
" 6	" 41 - J47		
" 5	" 41 - J45		
" 4	" 41 - J42		
" 3		Rack 45 - J8	
" 2		" 45 - J7	
" 1		" 45 - J6	
SEL1-1	Rack 41 - J41		5020
" 2		" 45 - J5	
" 3		" 45 - J4	
" 4	-	-	
SEL2-1	Rack 41 - J38		
" 2		Rack 45 - J3	
" 3		" 45 - J2	
" 4	-	-	
SEL3-1		Rack 45 - J16	
" 2		" 45 - J15	
" 3		" 45 - J1	
" 4	-	-	
SEL4-1		Rack 45 - J14	5022
" 2		" 45 - J13	
" 3	-	-	
" 4	-	-	
SEL5-1		Rack 45 - J12	
" 2		" 45 - J11	5024
" 3	-	-	
" 4	-	-	
SEL6-1	-	Rack 45 - J10	
" 2	-	" 45 - J9	
" 3	-	-	
" 4	-	-	
Direct Control 1		Rack 45 - J19	
2		" 45 - J20	
3		" 45 - J21	
4		" 45 - J22	
5		" 45 - J23	
6		" 45 - J24	

CAUTION

Remove all power from the system before attempting to remove or replace a fan assembly; remove AC power by placing the site circuit breakers in the OFF position.

Total heat dissipation is based on a 3-platter frame with the following conditions:

Gate dissipation - .122 watts average

Average dissipation/board 14 x .122 = 1.7 watts

Average dissipation/platter 80 x 1.7 = 136 watts

T.R. Module dissipation/platter 73 x .65 = 47.45 watts

Average dissipation/platter = 136 + 47.45 = 183.45 watts

Average dissipation, 3-platter frame - 183.45 x 3 - 550.35 watts

Temperature withing a 3-platter frame is maintained to a 20°F rise above the room ambient temperature.

2.5.2 FILTERS

The air through each platter-frame section of the memories is independently filtered by a nylon filter located at the bottom of each of the frame sections. Air for platter-frame sections of the BPU passes through nylon filters located at the bottom of each door. (See Figure 3-5 and 3-6.)

If necessary during system check, remove a memory filter by unlocking the slide fastener at each side of the tray assembly and pull the unit forward. In replacing the filter in the rack, slide the tray assembly into place slowly; do not disturb the adjacent harness assemblies.

2.5.3 TEMPERATURE THERMOSTATS

Check the operation of the high-temperature thermostats for five minutes with power on and fans operating. Make the check by observing the OHW Indicator on the Maintenance Panel and the HIGH TEMPERATURE WARNING light on the Control Panel of the power supply.

The thermostats, two in each platter-frame, are located in the air stream of the fans at the top of the frame and react to abnormally high temperatures in each frame. One thermostat lights the indicators when the temperature reaches 122 degrees F. The other cycles down DC power in the system when the temperature reaches 131 degrees F.

2.5.4 HEAT SINK FANS

With power on, observe that the heat sink fans are operating. A malfunction is indicated by one of the heat sink warning indicators on the Control Panel of the power supply.

2.5.5 OPERATING CONSOLE

Check the Operating Console. (Refer to the 70/97 Maintenance Manual for applicable procedures.)

2.5.6 MEMORIES

Check the memories. (Refer to Sections 5 and 6 for applicable procedures.)

2.5.7 SIGNAL CABLES

Check the input/output signals at the appropriate multiplexor or selector. (See Table 2-6 if it becomes necessary to determine the correct signal and pin assignment for the interface cable.)

2.5.8 INPUT/OUTPUT DEVICES

Check each input/output device, one at a time, to determine whether the processor is operating correctly.

2.5.9 T&M ROUTINES

Conclude the system check by running all T&M routines to ensure that the system is operating properly.

2.6 DRAWING TREE

Figure 2-9 illustrates the top MI and assembly drawings for the Spectra 70/55 H Processor System.

Table 2-6. Signal and Pin Assignment for I/O Interface Cable

Signal Name	Connector Pin No.		Logic Ref. Pin No.		Signal Name	Connector Pin No.		Logic Ref. Pin No.	
	H	L	H	L		H	L	H	L
DOUT 0	1	4	201	101	DIN 0	40	43	207	107
DOUT 1	2	5	401	301	DIN 1	41	44	407	307
DOUT 2	3	7	601	501	DIN 2	42	45	607	507
DOUT 3	8	12	202	102	DIN 3	46	49	208	108
DOUT 4	10	13	402	302	DIN 4	47	50	408	308
DOUT 5	11	14	602	502	DIN 5	48	51	608	508
DOUT 6	15	18	203	103	DIN 6	52	55	209	109
DOUT 7	16	20	403	303	DIN 7	53	56	409	309
DOUT 8	17	21	603	503	DIN 8	54	57	609	509
SPARE	22	25	204	104	SPARE	58	62	210	110
ACTIVATE	23	26	404	304	SERVICE REQ	59	63	410	310
SELECT	24	27	604	504	READY	60	64	610	510
TRAC	28	31	205	105	INTERRUPT	65	70	211	111
STROBE	29	32	405	305	END	66	71	411	311
TERMINATE	30	33	605	505	SPARE	67	72	611	511
SET INTERRUPT	34	37	206	106	DIP	73		212	
GENERAL RESET	35	38	406	306	GROUND		76		112
PROP	36		606		SPARE	74	77	412	312
GROUND		39		506	SPARE	75	78	612	512
					SPARE	79	80	213	413
					SHIELD (GRD)	82		613	

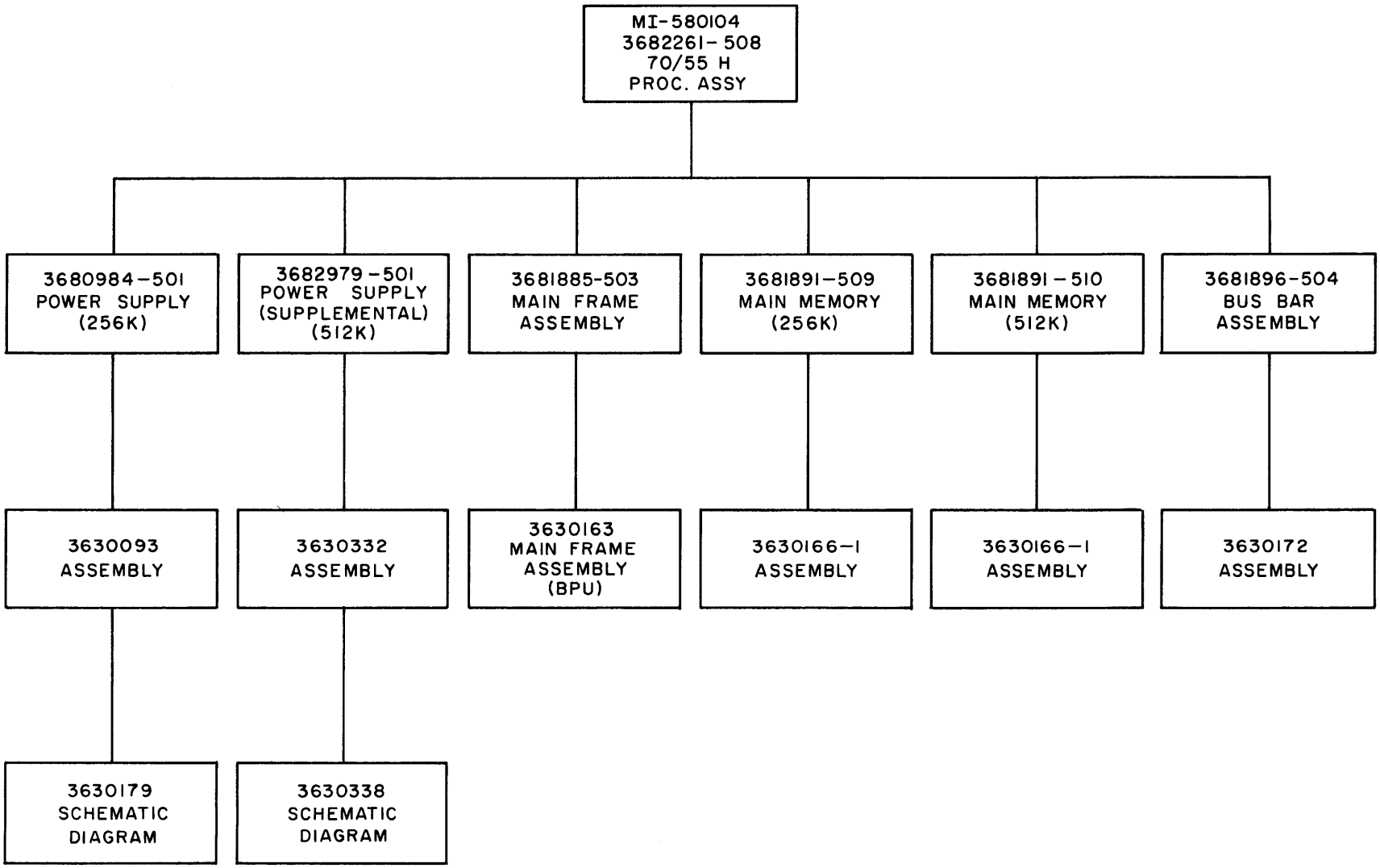


Figure 2-9. Top MI and Assembly Drawings

SECTION THREE

MAINTENANCE

3.1 PREVENTIVE MAINTENANCE

The preventive maintenance of the 70/55 Processor will vary from site to site depending on environmental conditions. Continued dependable performance can be achieved only by establishing and adhering to a fixed preventive maintenance routine. This section will outline a suggested base line from which site managers and/or maintenance personnel can develop a system of preventive maintenance which best fits the specific processor.

3.1.1 INITIAL PM PROCEDURES

After installation of the Processor, during the test phase, the following measurements must be made for future reference.

1. After reliable operation is achieved the actual power supply voltages at the outputs of the D.C. supplies should be measured and logged. The voltage readings may be greater than the rated outputs of the D.C. supplies. However, due to the high currents involved, voltage levels measured at the Power Supply rack will be higher than the voltage levels measured at the logic racks. When subsequent voltage checks are made this log can serve as a reference standard for the specific system.

2. The bias range of all memory banks must be noted for future reference. This chart should indicate the voltage setting when the particular memory bank starts dropping bits, and the voltage setting when the memory starts picking up bits. The Memory Address and Console Conditions can also be logged when the limits of the bias are reached. Measure and record the drive current settings. Later, if memory troubles occur, this chart will serve as a reference table. For preventive maintenance purposes, maintenance personnel should be sure that the bias range between the two limits is not narrowing.

3. Due to the different environmental conditions at various sites, the initial period should be used by maintenance personnel to determine the frequency for cleaning air filters in the system. In the suggested maintenance schedule that will follow, inspection and cleaning of air filters is listed with monthly procedures. This frequency should be adjusted according to need at the particular site.

3.1.2 REGULAR PM PROCEDURES

The procedure consists of two sections, a Schedule and a Task Outline. The Schedule lists the items to be done and the time required in minutes. The Task Outline presents a brief description of how the item is to be performed and the limits and/or references, if applicable. Note that the cycles are given in periods of 24, 120, 500, 3000, and 5000 operating hours.

SCHEDULE	TIME REQUIRED IN MINUTES		
		CSR	
	OPER	ON-LINE	OFF-LINE
Every 120 Hours of Operation			
A. CLEAN			
1. Outside of cabinets	15		
B. INSPECT			
1. Indicator lamps	5		
2. Check repaired plug-ins		15	
Every 500 Hours of Operation			
A. CLEAN			
1. Air Filters	10		
B. INSPECT			
1. Fans	2		
2. Bias range		30	
3. Drive currents		30	
C. RUN HARDWARE CHECK ROUTINES		10	
Every 1500 Hours of Operation			
A. INSPECT			
1. Power supply voltages		30	
Every 3000 Hours of Operation			
A. INSPECT			
1. Series pass transistors in the power supply		60	
2. Push-on contacts		15	

70/55 PREVENTIVE MAINTENANCE TASK OUTLINE

Every 120 Hours of Operation

A. CLEAN

1. Outside of cabinets -- Clean the cabinets with a damp cloth and Johnson's Upholstery Cleaner.

B. INSPECT

1. Indicator lamps -- Check lamps and replace as necessary.

2. Check repaired plug-ins -- All repaired plug-ins should be checked for satisfactory operation under actual operating conditions.

Every 500 Hours of Operation

A. CLEAN

1. Air Filters -- Clean air filters by washing in water. Spray with Handikoter CSC 932621.

B. INSPECT

1. Fans -- Check fans for air flow at all three platter sections.

2. Bias Range -- Bias Range should be checked against the chart suggested above. See 3.1.1, paragraph 2.

3. Drive currents -- Check voltage values and compare with standard range values recorded at initial operation (see above).

C. RUN HARDWARE CHECK ROUTINES -- Until hardware check routines are available, run a typical customer routine to insure acceptable operation of the processor.

Every 1500 Hours of Operation

A. INSPECT

1. Power supply voltages -- Check power supply voltages at the Processor racks and adjust if necessary. Refer to section 8.14.3 of this Maintenance Manual for adjustment procedures.

Every 3000 Hours of Operation

A. INSPECT

1. Series pass transistors in the power supply -- To check for faulty condition (open transistor) measure the DC voltage between the common emitter bus and the series emitter resistor for each transistor in turn. Particular attention should be given to the -5 volt supply which has 128 series pass transistors. Nominal readings range from .5V for the -5 volt supply to 2V for the +50 volt supply.

2. Push-on contacts -- Contacts used in the maintenance panel may become loose and fail to make contact. Loose contacts should be soldered, exercizing care not to overheat the contacts.

3.2 PLATTER REPAIRS

Before attempting platter repairs, some training is necessary. Some of the repair procedures outlined are exerpts from the RCA Repair Procedure Number 8401506 and EDP Service TIP, 70/System-12. These drawings will prove extremely helpful to the maintenance personnel.

3.2.1 BROKEN COPPER PATH

When a break in a copper wiring path is found, a wire wrap connection between two component pins can be added to complete the circuit. First, isolate the broken section by cutting the copper wiring path at the first component pins to each side of the break. Select locations for the cuts by referring to the platter layout drawing. Exact location is not critical but the cuts must be within two inches of the component pins.

Add a repair wire between the 2 pins. If the length is 2 inches or less, "A" type wire may be used, (3501328-2); if longer than 2 inches, use "TA" wire (3509745-1).

TA wire must not run parallel to another wire in the same channel for more than 4 inches. Alternate wire channels shall be used to meet this requirement. The TA ground wire must be terminated within 1.5 inches of its signal termination.

3.2.2 CUTTING A COPPER PATH

Considering the consequences of a damaged platter due to improper cutting techniques, it is mandatory that this procedure be followed without exception. The tool consists of a cutter (CSC 938199), held in a pin vise (CSC 938198). This tool is to be used for cutting printed circuit paths. Scribes, X-acto knives or other similar tools are <u>not</u> to be used for cutting printed circuit paths.

Before performing any cutting operation, double check to insure that the correct path is selected. If there is any doubt whatsoever, refrain from any cutting until the desired path is absolutely defined. The cutting procedure follows:

1. Insert the tool in the pin vise so that approximately one inch of the tool protrudes.

2. Straddle the circuit path with the tool as illustrated in Figure 3-1. If the path is not completely straddled, incomplete cutting will result. Using a light downward pressure, rotate the tool back and forth in a 180° arc across the circuit path. As the tool begins to cut through the protective coating, the bright copper of the circuit path will begin to show. As soon as the copper is cut through, a powder will begin to be produced. The cutting operation should then be ceased immediately.

CAUTION

A platter is a five layer printed board.
Cutting too deeply will result in damage to
other circuit paths.

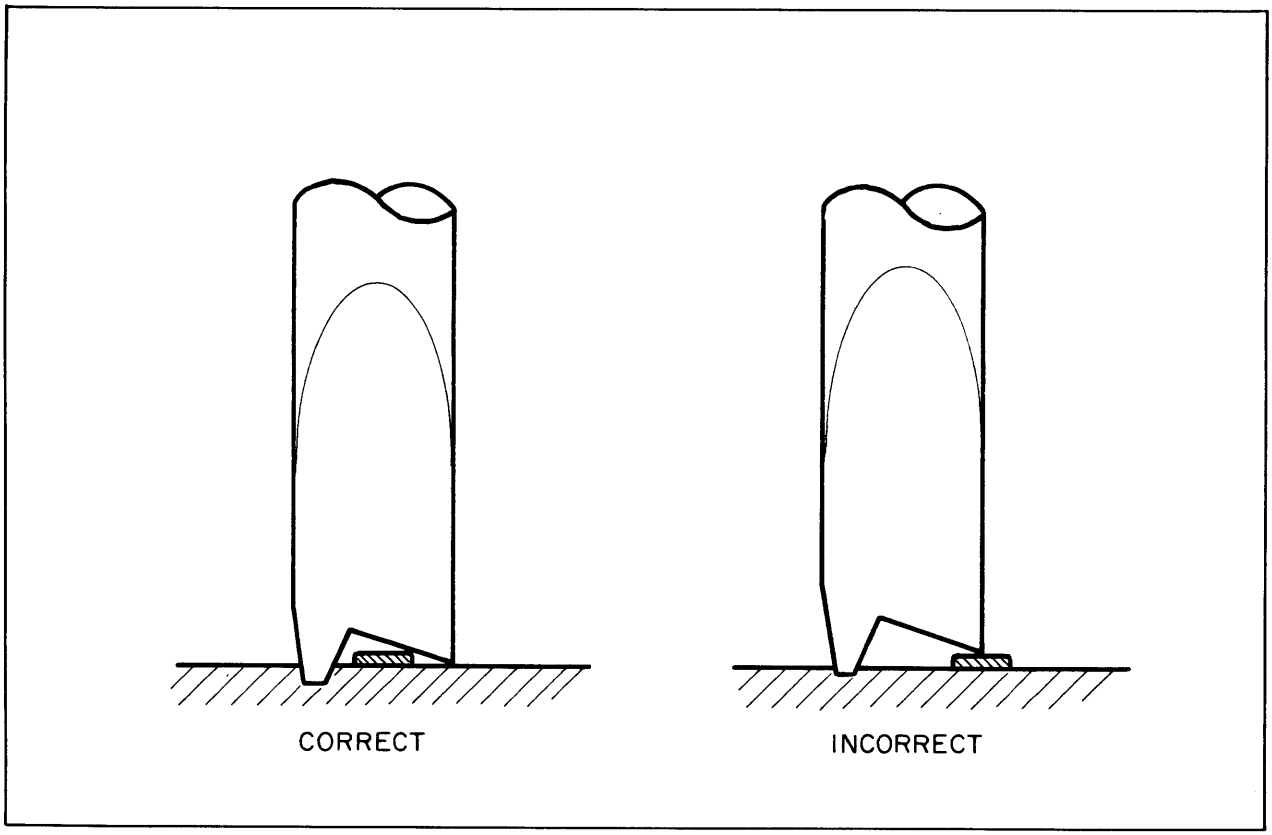


Figure 3-1. Cutting a Copper Path

3. Using a jeweler's loupe (CSC 937347), visually inspect the cut. A correct cut will appear as a semicircular hole across the printed circuit path. An incomplete cut will have some copper in the hole.

4. Perform a continuity check, between the appropriate points, with an ohmmeter in order to verify that an open circuit exists.

5. If an error is made and the wrong path is cut, no repairs are to be made to the cut. The open circuit should be bridged by using a discrete wire.

6. When attempting to cut one of two parallel paths that are extremely close together, the pivot should be outside of the path to be cut rather than between the two paths. This is to prevent damage to the adjacent path when the desired path is cut.

3.2.3 BROKEN CONNECTOR PIN

To replace a broken connector pin:

1. Snip the pin close to the platter surface with a pair of end cutting pliers (Drawing Number 3683293 or equivalent).

2. Using a low wattage soldering iron, place the soldering iron tip (Drawing Number 3683294 or equivalent) directly on the cut surface of the pin. Hold the iron perpendicular to the platter.

3. Apply pressure to the pin; as the solder melts, the pin can be pushed through the platter. Pressure required will be five to fifteen pounds.

4. Remove the pin with long nose pliers.

5. Remove excess solder from the hole using a 0.036 inch drill in a pin vise.

6. Insert a replacement pin of the same type in the connector. Do not attempt to seat the pin fully at this time. Carefully insert a plug-in board which will hold the pin in proper position to be fully seated.

7. Pull the pin from the wiring side, using a long nose pliers, until the tip of the pin is even with adjacent pins of the same type.

8. Solder the pin using a low wattage iron and standard tip. Hold the soldering iron tip at the base of the pin, but take care not to contact the platter surface.

9. Recheck with ohmmeter for continuity.

After rechecking, if there is no continuity between the copper path and the connector pin, reheat the pin to flow the solder around it. If connection is still not made, add a wire wrap from the pin in question to the nearest pin in the net to which contact is required. Cut the copper path as outlined in paragraph 3.2.2.

3.2.4 REPLACING A TERMINATING RESISTOR (TR) MODULE

Clip all 12 leads just below the ceramic body on the component side of the platter. Use an end cutting tool (RCA Drawing Number 3683293 or equivalent). When all the leads are severed, the block can be removed leaving only the pins in place. Take care that each lead is clipped in turn as it is difficult to locate an unclipped lead. Remove each lead separately using standard pin removal technique described above. Clean holes of excess solder using 0.036 inch diameter drill held in a pin vise. Install the new termination resistor module, and check each pin electrically for opens, shorts, and correct resistance value.

3.3 SIGNAL CABLE REPAIRS

The 70/55 Processor uses two basic types of signal cables (harnesses). Interplatter cables which terminate at platter sockets are inserted or removed with an extraction tool (see Figure 3-2). The platter to I/O cables plug into the platters and terminate at a 75-pin connector (8542395) which mates with a standard interface cable.

> NOTE: Some of the procedure outlined in this section are excerpts from the Harness Assembly Instruction, 3682973.

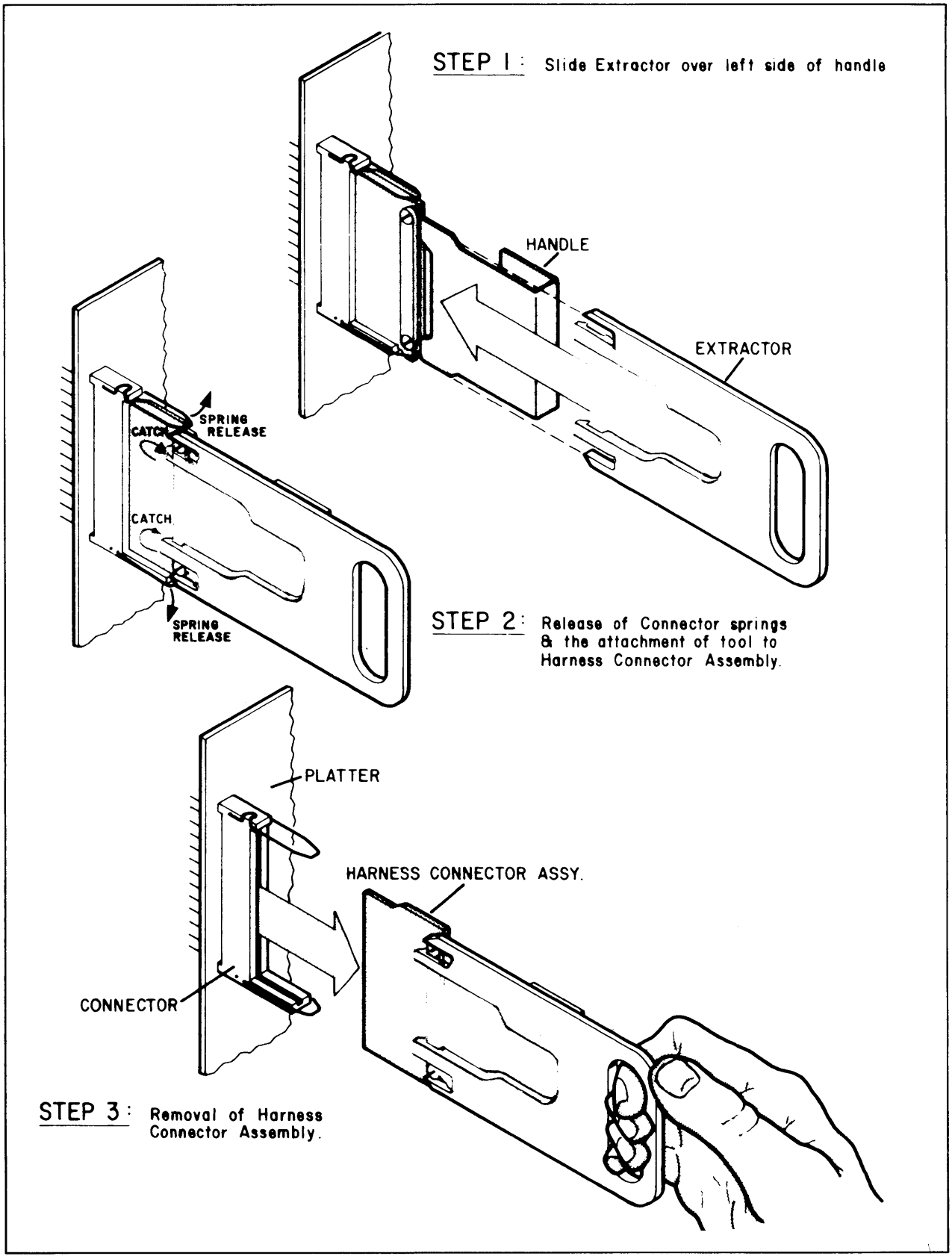


Figure 3-2. Extractor Removal of a Harness Connector

3.3.1 INTERPLATTER CABLES

The Interplatter cables contain twisted triplet wire, RCA drawing number 8541633-1. The red wire is the signal wire; the yellow and white wires are usually crimped in a common terminal (RCA drawing number 3682908-1) which goes to ground. Sometimes the yellow wire is used for a signal that is the complement of the signal on the red wire. The signal wire should be stripped 0.188 $\pm$.010 inch and inserted in a terminal pin RCA drawing number 3682643-1. The terminal is then crimped, using tool, 3682643-3 or equivalent.

Installation of the terminals onto the printed board assembly is shown in Figure 3-3. The signal terminals are inserted into the appropriate hole on the A side of the printed board assembly using an insertion tool (3682643-2 or equivalent). Then the terminal is soldered in place, making sure that the printed pads on both sides of the board are wetted. Do not allow any solder to touch the printed finger contacts. A teflon shield should be used to prevent the heat which is required to melt the solder rings on the signal terminals from melting the solder on the ground bar terminations.

The ground terminals are crimped into a barrel type connector (3682908-1). Then the connector is pushed onto the ground tang with the insertion tool (drawing number 3682908-2 or equivalent). This is also shown in Figure 3-3.

3.3.2 PLATTER TO I/O CABLES

Repairs of the platter end of these cables has been described in the previous portion of this section (3.3.1). If it is necessary to make changes or repairs to a 75-pin connector (drawing number 8542395):

1. Disconnect the mating interface cable.

2. To remove the 75-pin connector, remove the guide pins and nuts at the four corners, using a screw driver to turn the pins.

3. Remove the cable clamp.

Terminal contacts may be removed from the 75-pin connector block (using extraction tool, AMP #305183) by inserting the tool from the contact side until the barrel is seated, then pressing the plunger. To install a new terminal contact:

1. Strip the wire about 0.15 inch.

2. Crimp on the contact required by harness assembly drawing. The tool required will be AMP #90066-2 or 90067.

3. Insert the contact into the connector block.

4. Check to ensure that the retaining lance of the contact is beyond the step in the connector block.

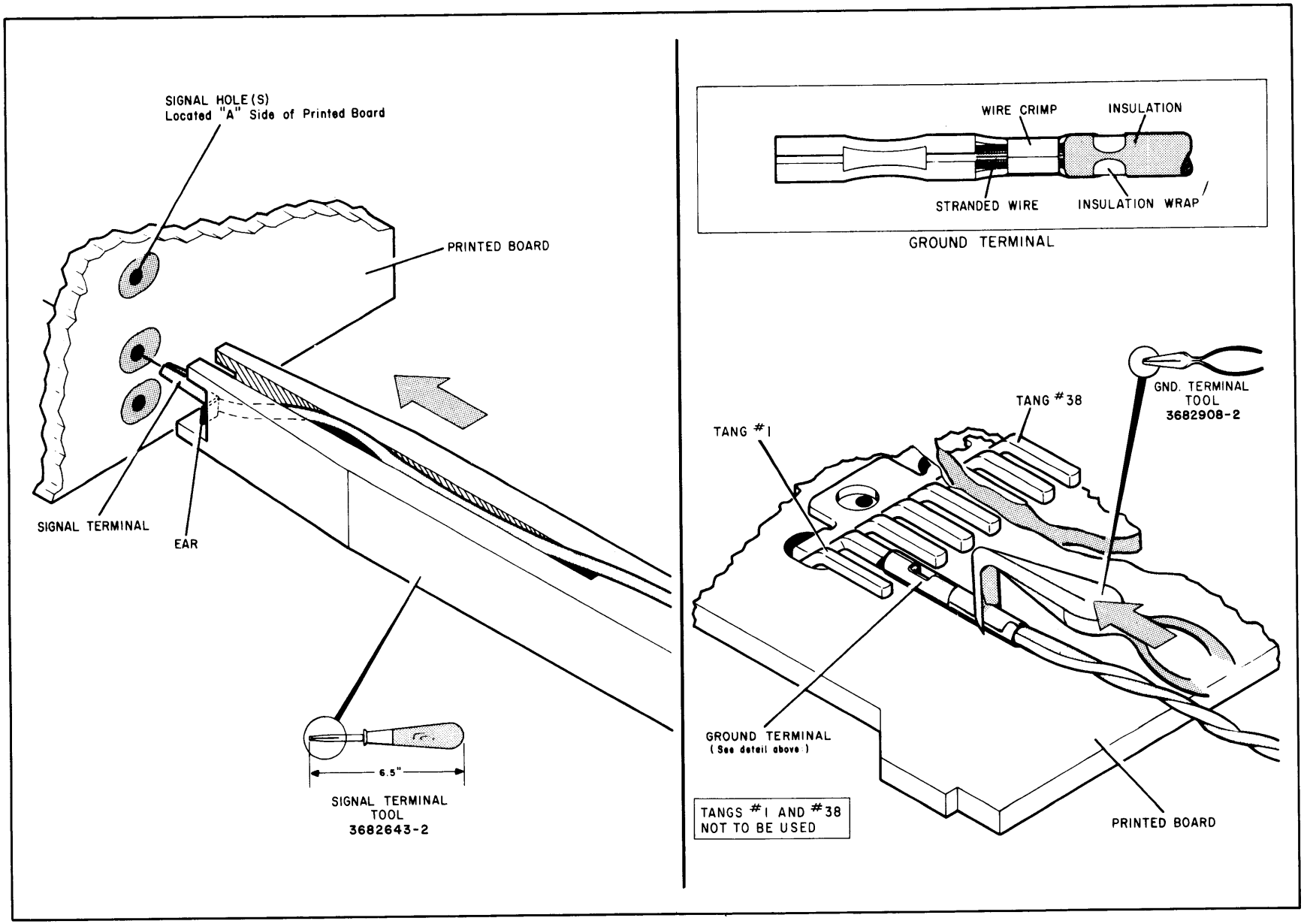


Figure 3-3. Terminal Insertion Procedure

5. Replace the connector in the rack using the guide pins. Be careful to replace the male and female guides at the upper and lower corners, respectively.

In some cases it may be convenient to replace a terminal pin without removing the connector block from the rack. The location of the new pin can be determined on the face (opposite the wiring side) of the connector block. After locating the correct hole, insert a small piece of wire through the block, this will serve as a guide for insertion of the new pin from the wiring side.

3.4 COOLING

The 70/55 Processor cooling system is an important maintenance item. Temperature sensors are located throughout the various racks for the protection of the system against overheating. The sensors will cause an overheat light on the Operator's Console to light. Also, a temperature warning indicator on the Power Supply Control Panel will light. Overheat warning occurs when 122 degrees Fahrenheit is reached or exceeded. These warning indicators are labelled so that the overheating area is identified. If the overheat warning is not seen and corrected, and the temperature rises to 131 degrees Fahrenheit, the temperature overheat sensors will cause the DC power supplies to shut down. Also an overheat indicator will light on the Power Supply Control Panel (Figure 3-4) to show where the overheat occurred.

Immediate corrective action should be taken whenever a temperature warning indicator lights or whenever an overheat condition causes the DC power supplies to shut down.

1. Check the fans in the affected area by holding a hand in the airstream above the fan to determine if air is flowing.

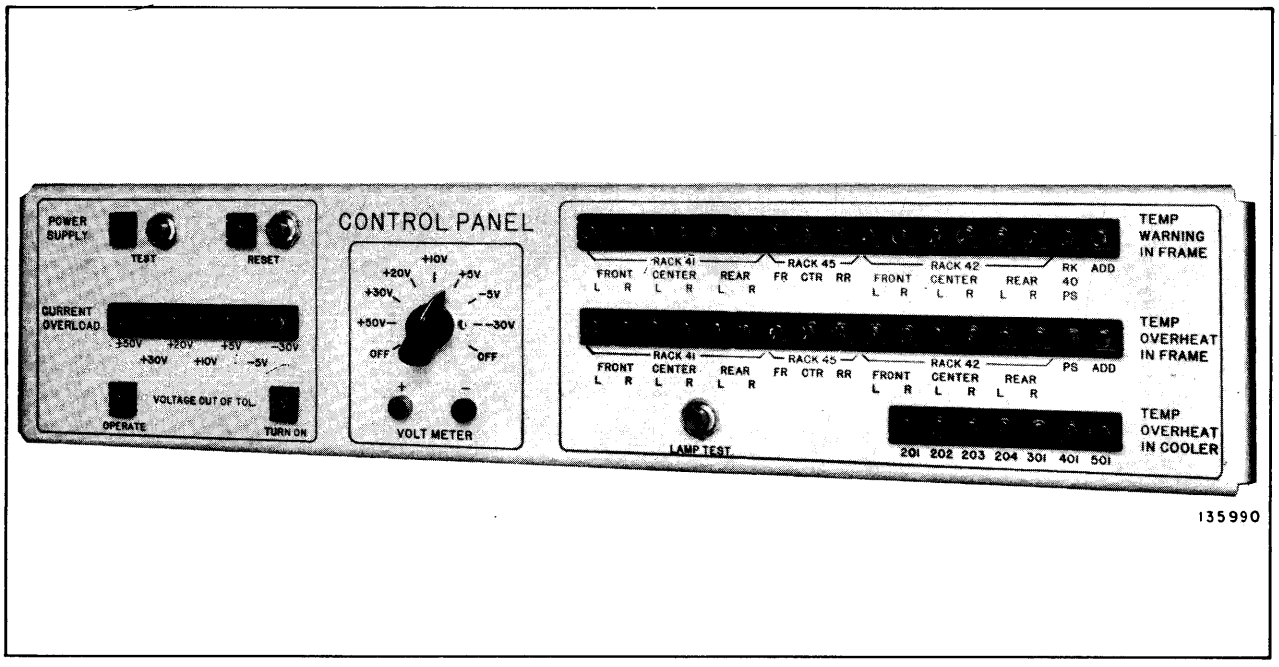


Figure 3-4. Power Supply Control Panel

2. Check the filters in the affected area for dirt or obstruction so that the correct volume of air can be drawn into the equipment. Clean if needed.

   a. With a vacuum cleaner, remove the dust and dirt.

   b. Wash the filter in a mild detergent and rinse thoroughly.

   c. Air dry thoroughly.

3.4.1 BPU COOLING SYSTEM

Each three platter section is suction cooled, utilizing three Boxer fans. The fans are mounted as an assembly at the top of the three platter section. The fan assembly can be removed in the following manner:

1. Remove the ac power from the fans. To do this, CB704 in the basic power supply (Rack 40) and CB103 in the add on power supply (Rack 44) must be turned off.

2. Remove the two nuts, washers and lock washers securing the fan assemblies. These are located at the top (front) of the three platter section, near the right and left corners.

3. Slowly pull the fan assembly straight out until enough clearance is provided to unplug the ac feed lines from the fan assembly.

The air filters in the BPU are mounted on the doors as shown in Figure 3-5.

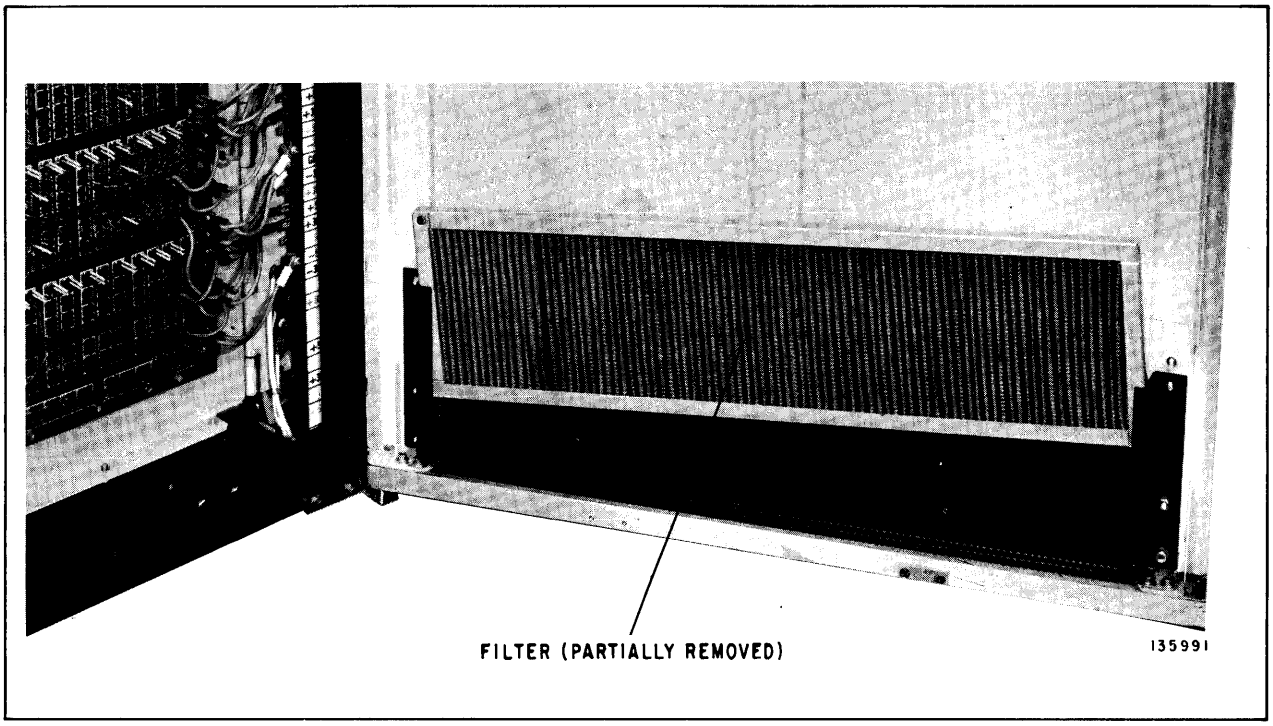


Figure 3-5. Filter Removal, BPU and Power Supply

The fans cause the air currents to enter through the bottom of the doors, through the air filter, between plug-ins on the platters and exhaust from the tops of the racks. The temperature sensors (3.4, first paragraph) are located in the airstream at the top of each three platter section.

3.4.2 MEMORY COOLING SYSTEM

The fan assembly in the Memory racks is the same as the fan assemblies used in the BPU. Removal is described under BPU Cooling System.

Each three platter section of the Memory contains a filter assembly, see Figure 3-6. To remove the filter for inspection and/or cleaning:

1. Unlock the slide fasteners located at the bottom (front) of the three platter section.

2. Pull the tray assembly forward and remove from the unit.

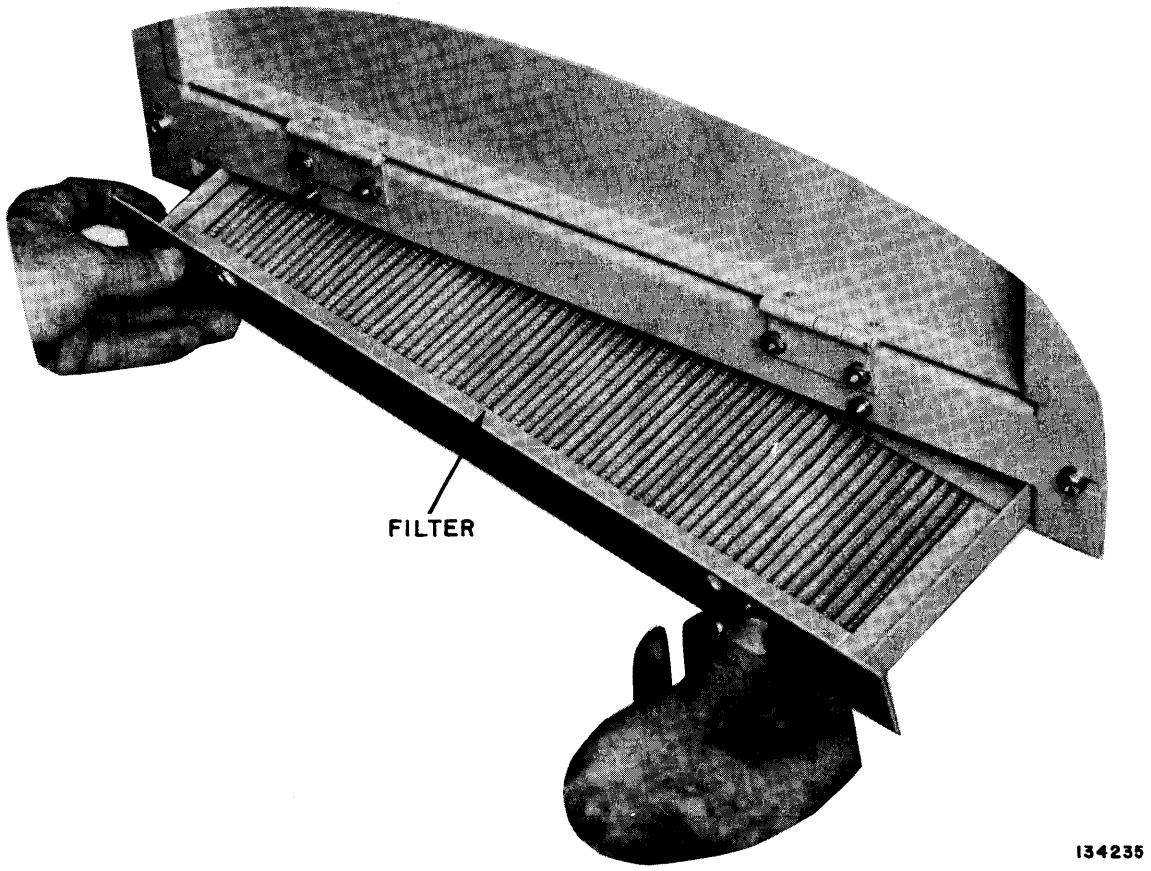


Figure 3-6. Filter Removal, Main Memory

CAUTION

Remove or install the filter tray assembly s-l-o-w-l-y. Care should be taken not to disturb any Cable or Harness assemblies which could be close to the filter tray assembly.

3.4.3 POWER SUPPLY COOLING SYSTEM

Heat dissipation in the main power supply rack can rise to 26,000 BTU/hour when maximum currents are drawn. For this reason, cooling of the power supply racks require movement of large quantities of air.

The air filters are mounted on the doors, as in Figure 3-5.

Fans are mounted on each power supply cooler assembly and on the rectifier assemblies.

There are two chassis assemblies containing four fans each (drawing number 3660767-502). These assemblies are responsible for dissipating the heated air from the top of the power supply racks.

Heat sensors are located on each cooler assembly which (in case of overheat condition) will cause the DC power to shut down and also will light the corresponding indicator on the power supply control panel. The rack heat sensors are part of the two fan chassis assemblies; these also have corresponding indicators on the power supply control panel.

Some of the causes of overheating in the power supply are:

1. Dirty filters or some other obstruction to the flow of air into the unit.

2. Failure of a fan on a cooler assembly or on the rectifier assembly. The fans are permanently lubricated. If the fan power circuitry is complete, then the fan should be replaced if any malfunction is detected.

3. Obstruction of air flow through the cooler assemblies.

4. Failure of a fan in the fan chassis assembly at the top of the rack.

3.5 OPERATOR'S CONSOLE MAINTENANCE

Refer to RCA 8097 Console Typewriter Maintenance Manual 70-01-097 for maintenance instructions on the Operator's Console.

Pages 3-14 through 3-21 Deleted

7. Place the paper under the paper retainer fingers and push the fingers down against the platen.

8. Close the Top Cover and ensure that the paper is properly situated to enable it to move freely when typewriter is in operation.

3.5.2 RIBBON REPLACEMENT

To install a new ribbon in the typewriter proceed as follows: (Reference Figure 3-8.)

1. Be sure that the type box of the typewriter is at the left margin, then raise the Top Cover.

2. Snap the spring latch which secures each spool in position, upward.

3. Raise the inked ribbon up over the roller and out of the ribbon reverse levers on both sides of the typing unit.

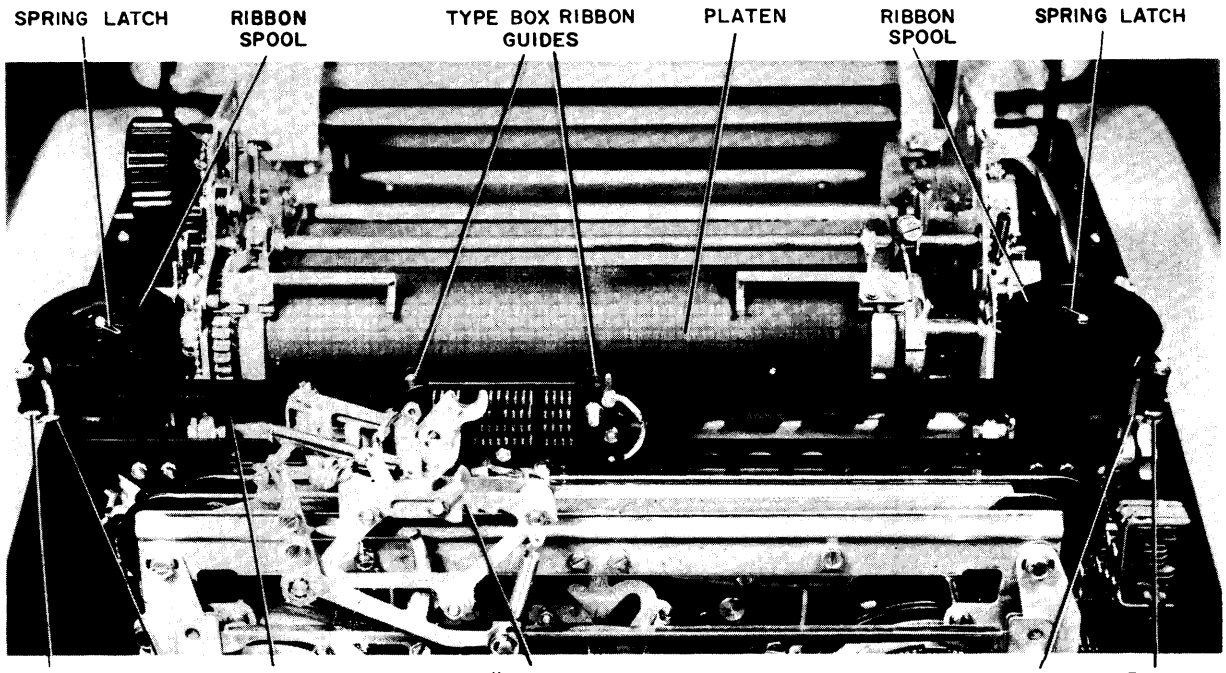


Figure 3-8. Ribbon Replacement

4. Remove the ribbon from the two ribbon guides on the type box carriage.

5. Lift both spools and the ribbon off the typing unit.

6. Unwind and disconnect the ribbon from one of the spools. Discard the other spool and the ribbon.

7. Connect the end of the new inked ribbon to the empty spool and wind on enough ribbon to cover the metal eyelet on the end of the ribbon.

8. Install both spools on their respective mechanisms. Rotate each spool slightly to ensure that each spool is properly engaged with the pin on the mechanism.

9. Slip the ribbon around each roller and into the ribbon reverse levers on both sides of the typing unit.

10. Position the ribbon in the two guides on the type box carriage.

11. Snap the two spring latches downward to secure the spools on their mechanisms.

12. Place the paper in the typing position and lower the cover.

3.5.3 LAMP REPLACEMENT

To replace defective indicator lamps (Figures 3-9 and 3-10) in the Operator's Display Panel, proceed as follows:

1. Grip the Display Panel at the center on both sides and pull the panel forward and up.

2. Using a Bulb Extractor tool, carefully grasp the envelope of the defective bulb and with moderate pressure remove bulb from its socket. (See Figure 3-10.)

3. Install a new light bulb (G.E. Type #334). Make certain bulb base is firmly fitted into its socket.

4. Perform lamp check test to assure that bulbs are indicating properly.

To replace the lamp bulb located under the Top Cover of the Operator's Console proceed as follows:

1. With the type box at the left margin, raise the Top Cover of the Operator's Console. Refer to Figure 3-11.

2. Remove the defective lamp by pushing and turning it counterclockwise until the lamp is released from the bayonette type socket.

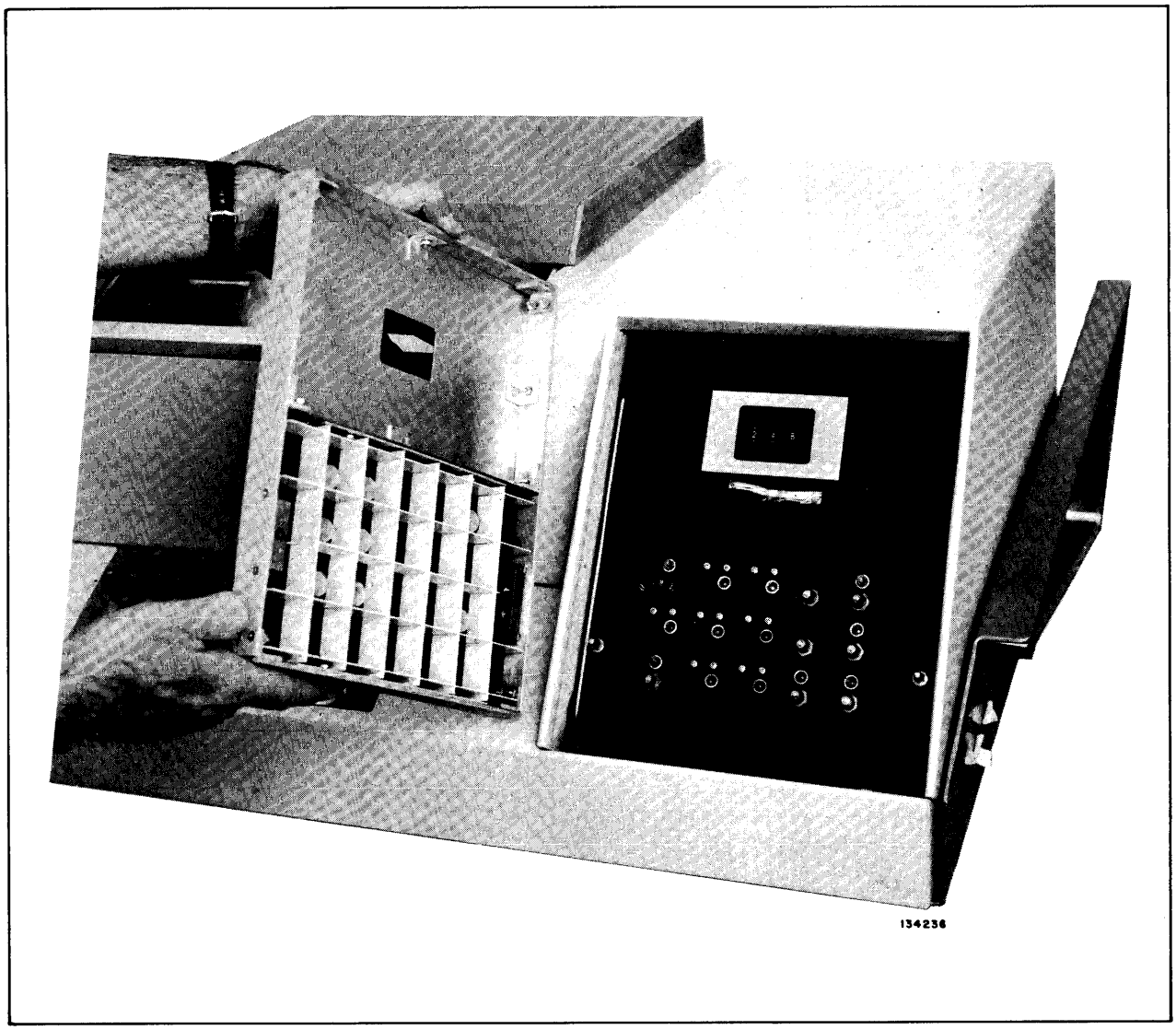


Figure 3-9. Removal of Operator's Display Panel

3. Insert new lamp (G.E. 1314X) into the socket with the lamp pins coinciding with the slot in the bayonette socket. Twist the lamp in a clockwise direction until it is locked into place.

4. Lower Top Cover.

3.5.4 FUSE REPLACEMENT

The Operator's Console is equipped with two tubular glass fuses which are accessible when the top cover of the Console is raised. (See Figure 3-12.)

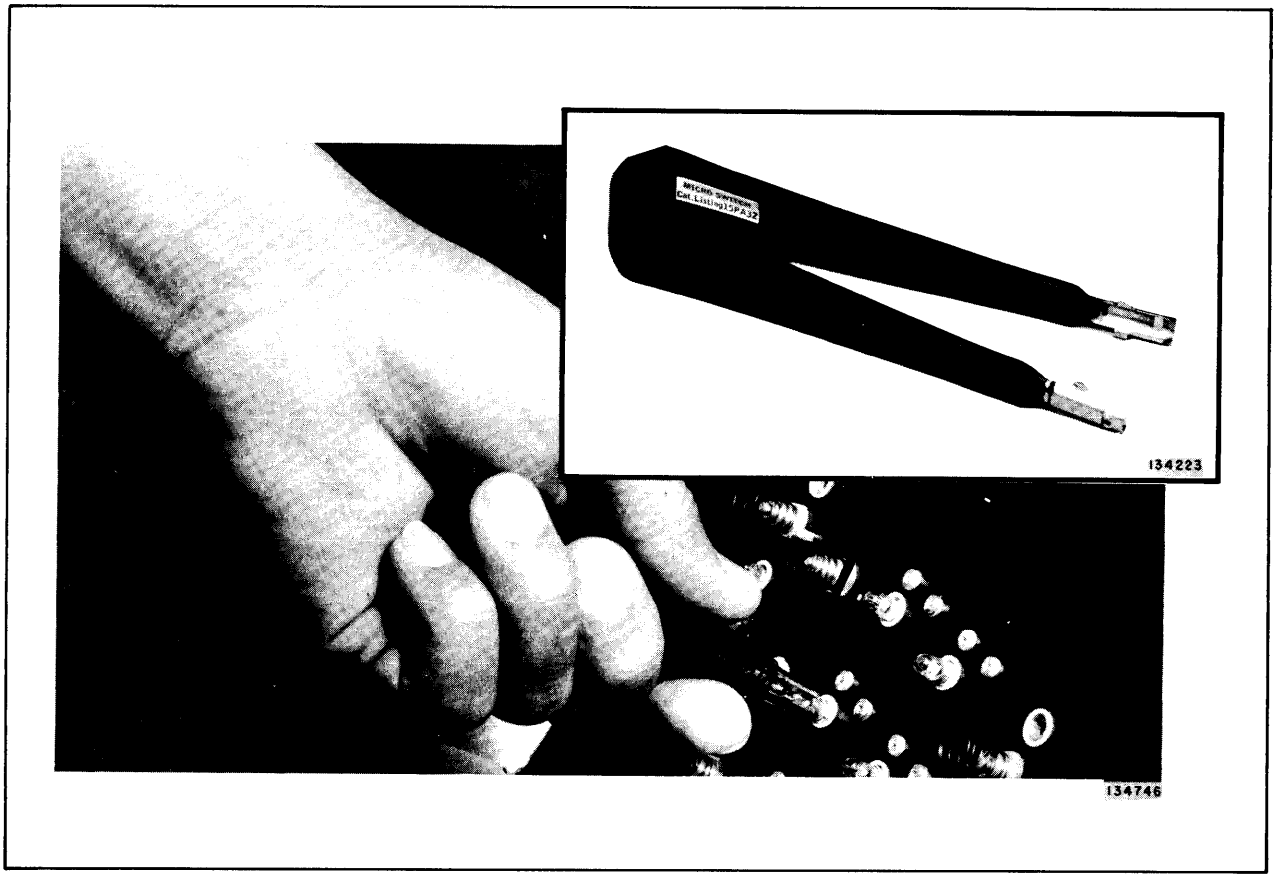


Figure 3-10. Light Bulb Replacement

CAUTION

Never attempt to replace a fuse with the power on. Whenever a fuse is being replaced make certain that the BPU, ac Main Circuit Breaker is in its OFF position.

To replace a fuse proceed as follows:

1. Raise the Top Cover.

2. Determine which of the two fuses has blown by the following:

   a. The MDL 3/8 ampere fuse when blown, will remove the current from the signal line and will be evidenced by excessive chattering in the typing unit.

   b. The MDX 4 ampere fuse, when blown, will remove all electrical power from the typewriter.

3. Turn the fuse holder cap counterclockwise and lift the cap with the attached fuse from the fuse holder.

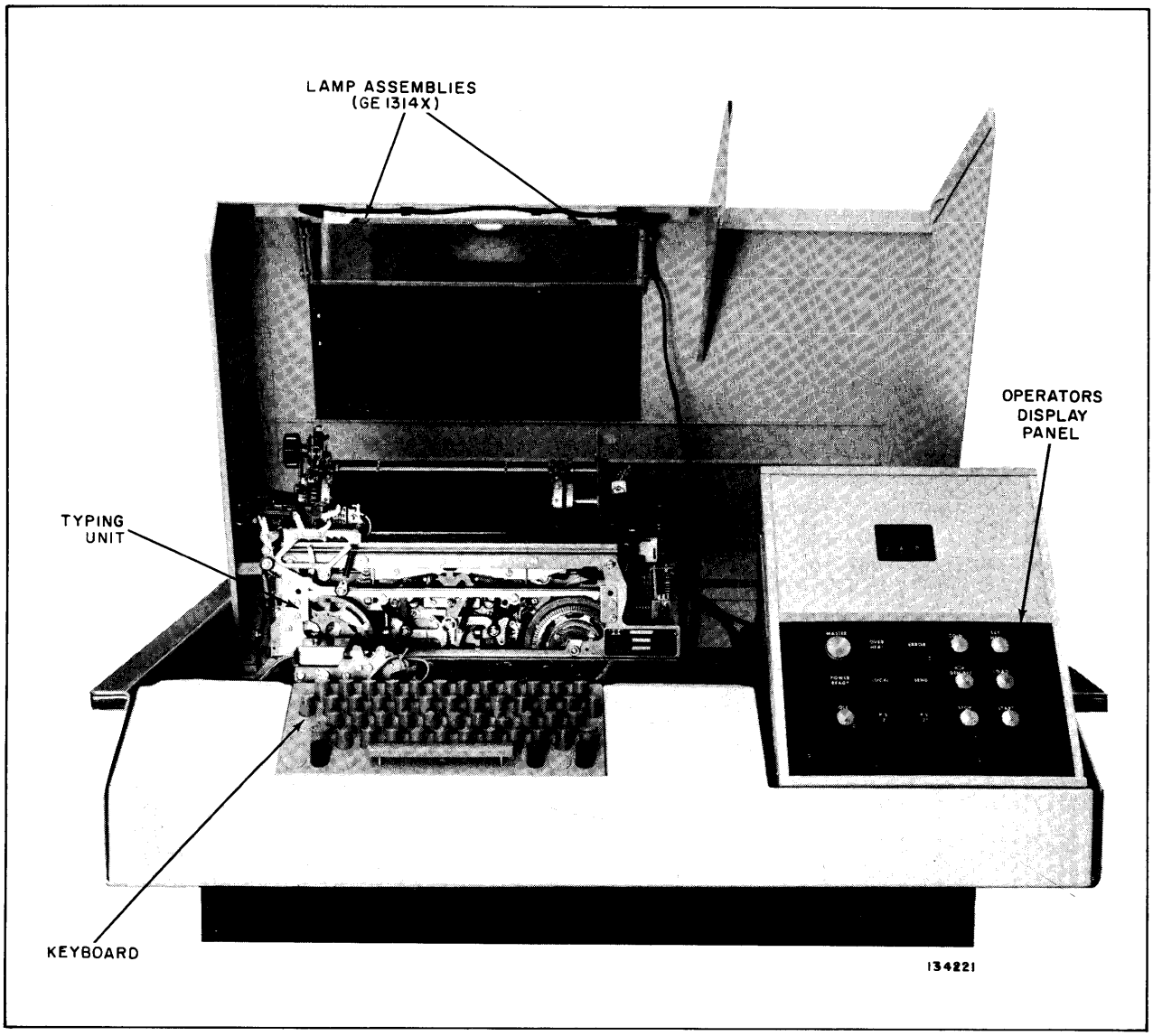


Figure 3-11. 70/97 Operator's Console (Top Cover Raised)

4. Slide the defective fuse out of the cap.

5. Install a new fuse into the cap.

6. Insert the cap and fuse into the fuse holder, ensuring that the slot in the fuse holder and the catch on the cap are aligned.

7. Push the cap downward and turn it clockwise to secure it in position.

8. Place power switch ON.

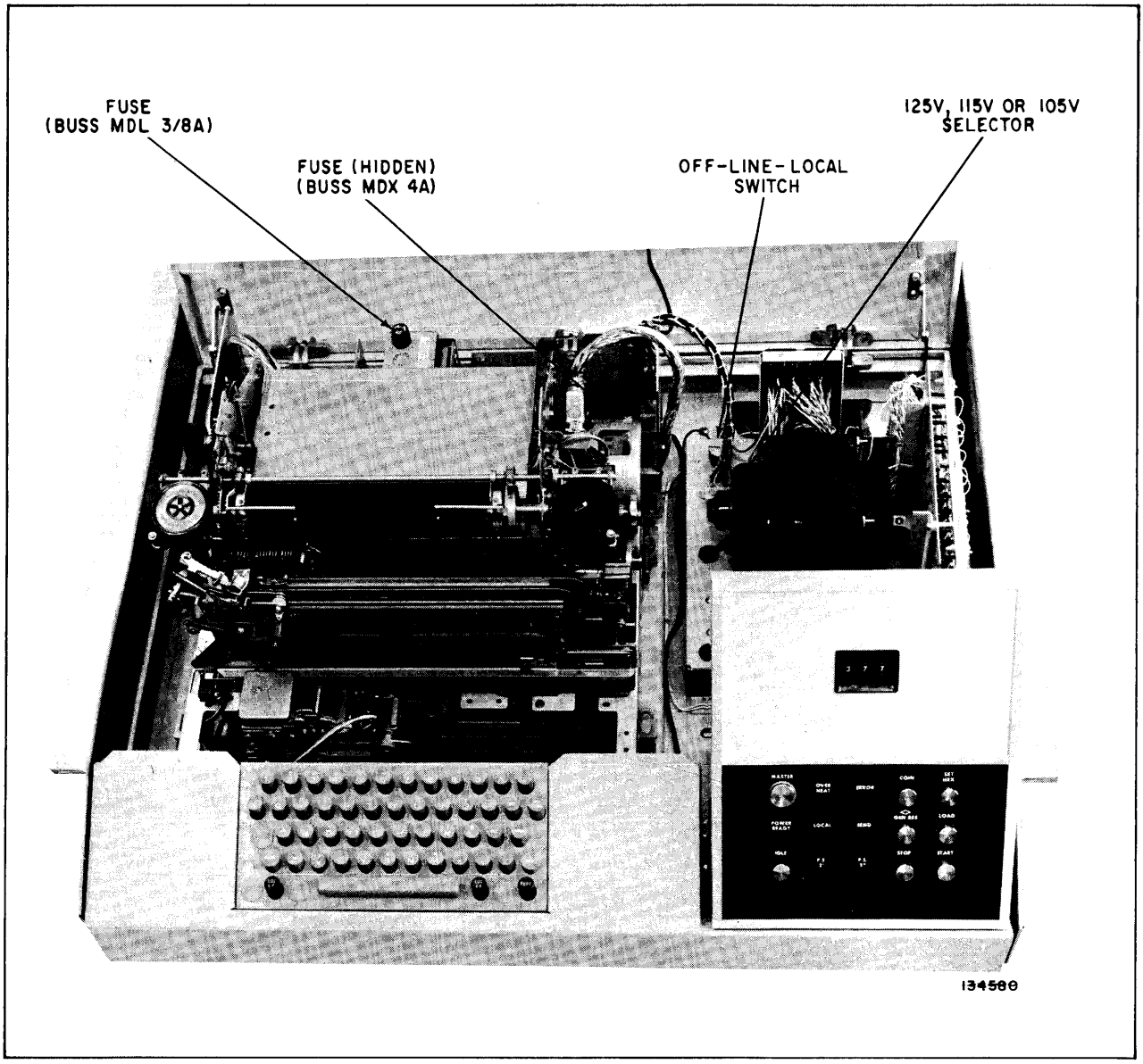


Figure 3-12. Fuse Replacement

NOTE: If the replaced fuse blows the first time power is applied or shortly thereafter, troubleshoot and remove the short.

3.5.5 CLEANING THE TYPE PALLETS

To remove and clean the type pallets proceed as follows:

1. With the type box at the left margin, raise the Top Cover.
2. Push the type box latch to the right to release it. (See Figure 3-13.)

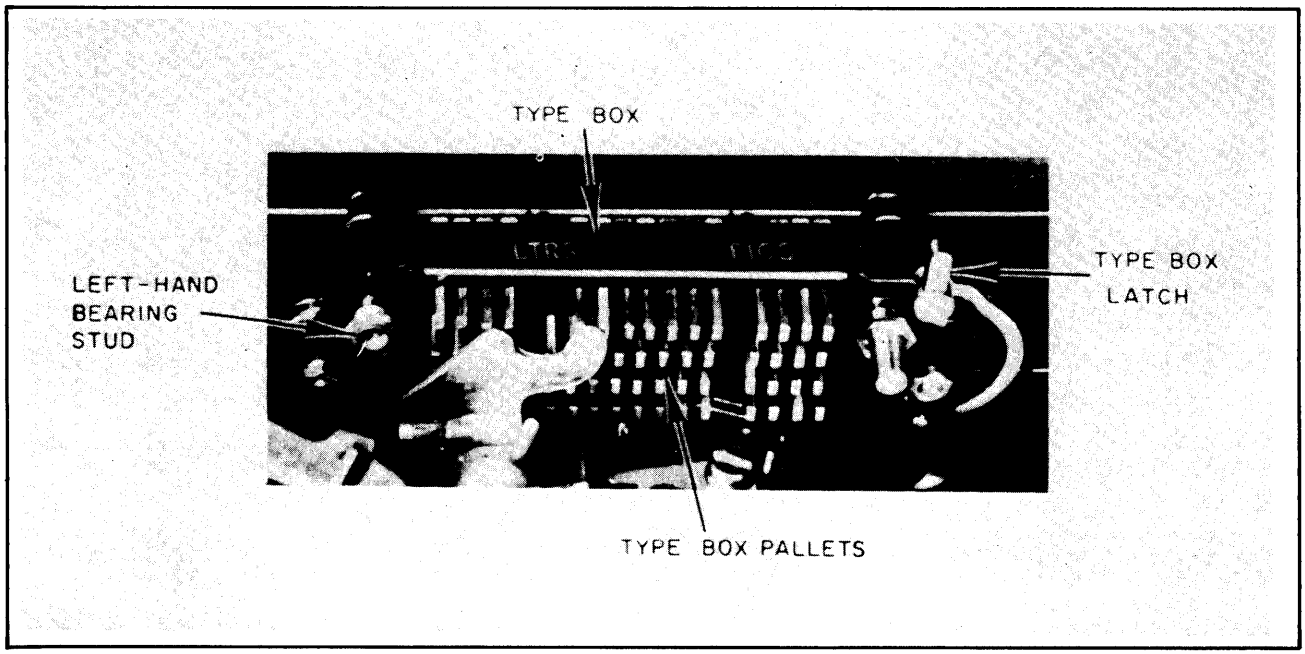


Figure 3-13. Removal of the Type Box

3. Lift the right side of the type box up to approximately 45 degrees and pull to the right to disengage it from the left-hand bearing stud.

4. Clean the face of the type pallets using Eberhard Faber Star Type Cleaner No. 1226.

5. With the right side of the type box elevated approximately 45 degrees, engage the left side of the box with the left-hand bearing stud and push the right side of the box downward.

6. Ensure that the box is firmly seated on the bearing stud. Place the point of the latch in the notch on the box and raise the latch to the left in its lock position.

7. Lower the Top Cover.

3.5.6 CLEANING THE PLATEN

To clean the typewriter platen proceed as follows:

1. Raise the Top Cover.

2. Using the manual platen knob, back the paper completely out of contact with the platen.

3. Using a clean lint-free cloth and an approved cleaning agent, clean the entire rubber portion of the platen.

4. Wipe the platen with a dry, clean, lint-free cloth.

3.7.3 ISOLATION OF AUXILIARY GROUND PATH

An auxiliary ground path can be isolated as follows:

1. Visually check for additional ground straps between dc ground and frame ground in the BPU, memory, and power supply racks.

2. Unplug jack J1 from the bottom of the maintenance panel and note whether the auxiliary ground path is removed. If the auxiliary ground path is removed by unplugging jack J1, disconnect and tape the wire attached to pin 82 of jack J1.

3. If the auxiliary ground is still present, disconnect all white wires from the B block ground bus in all BPU and memory racks. (These are the wires connecting the B block bus to the individual vertical ground buses in the racks.)

4. Measure the resistance between the BPU frame and one of the white wires just removed. If the resistance is less than 2 megohms, the auxiliary ground path is in one of the BPU or memory racks.

5. If the resistance measured in the preceding step is 2 megohms or greater, measure the resistance between the frame and dc grounds in the Power Supply. A resistance less than 2 megohms indicates the auxiliary ground path is in the main Power Supply or the add-on Power Supply, if used.

NOTE

If the preceding isolation procedure indicates that the auxiliary ground path is in the Power Supply, proceed to step 6 for further isolation. If the auxiliary ground path appears to be in the BPU or memory racks, proceed to step 8 for further isolation.

6. Visually check for a short circuit of the T-bar, such as a screw or scrap of wire lying on the ground bar and in contact with the shielding frame.

7. Remove each wire bolted to the vertical ground bus, and check the resistance to ground of each wire as it is removed. When a resistance less than 2 megohms is found, trace that wire to its source, and correct the cause of its auxiliary ground path.

8. If an auxiliary ground path is present in either the BPU or memory, and it becomes necessary to isolate racks, start with the memory and disconnect all edge connectors between the memory and BPU. Since all BPU and memory frames are usually bolted together, a ground on any platter is tied to the other through edge connectors and harness wiring. This makes it necessary to isolate each platter to determine if the auxiliary ground path is in the memory or the BPU.

9. Continue to isolate racks and platters, and check resistance until the auxiliary ground path is found.

3.8 MISCELLANEOUS MAINTENANCE INFORMATION

For more information about troubleshooting, adjusting or replacing parts in various areas of the system, refer to the section of this manual which describes that area.

3.6 STRIP SWITCH CLEANING

Strip switches are cleaned using the recommended contact cleaner, Contact Re-Nu Freon (CSC 241450), sprayed in moderation on the contacts. If further cleaning is necessary, remove the switch from the Maintenance Panel and burnish the contacts with a burnishing tool (CSC 937301).

CAUTION

Do not use any contact cleaner other than that specified above. Do not use emery paper or any abrasive other than a burnishing tool on the contacts. Do not use an EAM card to clean switch contacts as this leaves card fibers on the contact surface.

3.7 IMPROPER DC-TO-FRAME GROUNDING

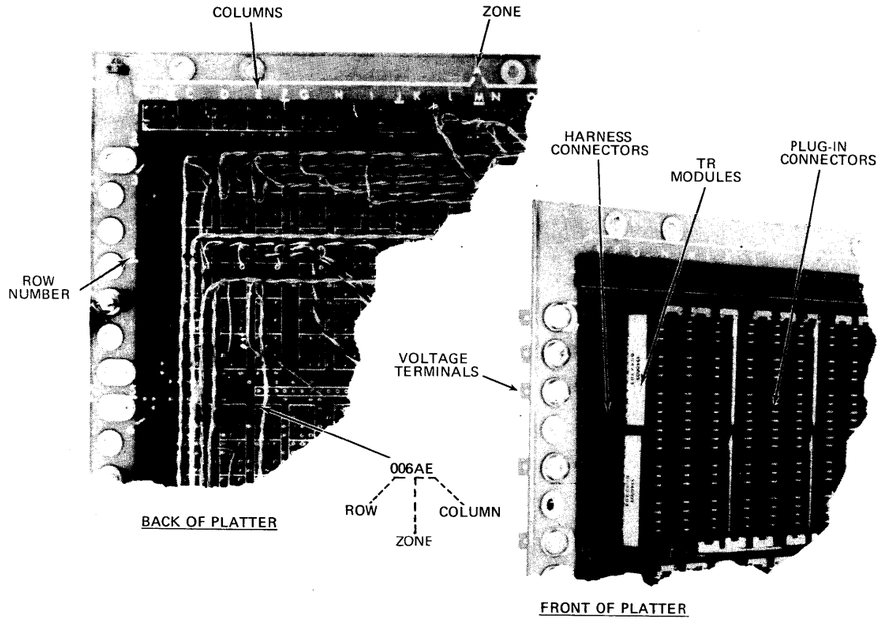
3.7.1 GENERAL

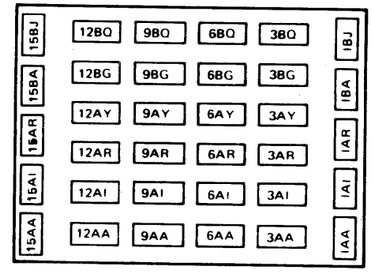
The processor dc ground must be attached to the processor frame ground at only one point or intermittent processor errors may occur. This connection is made at the factory by attaching a ground strap between the B block at the bottom of rack 41 and the processor frame.

3.7.2 CHECK FOR PROPER GROUNDING

To verify that the dc ground is connected to the frame at only one point, perform the following steps:

1. Turn the system power off, including power to all peripheral devices.
2. Turn the main ac circuit breaker off.
3. Disconnect all I/O interface cables from racks 41 and 45.
4. Unplug cables attached to jacks J1 and J2 in the console typewriter.
5. Disconnect the ground strap from the B block at the bottom of rack 41.
6. Measure the resistance between the dc ground bus and the frame of the BPU. If a reading of less than 2 megohms is obtained, an auxiliary ground path exists in the BPU, memory, or power supply rack.





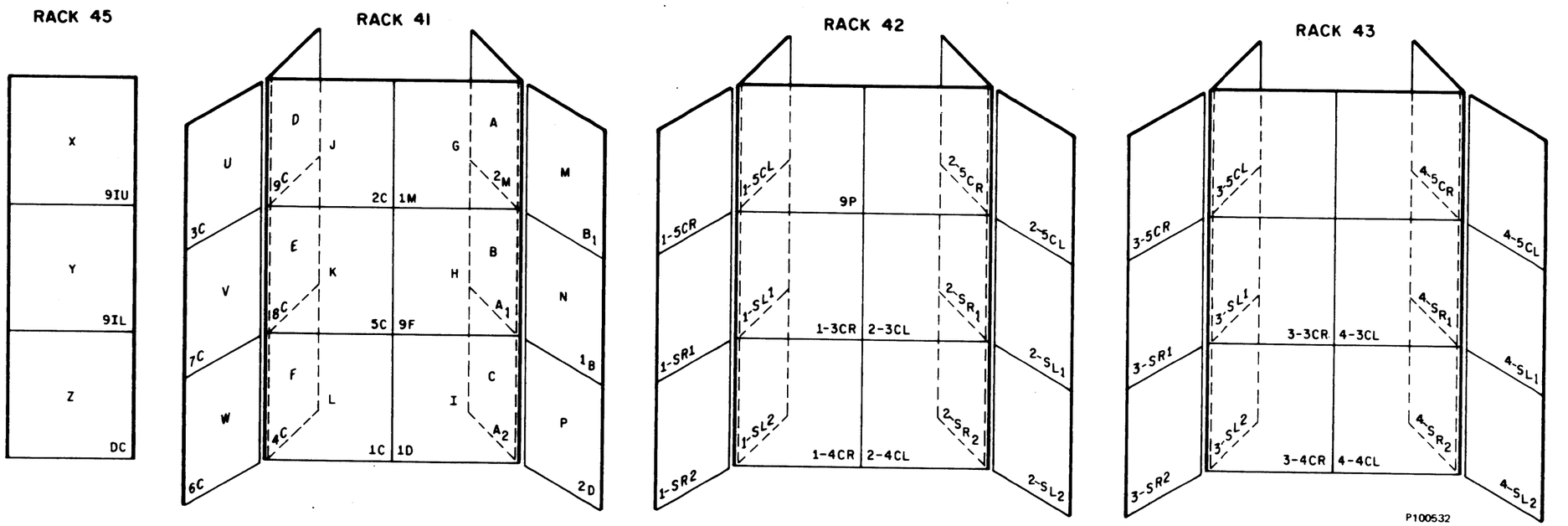


Figure 3-14. Rack and Platter Location

SECTION FOUR

BPU THEORY

4.1 GENERAL

The logic of the 70/55 Basic Processing Unit (BPU) is based on Integrated Circuit Packages (ICP's). These in turn are mounted on Series Eight plug-ins. For descriptive material about the individual logic elements, refer to the Microfiche File, Publication 70-FE-003, Series 8 Data Sheets, Index Sheets P and Q.

4.1.1 LOGIC DRAWING REFERENCES

In this logic description, drawing references will generally be given as a three digit number. This number represents the last three digits of the seven digit drawing number, 3660XXX.

The exceptions to this procedure may be found in Main Memory signals or in signals originating in an option platter such as Memory Protect or Direct Control. The exception signals will be designated as a four digit number representing 366YYYY. On the drawings that are unique to the above exceptions, the BPU signals will be referenced as four digit numbers, and the particular signals within the option structure will be referenced as three digit numbers.

To designate a particular logic element, a six character code is used. For example, 123A4B;

1. The first three characters (123) are a logic drawing number.

2. The next two characters (A4) are coordinates of that logic drawing which locates an area in which a logic element is shown.

3. The last character (B) identifies the specific logic element.

Each logic element on a drawing has the following information contained within the logic symbol.

1. Top row (B-A4B). The first character (B) shows the platter on which the logic element is located. See "Platter Locations" in Section Two of this manual. The last three characters (A4B) designate that logic element as described in the previous paragraph.

2. The second row is the plug-in type. This number identifies the plug-in type and its variation as listed in the Series Eight Maintenance Data Sheets, 70-01-013.

3. The bottom row shows the plug-in location on the platter.

4.2 FUNCTIONAL DESCRIPTION

This section describes the functions of major segments of logic in the 70/55 Processor.

4.2.1 BPU DATA LOGIC

The BPU Data Logic Block Diagram is shown in Figure 4-1. Interchange of Data takes place by way of the Information Bus (IB). Control of the IB takes place in the Bus Separator Logic (drawings 238-241). The Bus Commands are listed in Section 4.2.8.2. Some references to the byte (C0, C1 etc.) and specific bits are used in this description. Figure 4-2 shows the relative character and bit positions.

4.2.1.1 DR (Data Register) drawings 803-806

DR is a 32 bit multi-purpose register and is said to contain the X operand. Any of its four characters can be set or reset by way of the maintenance console. DR receives its data from Scratch-Pad during SPC-RD (Scratch Pad Read). DR can also be fed by IB. Either a word, byte, character C0 or C3 can be selected by command SDRW, SDRK, SDRC0, or SDRC3. SDRK is function of IOU.

The contents of DR are used as follows:

1. Parity check (drawing 206)
2. Parity predict (drawing 207)
3. Recognition (drawing 208)
4. Scratch-Pad Regenerate (drawing 201, 202, and 203).
5. Adder - via one of the Adder Commands generated on drawing 245 or 246.
6. Transfer - via one of the transfer commands, which is applicable to DR, generated on drawing 246.

The first stage outputs after the X-collect (drawings 209, 215, through 219) are called X(00-31). These outputs feed the Adder, the inputs of IB, and the recognition of sign and valid data.

4.2.1.2 UR (Utility Register) drawing 210

UR is a 32 bit register and is said to contain the Y operand. Any of its four characters can be set or reset by means of the maintenance console. UR, receives its data from IB, a word/half word (C_0 and C_1 only) by the Command SURW/SURM.

The contents of UR are used as follows:

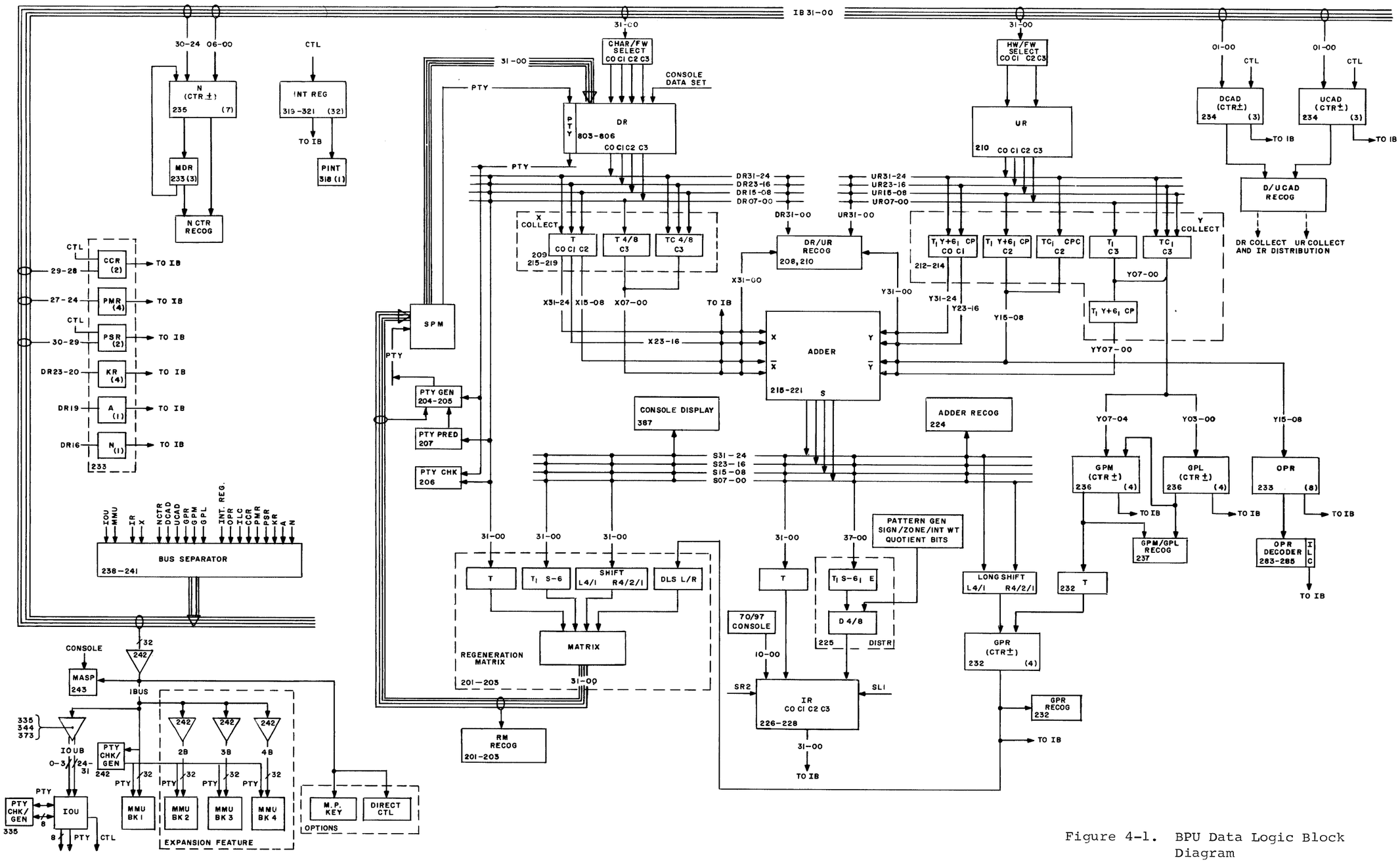


Figure 4-1. BPU Data Logic Block Diagram

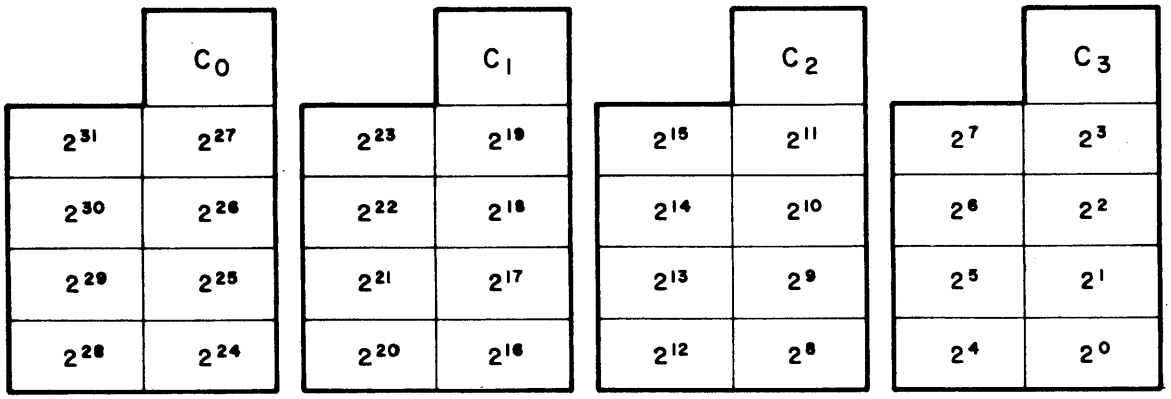


Figure 4-2. Character and Bit Relationship

1. Recognition, (drawing 210)

2. Adder - via one of the Adder commands generated on drawing 245 or 246.

3. Transfer - via one of the transfer commands, which is applicable to UR, generated on drawing 246.

The first stage outputs after the Y collect (drawing 212, -214) are called (Y(00-31). These outputs feed the Adder, the General Purpose Least (GPL), General Purpose Most (GPM), and Op-code Register (OPR), and the recognition logic for sign and valid data.

If the Adder command is DAW (Decimal Add Word) or DAK (Decimal Add Character), (+6) is added to each digit of UR.

4.2.1.3 Adder (drawings 215, -221)

The Adder can add, subtract, perform logical functions, and transfer either a word, halfword, character, or digit. Controls are mechanized as per Adder Control Chart #1 and #2, (drawings 222 and 223).

The outputs of the Adder S(00-31) are used as follows:

1. Console Display

2. Adder Recognition (drawing 224)

3. Regeneration to Scratch Pad

   a. Binary number - depends upon regenerate command (drawing 254)

   b. Decimal number - if necessary, (6) is subtracted from each digit (drawing 201 - 203).

   c. Shift Left/Right 1 or 4 bits, or shift right 2 bits (drawing 255).

4.2.1.4 IR (Intermediate Register) drawings 226 - 228)

IR is a 32-bit Double Rank register. Any of its four characters can be set or reset by means of the maintenance console. IR receives its data mostly from intermediate operation through the S bus, either a:

1. Word

2. Character - f(DCAD) - if the character is a result of decimal operation, and if necessary, (6) is subtracted from each digit before reading into IR (drawing 225).

3. Digit - f(DCAD & DIGIT) - the digit may;

   a. EIRL - Exchange IR Left S(00-03) to IR (04-07) or

   b. EIRR - Exchange IR Right S(04-07) to IR (00-03).

The sign and zone digits generated by SIR(00-03)D & SIR(04-07)D, respectively. The code depends on the setting of the A (ASCII) flip-flop. The read-in of SIR(00-03)D and SIR(04-07)D into IR is f(DCAD).

Values of the various interrupts are generated into IR(02-06), see drawing 225.

The setting of Digit Switches on the operator's console are read into IR(00-10) during a "LOAD" by command SIRFC, drawing 226.

IR00 is set by command GIRQ when either a fixed or floating point divide instruction is in process.

The contents of IR can be shifted right by 2 or left by 1 internally. The output of IR feeds IB.

4.2.1.5 N Counter

The N Counter is a 7 bit register (see drawing 235). It is used to keep track of the number of shifts in a shift instruction, to increment or decrement the value of the exponent in floating point instructions. The least 4 bits are also used to address each of the 5 scratch pad locations used in the Multiply Decimal Instruction. The most 3 bits are also used to address utility registers 3, 4, 5, and 6 in scratch pad. The N Counter can address every one of the 128 locations in scratch pad if SPA is set to (01)8. For N Counter recognitions see drawing 237.

4.2.1.6 MDR Register

The MDR (Multiply Divide Decimal) Register is a 3 bit register (see drawing 233), which keeps track of the length of the Multiplicand or Dividend in the Multiply or Divide Decimal instructions.

4.2.1.7 GPM Register

The General Purpose Most register is a 4 bit register. It can only be set from Y(04-07), see drawing 236. This register contains the length of the OP 1 word and sometimes part of the count, where GPM and GPL are used. It is also part of a byte where GPM and GPL are used in the SI format instruction.

4.2.1.7 GPM Register

The General Purpose Most register is a 4 bit register. It can only be set from Y(04-07), see drawing 236. This register contains the length of the OP 1 word and sometimes part of the count, where GPM and GPL are used. It is also part of a byte where GPM and GPL are used in the SI format instruction.

The GPM recognition signals are:

1. GPME17(236-B6A): GPM is equal to $(17)_8$ - GPM(00,01,02,03) flip-flops are set.

2. GPMZ(236-B5A): GPM is equal to zero - GPM(00,01,02,03) flip-flops are reset. The GPM register is displayed on the maintenance panel when OPR button is depressed.

4.2.1.8 GPL Register

The General Purpose Least register is a 4 bit register. It can only be set from Y(00-03), (see drawing 236).

This register contains the length of the OP2 word and sometimes part of the count, where GPM and GPL are used. It is also part of a byte where GPM and GPL are used in the SI format instruction.

The GPL recognition signals are:

1. GPLE17 (236-B4A); GPL is equal to $(17)_8$ - GPL(00,01,02,03) flip-flops are set.

2. GPMLZ (236-B3A); GPM and GPL are equal to zero - GPM and GPL flip-flops are all reset.

The GPL register is displayed on the maintenance panel when OPR button is depressed.

4.2.1.9 OPR Register

The Operation register is an 8 bit register which contains the instruction to be executed. It is set from Y(08-15), see drawing 233.

The OPR register is displayed on the maintenance panel when OPR button is depressed.

OPR, GPM, and GPL are set in 5C0 status level (Staticizing). The command BAH (Binary Add Halfword) as a function of UCAD, always places OPR, GPM, and GPL on Y(15-00).

4.2.1.10 GPR Register

GPR is a 4 bit register called General Purpose Register. It is used to store bits during shifts and decrement/increment GPM count while GPM is preserved. See drawing 232 for the set conditions of this register.

The GPR recognition signals are:

1. GPRZ (232-A5B); GPR is zero - GPR(00,01,02,03) flip-flops are all reset.

2. GPRE17 (232-A4A); GPR is equal to $(17)_8$ - GPR(00,01,02,03) flip-flops are all set.

3. GPRG2 (232-A4C); GPR is greater than 2 - GPR(00,01) flip-flops are set or GPR02 flip-flop is set.

4. GPRG6 (232-A3B); GPR is greater than 6 - GPR(00,01,02) flip-flops are set or GPR03 flip-flop is set.

The GPR register is displayed on the maintenance panel when N button is depressed.

4.2.1.11 DCAD Register

DCAD is a 3 bit register used to control the byte addressing of DR register and the digit or byte addressing of IR register. Two bits of the input bus are used to set this register. IB00 and IB01 set DCAD01 and DCAD02, respectively. DCAD00 can be set with a special control signal or by triggering DCAD register up or down 1. See drawing 234.

The digit/byte equivalents are shown below.

DCAD Setting	DR Address	IR Address
000	C0	D0/C0
001	C0	D1/C0
010	C1	D2/C1
011	C1	D3/C1
100	C2	D4/C2
101	C2	D5/C2
110	C3	D6/C3
111	C3	D7/C3

For DCAD recognition see drawings 209 and 237.

This register is displayed on the maintenance panel when OPR button is depressed.

4.2.1.12 UCAD Register

UCAD is a 3 bit register used to control the digit or byte addressing of UR register. Only 2 bits of the input bus are used to set this register. IB00 and IB01 set UCAD01 and UCAD02, respectively. UCAD00 can be set with a special control signal or by triggering UCAD register up or down 1. See drawing 234.

The digit/byte equivalents are:

UCAD Setting	UR Address
000	D0/C0
001	D1/C0
010	D2/C1
011	D3/C1
100	D4/C2
101	D5/C2
110	D6/C3
111	D7/C3

For UCAD recognition see drawings 211 and 237.

This register is displayed on the maintenance panel when OPR button is depressed.

4.2.1.13 Condition Code Register

The Condition Code Register (CCR), see drawing 233, is a two bit register. It indicates results obtained during the operation of an instruction.

The CCR can be manually set from the maintenance panel by depressing OPR strip switch, setting 2^{28}, 2^{29} bits in DR register and depressing SETREG switch. Control of CCR is shown on drawing 266 and 267.

4.2.1.14 Program Mask Register

The Program Mask Register (PMR), see drawing 233, is a four bit register. It is set by the non-privileged instruction, Set Program Mask, and it applies to the following interrupt conditions:

1. Significance Error
2. Exponent Underflow
3. Decimal Overflow
4. Fixed-Point Overflow

If any of the four bits in the PMR are reset, no interrupt flag can be generated for the interrupt condition occurring. If any of the four PMR bits are set, the interrupt flag can be generated in the Interrupt Flag Register (IFR). Either the interrupt is allowed by IMR masking or becomes pending.

The PMR can be manually set from the maintenance panel by depressing OPR strip switch, setting 2^{24}, 2^{25}, 2^{26}, 2^{27} bits in DR register and depressing SETREG switch.

The PMR can also be set by using the Program Control (PC-82) instruction.

4.2.1.15 Processor State Register

This is a two bit register. GENRES switch, when depressed, sets PSR (00,01) - this is processor state 1. The four processor states are indicated as follows:

	PSR 01	PSR 00
Processor State 1	1	1
Processor State 2	1	0
Processor State 3	0	1
Processor State 4	0	0

When GENRES switch is depressed the PSR is set to Processor State 1 and can be reset to any other Processor State by depressing PSR00SW/PSR01SW on the maintenance panel (see drawing 233). PSR can be set to any Processor State by software.

4.2.1.16 Key Register

This is a four bit register (KR - see drawing 233) which contains the memory protection key. When an interrupt occurs, the key in the Interrupt Status register of the processor state being initiated is placed in this register.

This four bit key provides a possible 15 keys ranging from 1_{16} to F_{16}.

Each 2,048 byte block of main memory has its individual cell for the protection key in the Memory Protect Memory. These cells can be loaded with any key by the SSK instruction. When the key related to the current processor state and the key related to the main memory block are equal or either is zero, the main memory block accepts a data store. Conversely, if the keys do not match, and neither is zero, an address error interrupt occurs. The KR can be manually set from the maintenance panel by depressing N strip switch, setting 2^{20}, 2^{21}, 2^{22}, 2^{23} bits in DR register and depressing SETREG switch.

This KR should not be confused with the MUX or SEL Key register. During I/O data transfer into the memory, the MUX and SEL Key Registers serve the same protection function, in conjunction with the Memory Protect Memory.

4.2.1.17 A Register

This is a one bit register (see drawing 233). If it is set, ASCII code is established; if it is reset EBCDIC is established.

It can be set in the PINT routine or by depressing N strip switch, setting 2^{19} bit in DR register and depressing SETREG switch.

4.2.1.18 Non-Privilege Register

This is a one bit register (NPRIV), see drawing 233. This is set by the program to indicate the privileged status of the processor state being initiated. If it is set the processor state runs in the non-privileged mode, inhibiting the execution of the privileged instruction; if it is reset the processor state allows execution of the privileged instructions.

4.2.2 BPU CONTROL LOGIC

The BPU Controls are shown in the block diagram Figure 4-3. This block diagram shows symbols representing the logic segments and their interrelationships. The symbols contain logic drawing reference numbers and the name (or abbreviations) of the logic. These block diagrams will be extremely useful for the maintenance personnel.

4.2.2.1 Timing Pulse Generator

The basic timing of the 70/55 Processor is controlled by the clock pulses produced by the Timing Pulse Generator (see drawing 323). The Timing Pulse Generator is in turn controlled by a crystal controlled oscillator (8003 plug-in) which has a 120 nanosecond period. The minimum pulse width produced by the generator is 60 ns. Figure 4-4 shows the various outputs. The C pulses are the primary pulses. The D pulses are delayed from the C pulses by 60 ns. The status levels (which are described in greater detail in Section 4.2.6) control the number of timing pulses that will be generated in each cycle.

Every status level has three common pulses; C1, C5 and C6. The corresponding D pulses are automatically generated. Figure 4-4 shows the four possible combinations of TP's. As indicated, TP's C2, C3, C4 are skipped in the three TP cycle; TP's C3, C4 are skipped in the four TP cycle and TPC4 is skipped in the five TP cycle. This is caused by the SKIP flip-flop (323-A6C). By controlling this flip-flop, C2, C3 and/or C4 can be inhibited.

In addition to the 120 ns TP's, the timing generator also produces 60 ns TP's and 180 ns TP's. These are shown and explained in Figure 4-4.

The TP generator also has the ability to pause if the memory is busy. The WAIT flip-flop (323A5B) can inhibit generation of C5 until the memory unbusies and sends back an accept pulse to reset the WAIT flip-flop. These memory addressing TP cycles are also shown in Figure 4-4.

When the TP generator is in a free running state, (not generating status level TP's) it generates five TP's. The SKIP flip-flop is set by the D3M pulse in each cycle and is reset by D5, thus, the C4 TP is inhibited.

4.2.3 START-STOP

The Processor is in a stopped state when the RUN flip-flop (322B7D) is reset. This generates HOLD (289B8B) which inhibits the generation of PSM, PXM, PNM, SM, XM and NM. These are mode control signals (see Section 4.2.4) which control status level generation which in turn must be present to perform any Processor operation.

Figure 4-5 shows the timing diagrams for setting and resetting the RUN flip-flop.

The STOP flip-flop (322D5A) can be set by pressing the STOP switch on the Operator's Console or the ICSP switch on the Maintenance Panel. This prevents the next instruction from being staticized but allows a ten second delay before resetting the RUN flip-flop. This permits any I/O instruction, previously initiated, to be completed. Should the ICSP switch on the Maintenance Panel be left in the ON state, the STOP flip-flop stays in the set condition and cannot be reset. This eliminates the ten second time out before resetting the RUN flip-flop for subsequent stops.

4.2.4 MODE SWITCHING CONTROL

The 70/55 can operate in any one of three modes, besides the special snap-shot mode. The three modes are normal mode (NM), multiplexor mode (XM), and selector mode (SM).

PNM, NM, PXM, XM, PSM and SM all enable their respective status level decoders. Hence, no pre-status levels or status levels are generated if these modes are inhibited. With no status levels, operations cannot take place in the machine.

The description below applies to drawing 289.

1. Gate-D3B

   Inputs LIP, XAC, PSM, MSINT and SPSM will inhibit the set of PNM if any one of these are active. This prevents any NM operation from taking place. The meanings of these signals follow:

   LIP (Load in progress) - Indicates transfer of data from a peripheral device to main memory after the LOAD button is pressed.

   XAC (Multiplexor active) - Multiplexor operations are being done which must finish before returning control to NM operation.

   PSM (Pre-selector mode) - Selector operations are being done which must finish before returning control to NM operation.

   MSINT (Multiplexor service interrupt) - Multiplexor channel requests service.

   SPSM (Set Pre-selector mode) - Selector channel requests service.

   If none of the above signals inhibits gate D3B, then the Processor is allowed to perform operations in the NM mode.

2. Gate-C2B

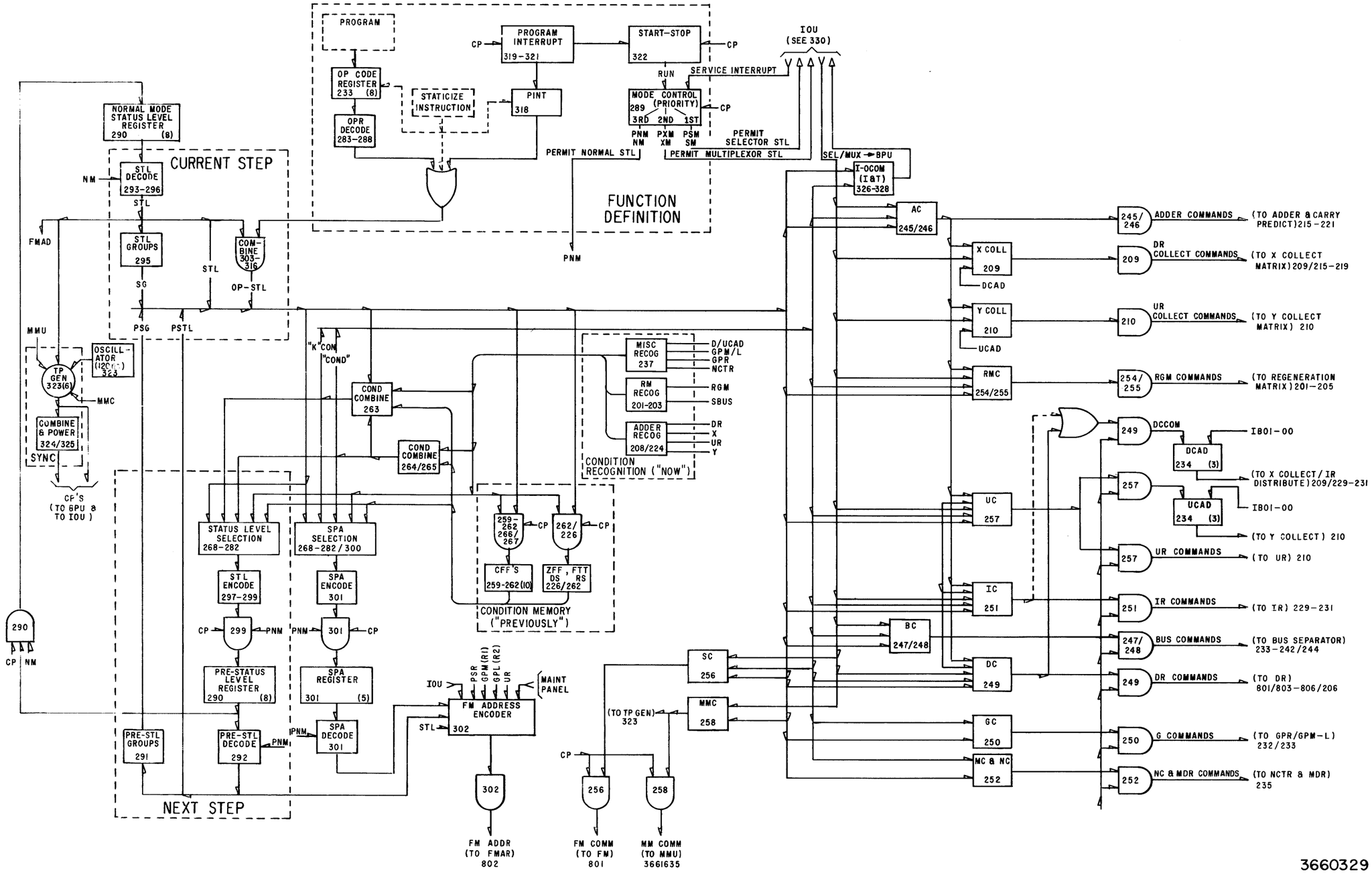
   Inputs HOLD, ISIM, SNAP and NORSP will inhibit PNM if any one of these go high.

   HOLD (Hold) - When the RUN flip-flop is reset or a Read/Write from/to main memory is done from the maintenance panel, HOLD goes high.

   ISIM (Inhibit simultaneity) - This prevents transfer to NM until the I/O servicing is completed.

   SNAP (Snap-shot mode) - Snap-shot operation is separate from NM operation and therefore NM operation has to be suppressed.

   NORSP (Normal Stop) - This prevents a new instruction from being staticized while an I/O operation (if any) is allowed to be completed during a 10 second delay, from the time that NORSP flip-flop is set.



3660329

Figure 4-3. 70/55 BPU Control Block Diagram

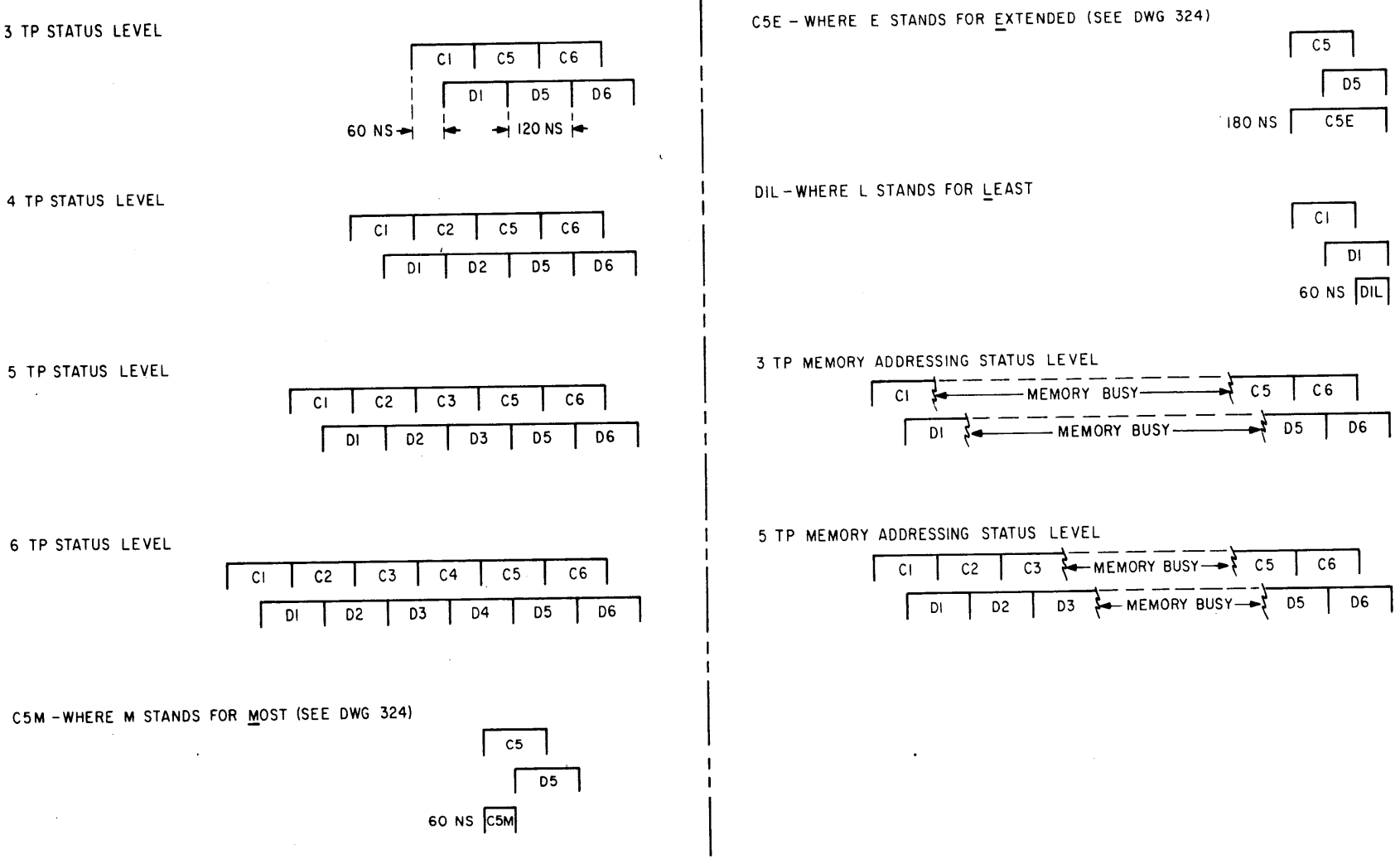
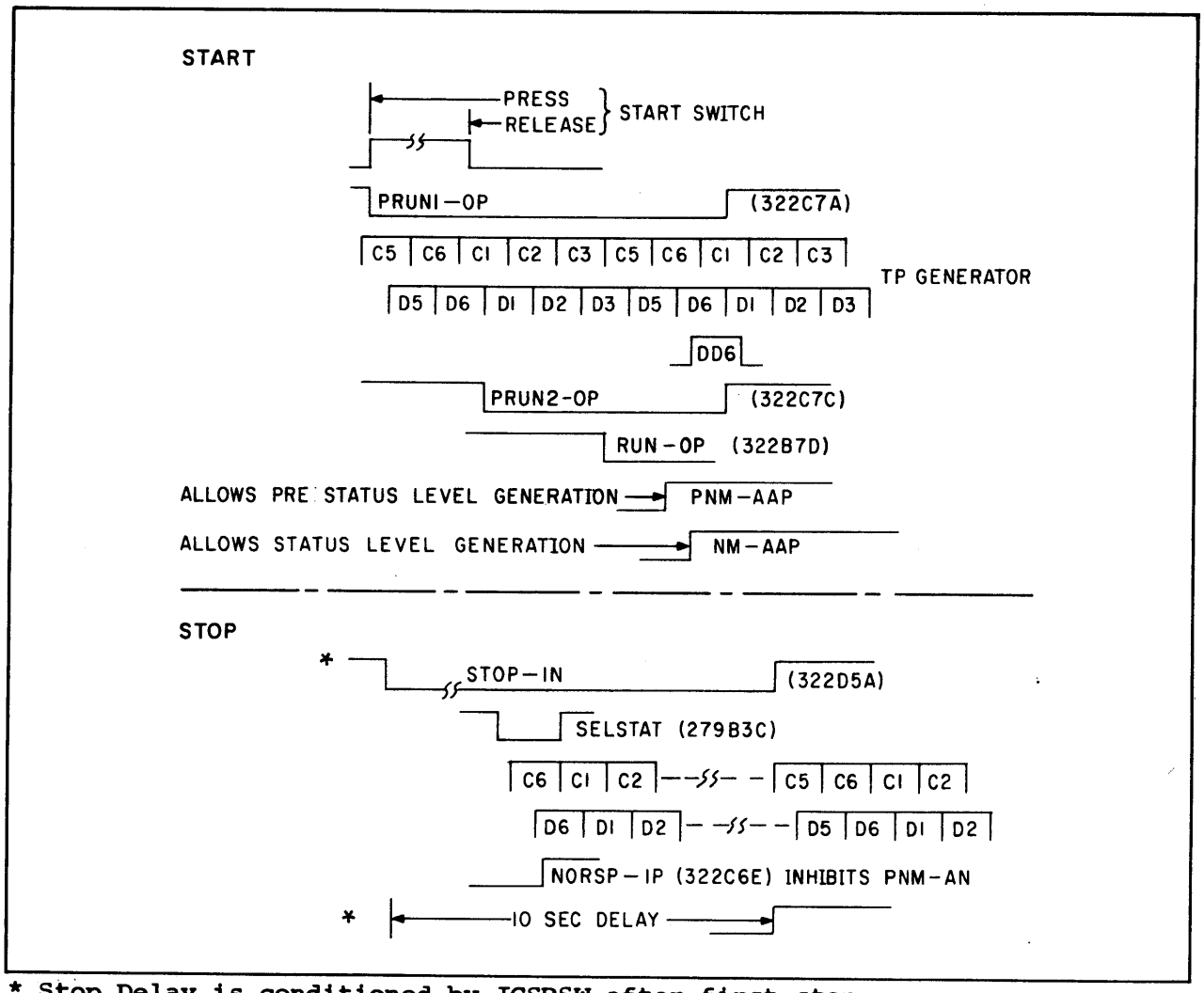


Figure 4-4. Timing Generator Pulses



*** Stop Delay is conditioned by ICSPSW after first stop**

FIGURE 4-5. START-STOP TIMING

3. Gate-B2A

   Inputs SECN and CLOSN will inhibit NM if either goes high. SECN (Set close normal) - This sets CLOSN flip-flop at DD6 time when PNM is inhibited. This signal inhibits NM a little sooner than CLOSN.

   CLOSN (Close normal) - This inhibits NM because PNM is inhibited.

4. Gate-D4B

   The output of this gate will set PXM (Pre-Multiplexor Mode), if multiplexor service interrupt occurs and no selector is busy or asking for service.

5. Gate-D5A

   This gate will set PXM, for each MUX servicing status level as long as MUX servicing is interrupted by Selector service.

6. Gate-B3A

   CLOSIO (Close I/O) - This inhibits XM (multiplexor mode) for HOLD and during snap-shot mode.

7. Gate-D6A

   This gate sets PSM (Pre-selector mode), whenever a selector channel requests service.

4.2.4.1 Priority of Operation

In priority of operation SM is first, XM is second and NM is last.

Whenever NM is interruptable, the processor can enter into SM or XM.

If the processor is in XM and SM is requested, then SM takes precedence. Hence, the processor has to be able to enter XM again after SM is done. This requirement is provided by the XAC flip-flop which enables XM after SM is completed.

4.2.5 OPERATION DECODING & INSTRUCTION GROUPS

The Op Decoders and Instruction (Inst.) Groups are found in the following Logic Diagrams.

Op Decoder I	3660283
Op Decoder II	3660284
Op Decoder III	3660285
Inst. Group I	3660286
Inst. Group II	3660287
Inst. Group III	3660288

The least significant four bits of OPR (Operation Register) (00-03) are decoded into 16 combinations (IX0 to IXF).

The most significant 4 bits of OPR (04-07) are also decoded into 16 combinations (I0X to IFX). X is used here as a filler character.

The outputs of (IX0 to IXF) with (I0X to IFX) are the various Op-codes. For example I83 = I8X · IX3.

Instructions are further grouped into IGXX's or groups as follows:

LD1 (286 - A6A) Load group 1 = I10 + I11 + I13 + I48

LD2 (286 - C8C) Load group 2 = I12 + I18 + I30 + I31 + I32 + I33 + I38

LD3 (286 - C7A) Load group 3 = I20 + I21 + I22 + I23 + I28

LD4 (286 - A5A) Load group 4 = I58 + I78

MACO (286 - C6B) Move numerics, Move Zone, Move, Logical AND, Logical OR, Compare Logical OR, and Exclusive OR = ID1 + ID2 + ID3 + ID4 + ID5 + ID6 + ID7

ASC (286 - C5A) Add/Subtract Word and Half Word, Add/Subtract Logical, Compare Word and Half Word = I1A + I1B + I1E + I1F + I4A + I4B + I5A + I5B + I5E + I5F + I19 + I49 + I59

BLOC (286 - C4B) Branch On Condition/Count, Branch and Link = I05 + I06 + I07 + I45 + I46 + I47

CAOE (286 - C4A) Logical AND/OR, Exclusive OR and Compare Logical = I14 + I15 + I16 + I17 + I54 + I55 + I56 + I57

ADD (286 - C1A) Add Normalized and Unnormalized = I2A + I3A + I6A + I7A + I2E + I3E + I6E + I7E

SUB (286 - B7B) Compare, Subtract Normalized and Unnormalized = I29 + I39 + I69 + I79 + I2B + I3B + I6B + I7B + I2F + I3F + I6F + I7F

FPA (286 - B8B) Floating Point Add - includes all Add/Subtract Normalized and Unnormalized and Compare = I29 + I2A + I2B + I2E + I2F + I39 + I3A + I3B + I3E + I3F + I69 + I6A + I6B + I6E + I6F + I79 + I7A + I7B + I7E + I7F

TMCA (286 - B6C) Test Under Mask, Move, Logical AND/OR, Exclusive Or and Compare Logical = I91 + I92 + I94 + I95 + I96 + I97

FPLS (286 - B6B) Floating Point Load and Store = I60 + I68 + I70 + I90 + I98

DAD (286 - B5A) Decimal Add = IF8 + IF9 + IFA + IFB

DIC (286 - B4A) Direct Control = I84 + I85

DMD (286 - B4B) Decimal Multiply/Divide = IFC + IFD

BOI (286 - B4C) Branch on Index High or Branch on Index Low or Equal = I86 + I87

DVD (286 - B3A) Divide (Fixed Point) = I1D + I5D

EDIT (286 - B3B) Edit or Edit and Mark = IDE + IDF

FPD (286 - B3C) Floating Point Divide = I2D + I3D + I6D + I7D

FPH (286 - B2A) Floating Point Halve = I24 + I34

TRAT (286 - B2A) Translate or Translator and Test = IDC + IDD

FPM (286 - B2B) Floating Point Multiply = I2C + I3C + I6C + I7C

IOINST (286 - A7A) Input Output Instructions I9C + I9D + I9E + I9F + Load Switch

LGFP (286 - A5B) Long Floating Point (Any) = I2X + I6X

MPU (286 - A5C) Moved with Offset, Pack, or Unpack = IF1 + IF2 + IF3

MPY (286 - A4A) Fixed Point Multiply = I1C + I4C + I5C

SLR (286 - A4B) Shift Left Single/Double, Shift Right Single/Double, Shift Left Single/Double Logical, and Shift Right Single/Double Logical = I88 + I89 + I8A + I8B + I8C + I8D + I8E + I8F

SPLS (286 - A4C) Scratch-Pad Load/Store = ID0 + ID8

RRFP (286 - A3A) RR (format) Floating Point = I2X + I3X

RXFW (286 - A3B) RX (format) Full Word I5X + I7X

MPC (286 - A3C) Memory Protect, Set Storage Key/Insert Storage Key = I08 + I09

With few exceptions, most of the IGXXs are formed by two or more inputs to an OR gate;

IG34 (287 - B3B) Load Positive/Negative/Complement = I20 + I21 + I23 + I30 + I31 + I33

IG42 (288 - D4A) Shift Left Single/Double = I8B + I8F

IG43 (288 - D4B) Add/Subtract Logical = I1E + I1F + I5E + I5F

IG47 (288 - D2B) Add/Subtract Word and Half Word, Compare Word and Half Word = I1A + I1B + I4A + I4B + I5A + I5B + I19 + I49 + I59

IG53 (288 - B5A) Floating Point Multiply (Short) = I3C + I7C

IG54 (288 - B5B) Add/Subtract Normalized (Short) = I3A + I3B + I7A + I7B

IG55 (288 - B4A) Add/Subtract Normalized (Long) = I2A + I2B + I6A + I6B

IG56 (288 - B4B) Floating Point Add/Subtract Unnormalized (Long) = I2E + I2F + I6E + I6F

IG58 (288 - B3B) Floating Point Divide (Long) = I2D + I6D

IG59 (288 - B2A) Floating Point Divide (Short) = I3D + I7D

IG60 (288 - B2B) Floating Point Add/Subtract Unnormalized (Short) = I3E + I3F + I7E + I7F

IG61 (288 - B1A) Floating Point Multiply (Long) = I2C + I6C

IG62 (288 - A8A) Fixed Point Multiply Word = I1C + I5C

IG71 (288 - A5A) Move, Move Numerics Move Zones = ID1 + ID2 + ID3

Instruction Formats (286-D3A)

Format	OPR 06	OPR 07
RR	0	0
RX	1	0
RS/SI	0	1
SS	1	1

4.2.6 STATUS LEVELS

The basic hardware control in the 70/55 Processor is the Status Level. The Status Level logic can be divided into two levels. They are the Pre Status Level logic (see NEXT STEP box in Figure 4-3) and the Status Level logic (see CURRENT STEP box in Figure 4-3).

4.2.6.1 Status Level Decoding

The 70/55 Status Levels may be divided into three groups. The mode is determined by the Processor Interrupt.

1. Normal Mode Status Levels (NM)

2. Multiplexor Mode Status Levels (XM)

3. Selector Mode Status Levels (SM)

Multiplexor and Selector Modes will be discussed in I/O description. Table 4-1 shows many of the normal mode status levels. It identifies them by a type designation, the bit configuration shown in the status level register display and also gives an abbreviated description of its standard function.

Meanings of the status level designation are as follows:

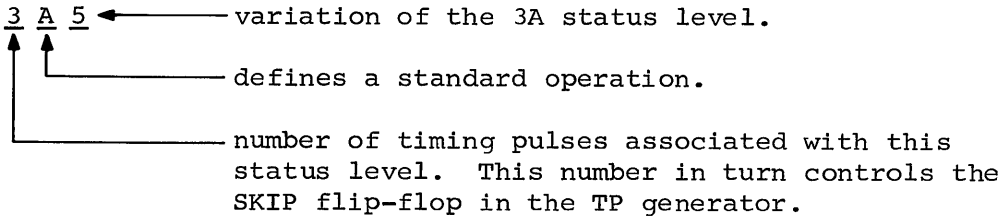


Table 4-1. Normal Mode Status Levels

Type	PSTLR/STLR Bit Display 7 6 5 4 3 2 1 0	Standard Function
3A(0-15)	1 0 0 0 0 0 X X	Result of operation to scratch pad.
	1 0 0 0 0 1 X X	" " " " " "
	1 0 0 0 1 0 X X	" " " " " "
	1 0 0 0 1 1 X X	" " " " " "
	1 0 0 1 0 0 X X	" " " " " "
	1 0 0 1 0 1 X X	" " " " " "
	1 0 0 1 1 0 X X	" " " " " "
	1 0 0 1 1 1 X X	" " " " " "
3B(0-15)	1 0 1 0 0 0 X X	Result of operation does not go to Scratch Pad.
	1 0 1 0 0 1 X X	
	1 0 1 0 1 0 X X	" " " " " " " "
	1 0 1 0 1 1 X X	" " " " " " " "
3C(0-15)	1 0 1 1 0 0 X X	Sum (or scratch pad) to register; DR to scratch pad.
	1 0 1 1 0 1 X X	
	1 0 1 1 1 0 X X	" " " " " " " "
	1 0 1 1 1 1 X X	" " " " " " " "
3D(0-7)	1 1 0 0 0 0 X X	Main Memory to DR; DR to scratch pad.
	1 1 0 0 0 1 X X	" " " " " " " "
3E(0-3)	1 1 0 0 1 0 X X	Store DR in Main Memory
3F(0-3)	1 1 0 0 1 1 X X	Staticizing
3G(0-3)	1 1 0 1 0 0 X X	Staticizing
3H(0-3)	1 1 0 1 0 1 X X	Interrupt routine
3X(0-3)	1 1 1 0 0 0 X X	Three pulse Memory Addressing
3Y(0-3)	1 1 1 0 1 0 X X	Three pulse Shaded Memory Addressing (or for standard locations)
4A(0-15)	0 1 0 0 0 0 X X	Result of operation to scratch pad.
	0 1 0 0 0 1 X X	" " " " " "
	0 1 0 0 1 0 X X	" " " " " "
	0 1 0 0 1 1 X X	" " " " " "
4B(0-7)	0 1 0 1 0 0 X X	Result of operation does not go to scratch pad.
	0 1 0 1 0 1 X X	
4C(0-3)	0 1 0 1 1 0 X X	Transfer to DR; result to scratch pad.
4D(0-3)	0 1 0 1 1 1 X X	Store IR
4E(0-3)	0 1 1 0 1 0 X X	Staticizing
4F(0-3)	0 1 1 0 0 1 X X	Staticizing
4G(0-3)	0 1 1 0 0 0 X X	Interrupt routine
5A(0-7)	0 0 0 0 1 0 X X	Scratch pad to scratch pad transfer
	0 0 0 0 1 1 X X	" " " " " "
5B(0-7)	0 0 0 1 0 0 X X	Non Memory Addressing five pulse status levels.
	0 0 0 1 0 1 X X	
5C(0-3)	0 0 0 0 0 1 X X	Staticizing
5D(0-3)	0 0 0 1 1 0 X X	Interrupt routine
5E(0-3)	0 0 0 1 1 1 X X	Five pulse I/O cycle
5X(0-3)	0 0 1 0 0 0 X X	Staticizing
5Y(0-3)	0 0 1 0 0 1 X X	Five pulse Memory Read cycle
5Z(0-3)	0 0 1 0 1 0 X X	Five pulse Memory Write cycle
	0 0 1 0 1 1 X X	" " " " "
6A(0-3)	0 0 1 1 0 0 X X	Six pulse status level with Scratch Pad Addressing
6B(0-3)	0 0 1 1 0 1 X X	Six pulse status level with no Scratch Pad Addressing

NOTE: XX = 01 = 1 XX = 11 = 3
= 10 = 2 = 00 = 4

4.2.6.2 Status Level Encoding

The Status Level Codes are generated as the results of the operation code, the previous status level and hardware conditions.

The status level encoder primes the bits needed to set the PSTLR (Pre-Status Level Register).

The status level select signals (shown on logic drawings 297-299) fall into one of four categories.

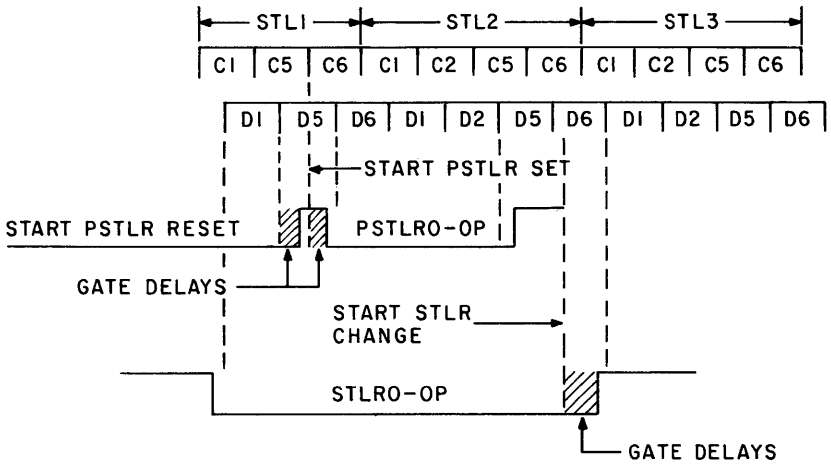
1. SXX3A1; this signal is a combination of a scratch pad address and a status level. The XX characters mean that the actual scratch pad address setting is not relevant.

2. S103A1; this signal is also a combination of a scratch pad address and a status level, but in this case the SPA must be 10 to generate this signal.

3. FPM3A14; this signal combines an operation code and a status level. This example uses Floating Point Multiply.

4. IG103C2; this signal is a combination of an instruction group (10) and a status level.

The status level timing chart is shown below.



The Status Level Display indicators on the Maintenance Panel are used for troubleshooting or debugging. This register can be read as a two digit hexadecimal number. Using the charts on the following page, and the Mode Indicators (NM = Normal, XM = Multiplexor and SM = Selector) the Status Level can be identified. Care must be exercised when using the Status Level Reset switch. This switch will reset the NM Status Level, even if the XM or SM indicator is lit.

STATUS LEVEL CHART - NORMAL

LEAST SIGNIFICANT DIGIT

MOST SIGNIFICANT DIGIT

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0					5C 4	1	2	3	5A 4	1	2	3	8	5	6	7
1	5B 4	1	2	3	8	5	6	7	5D 4	1	2	3	5E 4	1	2	3
2	5X 4	1	2	3	5Y 4	1	2	3	5Z 4	1	2	3	8	5	6	7
3	6A 4	1	2	3	6B 4	1	2	3								
4	4A 4	1	2	3	8	5	6	7	12	9	10	11	16	13	14	15
5	4B 4	1	2	3	8	5	6	7	4C 4	1	2	3	4D 4	1	2	3
6	4G 4	1	2	3	4F 4	1	2	3	4E 4	1	2	3				
7																
8	3A 4	1	2	3	8	5	6	7	12	9	10	11	16	13	14	15
9	3A 20	17	18	19	24	21	22	23	28	25	26	27	32	29	30	31
A	3B 4	1	2	3	8	5	6	7	12	9	10	11	16	13	14	15
B	3C 4	1	2	3	8	5	6	7	12	9	10	11	16	13	14	15
C	3D 4	1	2	3	8	5	6	7	3E 4	1	2	3	3F 4	1	2	3
D	3G 4	1	2	3	3H 4	1	2	3								
E	3X 4	1	2	3					3Y 4	1	2	3				
F																

STATUS LEVEL CHART - MULTIPLEXOR

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0					5BM 1	2	3	4	5AM 0				5ZM 1	2		
1	6AM 1	2			4AM 1	2			4BM 1	2			4DM 1	2	3	4
2	3AM 1		3						3BM 1	2						
3									3YM 1	2	3	4	5			

STATUS LEVEL CHART - SELECTOR

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0					5AS 5				5BS 1	2	3		6AS 1	2	3	
1	4DS 1	2	3	4									4BS 1			
2	3AS 1		3						3ES 1							
3	5ZS 1	2	3	4					4AS 1	2	3	4	5			

4.2.7 SCRATCH PAD (FAST MEMORY) OPERATION

The Scratch Pad Memory in the 70/55 Processor can be described as the center of operations. The name Fast Memory is also used, therefore the names assigned to logic signals can contain "SP" for Scratch Pad or "FM" for Fast Memory.

The timing sequence of Scratch Pad addressing is shown in Figure 4-6.

The SPA register is jammed with the correct bits at C2/C6 time. Actual Scratch Pad Memory addressing occurs at D2/D6 time. Logic drawing 302 shows the Scratch Pad addressing decoder whose output goes to the FM Address Register.

4.2.7.1 Scratch Pad Addressing

Logic drawing 300 shows the signals (SSPAXX-P) which are encoded to set the correct flip-flop of the SPA (drawing 301). To simplify this discussion, the SPA register is divided into two digits as follows:

SPA04, SPA03 = Most significant digit

SPA02, SPA01, SPA00 = Least significant digit

Table 4-2 shows the means of generating the Scratch Pad address, when operating in the Normal Mode.

On the first line of Table 4-2; when the SPA register contains the configuration $(01)_8$, then the Scratch Pad address (output of the FM Address decoder) is a function of the N Counter. Any portion of the Scratch Pad can be addressed (00-F7) in this manner.

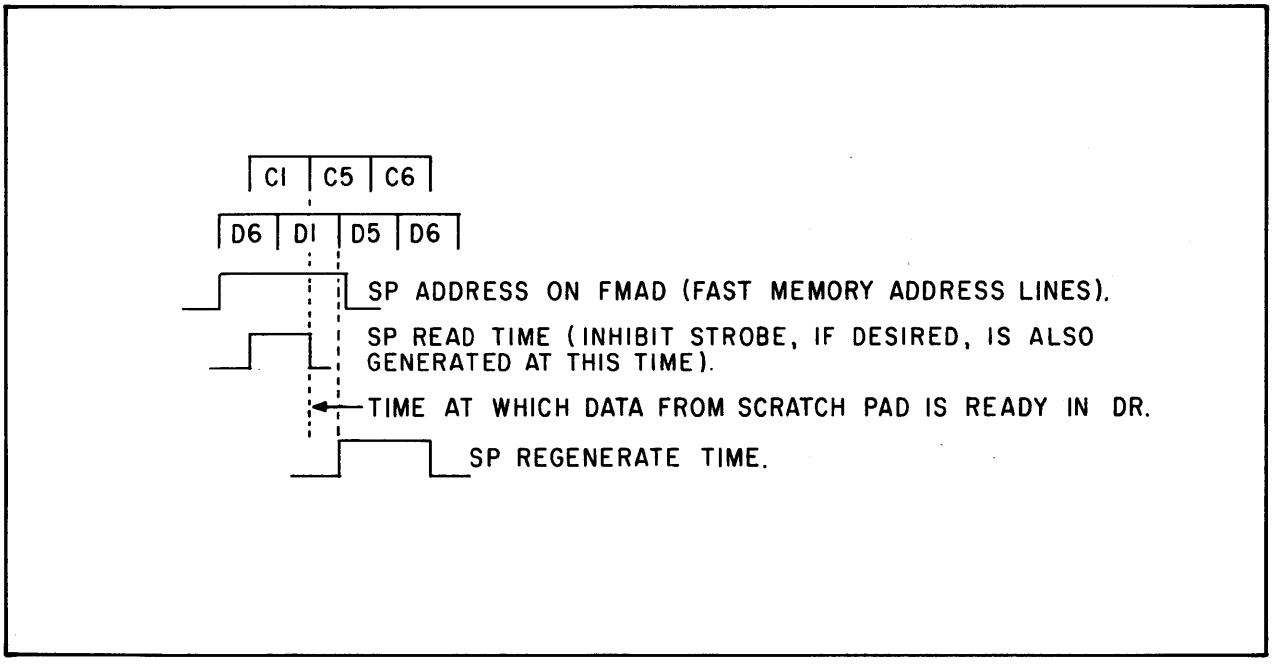


Figure 4-6. Scratch Pad Timing

Table 4-2. Scratch Pad Memory Address Generation

Selected Address	SPA REG 04	03	02-00	SPA FF $( )_8$	FM ADDRESS DECODER OUTPUTS (302) FMAD6	FMAD5	FMAD4	FMAD3	FMAD2	FMAD1	FMAD0
00-7F	0	0	001	01	NC06	NC05	NC04	NC03	NC02	NC01	NC00
E0-E7	0	0	010	02	1	1	1	0**	GPM02	GPM01	GPM00
E0-E7	0	0	011	03	1	1	1	0*	GPL02	GPL01	GPL00
02-05(NM-CTR)	0	0	100	04	0	0	0	0	NC05	$\overline{\text{NC05}}$	NC04
NIO SP	0	0	101	05	SPIT2	SPIT1	1	SPIT0	NC05	$\overline{\text{NC05}}$	NC04
70 (PAR)	0	0	110	06	0	1	1	1	0	0	0
43 (IF)	0	0	111	07	0	1	0	0	0	1	1
00 (UTY1)	0	1	000	10	0	0	0	0	0	0	0
01 (UTY2)	0	1	001	11	0	0	0	0	0	0	1
60 (UTY9)	0	1	010	12	0	1	1	0	0	0	0
61 (UTY10)	0	1	011	13	0	1	1	0	0	0	1
06 (D1A)	0	1	100	14	0	0	0	0	1	1	0
07 (D2A)	0	1	101	15	0	0	0	0	1	1	1
A0 (UTY11)	0	1	110	16	1	0	1	0	0	0	0
A1 (UTY12)	0	1	111	17	1	0	1	0	0	0	1
GPR's	1	0	000	20	PSR01	PSR00	0	GPM03	GPM02	GPM01	GPM00
ODD GPR's	1	0	001	21	PSR01	PSR00	0	GPM03	GPM02	GPM01	1
GPR's	1	0	010	22	PSR01	PSR00	0	GPL03	GPL02	GPL01	GPL00
ODD GPR's	1	0	011	23	PSR01	PSR00	0	GPL03	GPL02	GPL01	1
INT. MASK	1	1	000	30	0	if P4	0	$\overline{\text{PSR01}}$	$\overline{\text{PSR00}}$	0	0
INT.STATUS	1	1	001	31	0	if P4	0	$\overline{\text{PSR01}}$	$\overline{\text{PSR00}}$	0	1
PC	1	1	010	32	0	if P4	0	$\overline{\text{PSR01}}$	$\overline{\text{PSR00}}$	1	0
GR00	1	0	100	24	PSR01	PSR00	0	P1/P2=00; P3=11;P4=10		0	0
GR01	1	0	101	25	PSR01	PSR00	0	"	"	0	1
GR02	1	0	110	26	PSR01	PSR00	0	"	"	1	0
GR03	1	0	111	27	PSR01	PSR00	0	"	"	1	1

NOTES:
** GPM03 must be 0
* GPL03 must be 0

To simplify the decoding, the following bit relations are true:

SPA 2^4=0, FM Address is not a function of PSR.

SPA $2^4 2^3$=10, PSR generates 2^6 and 2^5 of the FM Address.

SPA $2^4 2^3$=11, PSR generates 2^5, 2^3 and 2^2 of the FM Address.

PSR, the Program State Register is interpreted as follows:

PSR01	PSR00	Program State
1	1	1
1	0	2
0	1	3
0	0	4

NIOSP is used in the Normal mode to address that portion of Scratch Pad associated with the I/O channels. This addressing is a function of the IT (Initiate/Terminate) register. See drawing 333.

The Scratch Pad can also be addressed by the MSPA register (in the Multiplexor Mode) or the SLSPA register (in the Selector Mode). These modes will be discussed in Sections 4.3.3 and 4.3.12.

Manual addressing of the Scratch Pad will be discussed in 4.2.10, Manual Operations.

4.2.8 COMMAND GENERATOR

The Command Generator (logic drawings 245 through 258) is the block of logic that controls the various operations of the processor. The Command Generator inputs are timing pulses, op-code status level combinations and control flip-flop outputs. Outputs of the command generator control the reset, read-in and triggering for all the registers, the functioning of the arithmetic unit, the gating onto the bus and the commands for the memories.

4.2.8.1 Adder Commands

BAA (245-C8A) - Binary Add Address - The contents of register DR (32 bits) is added to the contents of register UR (12 bits).

UR is a function of UCAD as follows: (DCAD ignored)

UR (00-11) if UCAD = 100
UR (16-27) if UCAD = 000

BAH (245-C7B) - Binary Add Half Word - The contents of register DR (32 bits) is added to the contents of register UR (16 bits).

UR is a function of UCAD as follows: (DCAD ignored)

UR (00-15) if UCAD = 100
UR (16-32) if UCAD = 000

BAK (245-C6A) - Binary Add Character - This command is used only for floating point Multiply/Divide instruction. The contents of register DR (8 bits) is added to the contents of register UR (8 bits).

DR is a function of DCAD
UR is a function of UCAD

BAX1 (245-C6B) - Binary Add DR (+1),

Increment the contents of register DR by 1. DCAD and UCAD ignored.

BAX2 (245-D6B) - Binary Add DR (+2),

Increment the contents of register DR by 2. DCAD and UCAD ignored.

BAX4 (245-C5A) - Binary Add DR (+4),

Increment the contents of register DR by 4. DCAD and UCAD ignored.

BSH (245-C3A) - Binary Subtract Half Word - The contents of register UR (16 bits) is subtracted from the contents of register DR (32 bits). UR is a function of UCAD as follows: (DCAD ignored)

UR (00-15) if UCAD = 100
UR (16-31) if UCAD = 000

BSK (245-C3C) - Binary Subtract Character - This command is used primarily for comparison. The contents of register UR (8 bits) is subtracted from the contents of register DR (8 bits).

DR is a function of DCAD
UR is a function of UCAD

BAW (245-C2A) - Binary Add Word - The contents of register DR (32 bits is added to the contents of register UR (32 bits). DCAD and UCAD ignored.

LAW (245-B8A) - Logical And Word - This command is used to logical AND the contents of register UR (32 bits) to the contents of register DR (32 bits). DCAD and UCAD ignored.

BSW (245-B7A) - Binary Subtract Word - The contents of register UR (32 bits) is subtracted from the contents of register DR (32 bits). DCAD and UCAD ignored.

BSX1 (245-B7C) - Binary Subtract DR (-1),

Decrement the contents of register DR by 1. DCAD and UCAD ignored.

BSX2 (245-B6B) - Binary Subtract DR (-2),

Decrement the contents of register DR by 2. DCAD and UCAD ignored.

BSX4 (245-B5C) - Binary Subtract DR (-4),

Decrement the contents of register DR by 4. DCAD and UCAD ignored.

EOK (245-B5D) - Exclusive Or Character,

Exclusive OR the contents register DR (8 bits) with the contents of register UR (8 bits).

DR is a function of DCAD
UR is a function of UCAD

EOW (245-B4A) - Exclusive Or Word,

Exclusive OR the contents of register DR (32 bits) with the contents of register UR (32 bits). DCAD ignored.

DAK (245-B4B) - Decimal Add Character,

Decimal add the contents of register DR (8 bits) with the contents of register UR (8 bits).

DR is a function of DCAD
UR is a function of UCAD

DIW (245-B4C) - Decimal Add Inverse Word,

Decimal add the contents of register DR (32 bits) with the complemented contents of the register UR (32 bits). DCAD and UCAD ignored.

DAW (245-B3C) - Decimal Add Word,

Decimal Add the contents of register DR (32 bits) with the contents of register UR (32 bits).

DIK (245-B2A) - Decimal Add Inverse Character,

Decimal Add the contents of register DR (8 bits) with the complemented contents of register UR (8 bits).

DR is a function of DCAD
UR is a function of UCAD

INOD (245-B2B) - Inhibit Odd Digit - This command is used to inhibit the odd digit for the first time through during execution of Decimal Add/Subtract/Compare or Zero & Add instructions.

INXC0 (245-B2C) - Inhibit DR Character C0.

Inhibit the read out of Character C0.

LAK (245-B1A) - Logical And Character,

Used to Logical AND the contents of register DR (8 bits) with the contents of register UR (8 bits).

DR is a function of DCAD
UR is a function of UCAD

LAIW (246-D8A) - Logical And Inverse Word,

Used to Logical AND the contents of register DR (32 bits) with the complemented contents of register UR (32 bits). DCAD ignored.

LOK (246-D8B) - Logical Or Character,

Used to Logical OR the contents of register DR (8 bits) with the contents of register UR (8 bits).

DR is a function of DCAD
UR is a function of UCAD

LOW (246-D7B) - Logical Or Word,

Used to Logical OR the contents of register DR (32 bits) with contents of register UR (32 bits). DCAD and UCAD ignored.

TCYW (246-D7C) - Transfer twos complement UR Word,

The contents of register UR (32 bits) is twos complemented and transferred onto the Sum (S) bus (00-31). DCAD and UCAD ignored.

TIYW (246-D6D) - Transfer Inverse UR Word,

The contents of register UR (32 bits) is complemented and transferred onto the Sum (S) bus (00-31). DCAD and UCAD ignored.

TTXD (246-D5A) - Transfer True DR Digit,

The contents of register DR (4 bits) is transferred onto sum (S) bus. DR is a function of DCAD and also:

If DCAD is odd (DDOD) - DR (4 bits) to S bus (00-03).
If DCAD is even (DDEV) - DR (4 bits) to S bus (04-07).

TTXK (246-D4B) - Transfer True DR Character,

The contents of register DR (8 bits) is transferred onto the sum (S) bus (00-07). UCAD ignored.

DR is a function of DCAD

TTXW (246-B2A) - Transfer True DR Word,

The contents of register DR (32 bits) is transferred onto the sum (S) bus (00-31). DCAD and UCAD ignored.

TTYH (246-B8A) - Transfer True UR Half Word,

The contents of register UR (16 bits) is transferred onto the sum (S) bus (00-15). DCAD ignored.

UR (00-15) if UCAD = 100
UR (16-31) if UCAD = 000

TTYK (246-B7C) - Transfer True UR Character,

The contents of register UR (8 bits) is transferred onto the sum (S) bus (00-07). DCAD ignored.

UR is a function of UCAD

TTYW (246-B4A) - Transfer True UR Word,

The contents of register UR (32 bits) is transferred onto the sum (S) bus (00-31). DCAD and UCAD ignored.

TTYD (246-B4C) - Transfer True UR Digit,

The contents UR (4 bits) is transferred onto sum (S) bus. UR is a function of UCAD and also: (DCAD ignored)

If UCAD is odd (UDOD) - UR (4 bits) to S bus (00-03).
If UCAD is even (UDEV) - UR (4 bits) to S bus (04-07).

4.2.8.2 Bus Commands

RODIAGC (247-C8A) - Read out Diagnostic,

Readout Diagnostic counter (00-04) onto the IB (02-06)..

RODRW (247-C3B) - Read out Data Register Word,

Readout the X Bus (00-31) onto the IB (00-31).

ROGP (247-C3C) - Readout General Purpose Least and Most,

Readout the contents of register GPL (00-03) onto IB (00-03) and GPM (00-03) onto IB (04-07).

ROGPL (247-C2A) - Readout General Purpose Least,

Readout the contents of register GPL (00-03) onto IB (00-03).

ROGPM (247-B7B) - Readout General Purpose Most,

Readout the contents of register GPM (00-03) onto IB (00-03).

ROGPR (247-B6A) - Readout General Purpose Register,

Readout the contents of register GPR (00-03) onto IB (00-03).

ROIN (247-B6B) - Readout Interrupt Bits,

Readout the contents of various interrupt registers onto the IB.

PF - Power Failure - 00

PEEX - Fast & Main Memory Parity Error - 01

EXS (1-6) - External Signal - (02-07)

S (1-6) - Selectors Interrupt - (09-14)

MINT - Multiplexor Channel Interrupt - 15

ETEX - Elapsed Time Clock - 16

COIN - Console Interrupt Request - 17

SCEX - Supervisor Call Instruction - 20

POEX - Privileged Operation - 21

OCEX - Op-Code Trap - 22

ADEX - Address Error - 23

DEX - Data Error - 24

EOEX - Exponent Overflow - 25

DIEX - Divide Error - 26

SEEX - Significant Error - 27

EUEX - Exponent Underflow - 28

DOEX - Decimal Overflow - 29

OVEX - Fixed Point Overflow - 30

DM - Test Mode - 31

ROKA (247-B6C) - Readout Key Register and American Standard Interchange.

The contents of the following registers are readout onto the IB:

IC - Initial Carry - 09

FC - Final Carry - 10

MDR 00-02 - Decimal Multiply & Divide Register - (12-14)

A - American Standard Interchange Mode - 19

KR 00-03 - Memory Protect Key - (20-23)

ROIRW (247-B5E) - Readout Intermediate Register Word,

Readout the contents of register IR (32 bits) onto the IB (00-31).

ROMRW (248-C4A) - Readout Main Memory Word,

Readout the contents of MM register (32 bits) onto the IB (00-31).

ROMSC (248-C2B) - Readout Miscellaneous,

Readout the contents of Miscellaneous registers onto the IB,

PMR 00-03 - Program Mask Register - (24-27)

CCR 00-01 - Condition Code Register - (28-29)

ILC 1,2 - Instruction Length Register - (30,31)

ROOPR (248-C2B) - Readout Op Code Register,

The contents of GPL, GPM, OPR, DCAD, UCAD are readout onto the IB,

GPL 00-03 - General Purpose Least - (00-03)

GPM 00-03 - General Purpose Most - (04-07)

OPR 00-07 - Op-Code Register - (08-15)

DCAD 00-02 - DR Character Address - (17-19)

UCAD 00-02 - UR Character Address - (21-23)

ROMXKCR (248-B8A) - Readout Multiplexor Channel Key & Command Registers onto IB.

COM 24-27 - Command - (24-27)

MKEY 0-3 - Multiplex Keys - (28-31)

ROMXNAD (248-B7B) - Readout Initiation Register and N-Counter,

The contents of INR and N Counters are readout onto the IB,

INR 00-05 - Initiation Register - (02-07)

INR 06,07 - Initiation Register - (12-13)

N Ctr 00-01 - N Counter - (14-15)

ROMSIR (248-B6B) - Readout Miscellaneous and Intermediate Register,

The contents of Miscellaneous Registers and IR are readout onto the IB.

ILC 1,2 - Instruction Length Register - (30-31)

CCR 00,01 - Condition Code Register - (28-29)

PMR 00-03 - Program Mask Register - (24-27)

IR 00-23 - IR Register - (00-23)

RONCCO (248-B5A) - Readout N Counter,

The 7-bit N Counter is readout onto the IB.

N 00-06 - N Counter - (24-30)

RONCC3 (248-B5B) - Readout N Counter,

The first 4 bits of the N Counter is readout onto the IB.

N 00-03 - N Counter - (04-07)

RODNCC3 (248-B4B) - Readout Decoded N Counter,

The N Counter is decoded and readout onto the IB.

N (00-03) - N Counter - (04-07)

ROPSR (248-B3A) - Readout Program State Register,

The contents of PSR is readout onto the IB.

PSR (00-01) - Program State Register - (29-30)

FMPE - Fast Memory Parity Error - 24

MMPE - Main Memory Parity Error - 25

ROSTR (248-B2A) - Readout Status Registers,

The contents of these various registers are readout onto the IB.

CFF (1-8) - Control Flip Flop - (00-07)

CFF (10-11) - Control Flip Flop - (09-10)

RSM - Result Sign Minus - 11

DS - DR Sign - 12

ZFF - Zero Flip Flop - 13

FTT1 - First Time Through - 14

FTT2 - Second Time Through - 15

STLR (0-7) - Status Level Register - (16-23)

PSLR (0-7) - Pre Status Level Register - (24-31)

4.2.8.3 DR & DC Commands

RDC (249-D7D) - Reset DCAD

RDRW (249-D6D) - Reset DR Word (32 bits)

SDCB (249-D5E) - Select DCAD Byte Address,

IB (00,01) to DCAD (01,02)

SDC7 (249-D4C) - Set all bits in DCAD. Set DCAD (00-02)

SDRC0 (249-D4D) - Select DR Character C0,

IB (24-31) to DR (24-31). Remaining bits unchanged.

SDRC3 (249-D1B) - Select DR Character C3,

IB (00-07) to DR (00-07). Remaining bits unchanged.

SDRK (249-B8A) - Select DR Character,

IB (8 bits) reads into DR (8 bits).

DR is a function of IOU (Input/Output). Remaining bits unchanged.

SDRW (249-B7D) - Select DR Word,

IB (32 bits) to DR (32 bits).

TDCD1 (249-B6B) - Trigger DCAD Down 1.

TDCD2 (249-B6C) - Trigger DCAD Down 2.

TDCU1 (249-B5E) - Trigger DCAD Up 1.

TDCU2 (249-B4D) - Trigger DCAD Up 2.

4.2.8.4 GC & GR Commands

RGPM (250-C8A) - Reset General Purpose Most Register.

RGPR (250-C8B) - Reset General Purpose Register.

SGPRL1 (250-C7C) - Select GPR Left 1,

Select bit 31 from Sum bus to GPR 00.

SGPL1 (250-C6B) - Set GPL to $(1)_{16}$. Set GPL 00.

SGPL3 (250-C6C) - Set GPL to $(3)_{16}$. Set GPL 00 & GPL 01.

SGPL17 (250-C5A) - Set GPL to $(F)_{16}$. Set GPL (00-03).

SGPM (250-C5B) - Select GPM. Select the Y collected (04-07) to GPM (00-03).

SGPRL4-P (250-C4B) - Select GPR Left 4, Select bit (28-31) from Sum bus to GPR (00-03).

SGPR11 (250-C3A) - Set GPR to $(9)_{16}$. Set GPR 00 & GPR 03.

SGPRR1 (250-C3C) - Select GPR Right 1. Select bit 00 from Sum bus to GPR 03.

SGPRR2 (250-B8B) - Select GPR Right 2. Select bit (00-01) from Sum bus to GPR (02,03).

SGPRR4 (250-B8C) - Select GPR Right 4. Select bit (00-03) from Sum bus to GPR (00-03).

TGPLD1 (250-B6D) - Trigger GPL Down 1.

TGPLU1 (250-B6E) - Trigger GPL Up 1.

TGPMD1 (250-B5D) - Trigger GPM Down 1.

TGPMGPR (250-B4C) - Transfer GPM to GPR. The contents of GPM (00-03) is transferred to GPR (00-03).

TGPMLD1 (250-B4D) - Trigger GPM & GPL Down 1.

TGPMU1 (250-B3D) - Trigger GPM Up 1.

TGPRD1 (250-B3E) - Trigger GPR Down 1.

TLIRGPR (250-B1B) - Transfer Lower IR 31 to GPR 00.

4.2.8.5 IR Commands

DIRD (251-C8A) - Distribute IR Digit,

The Sum (S) bus (00-07) is distributed into IR as a function of DCAD & Digit.

DIRK (251-C7C) - Distribute IR Character,

The Sum (S) bus (00-07) is distributed into IR (00-07) as a function of DCAD.

EIRL (251-D5A) - Exchange IR Left,

The Sum (S) bus (00-03) is read into IR (04-07).

EIIR (251-D5B) - Exchange IR Right,

The Sum (S) bus (04-07) is read into IR (00-03).

GIRQ (251-C4B) - Generate IR Quotient,

This command sets IR 00 during the execution of either fixed/floating divide instructions.

GMZN (251-C3A) - Generate Most Zone,

This command generates either $(F)_{16}$ or $(5)_{16}$ into IR (04-07). The zone is a function of A register (American Standard Interchange Mode).

GSL (251-C3B) - Generate Sign Least,

This command generates a sign digit (+/-) into IR (00-03). The sign digit is a function of A register (American Standard Interchange Mode).

RIRW (251-C1A) - Reset IR Word,

This command resets IR (32 bits).

SIRK (251-A8B) - Select IR Character,

This command reads Sum (S) bus (00-31) into IR (00-31) except the character specified by DCAD.

SIRR1 (251-A6A) - Select IR Right 1,

The command resets IR 31 only and permits SSS00 read into IR 31.

SIRR2 (251-A6B) - Select IR Right 2,

This command resets IR (30-31) only, and permits SSS(00-01) read into IR (30-31).

SRIR (251-A6C) - Shift Right IR,

The lower IR (LIR) (02-31) is shifted right by 2 bits into IR (00-29).

SIRW (251-A6C) - Select IR Word,

The Sum (S) bus (00-31) read into IR (00-31).

SLIR (251-A3A) - Shift Left IR,

The lower IR (LIR) (00-30) is shifted Left by 1 bit in IR (01-31).

JAIR (251-A3C) - Jam IR,

This command is used to reset and set lower IR (LIR).

TIRK (251-A8B) - Transfer IR Character,

The Sum (S) bus (00-07) is read into IR (00-07) and IR (08-31) is reset.

PIRD (251-B2A) - Permit IR Decimal,

The Sum (S) bus (00-07) is permitted to read into IR decimally corrected.

GINVA (251-B2B) - Generate Interrupt Value to read into IR (02-06).

SIRFC (251-B1A) - Select IR from Operator's Console,

This command reads the setting of Digit switches from the operator's console into IR (00-10) during the "LOAD" function.

STSIRW (251-CD4) - Select bytes 1, 2, and 3 of IR word during staticizing. The SUM(S) BUS (08-31) read into IR (08-31)

4.2.8.6 N Counter Command

RNLC (252-C8A) - Reset N Least,

This command resets N (00-03).

SCCPMR (252-C7C) - Select Condition Code and Program Mask Register,

IB (24-27) is read into PMR (00-03) and IB (28-29) is read into CCR (00-01).

SPSR (252-C6A) - Select Program State Register,

IB (29-30) is read into PSR (00-01).

SETPSR (252-C6B) - Set Program State Register,

This command sets PSR00 only during the interrupt sequence.

SKAR (252-C5C) - Select Key and A Registers,

This command reads out the contents of DR into the following registers:

DR 16 - NPRIV - Nonprivileged

DR 19 - A - American Standard Interchange Mode Flip-Flop

DR (20-23) - KR (00-03) - Key Register

SOPHW (252-C5D) - Select Op-code Half Word,

This command permits the following:

Y(00-03) to GPL (00-03)

Y(04-07) to GPM (00-03)

Y(08-15) to OPR (00-07)

ROPR (252-C4B) - Reset Op-Code Register.

RNMC (252-C3A) - Reset N Most Counter,

This command resets N (04-06).

SNCC0 (252-C2A) - Select Character C0 to N,

IB (24-30) is read into N (00-06).

SNCC3 (252-B8C) - Select Character C3 to N,

IB (00-06) is read into N (00-06).

SNC4 (252-B7C) - Set N Counter to $(4)_{16}$,

This command sets N02.

SNC3 (252-B7E) - Set N Counter to $(3)_{16}$,

This command sets N (00-01).

SNC40 (252-B6D) - Set N Counter to $(20)_{16}$,

This command sets N05.

SNC144 (252-B6E) - Set N Counter to $(144)_{8}$,

This command sets N (00-06).

SNCD (252-B5D) - Select Least Significant of N,

IB (00-03) is read into N (00-03).

SNMC2 (252-B4E) - Set N Most Counter to $(2)_{16}$,

This command sets N05.

SNMC1 (252-B2C) - Set N Most Counter to $(1)_{16}$,

This command sets N04.

TNCD1 (253-C8A) - Trigger N Counter Down 1.

TNCD2 (253-C5A) - Trigger N Counter Down 2.

TNCD4 (253-C4A) - Trigger N Counter Down 4.

TNCD16 (253-C3A) - Trigger N Counter Down 16.

TNCU1 (253-B8D) - Trigger N Counter Up 1.

TNCU16 (253-B4B) - Trigger N Counter Up 16.

REMDR (253-A4A) - Reset Decimal Multiply; Divide Register.

TRNMMDR (253-A3A) - Transfer N Most Counter to Decimal Multiply; Divide,

This command transfers N (04-06) to MDR (00-02).

TRMDNMC (253-B2B) - Transfer Decimal Multiply; Divide Register to N Most Counter,

This command transfers MDR (00-02) to N (04-06).

4.2.8.7 Regenerate Matrix Commands

GEPA (254-D8B) - Generate Parity.

RGBA (254-D6A) - Regenerate Binary Sum Arithmetic,

This command allows the sum (00-30) to be regenerated.

RGBS (254-D5C) - Regenerate Binary Result Sign,

This command allows the sign bit (31) to be regenerated.

RGDW (254-D4B) - Regenerate Decimal Sum Word.

RGS123 (254-D3B) - Regenerate Binary Sum C_1 C_2 & C_3.

RGBW (254-C8C) - Regenerate Binary Sum Word.

ROSCSR (254-C4A) - Readout Selector/Multiplexor Channel Status Registers,

This command reads out the Selector/Multiplexor Channel Status Registers into fast memory C_1 position.

RGX0027 (254-C4B) - Regenerate DR (00-27).

RGXA (254-C3C) - Generate DR Arithmetic,

This command allows DR (00-30) to be regenerated.

RGXC0 (254-C2A) - Regenerate DR Character C0.

RGXF (254-C1A) - Regenerate DR Fractions,

This command regenerates DR Fractions C_1, C_2 & C_3.

RGXW (254-A6A) - Regenerate DR Word.

RGRDB (254-B2A) - Regenerate Read Burst,

This command generates a Read Command in Fast Memory when a "LOAD" is initiated.

SLL1A (255-C8A) - Shift Left Long 1 Arithmetic,

The Sum (S) bus (00-29) is shifted left 1 bit and a sign is generated. The GPR (00) bit is permitted through the RM (00).

SLL1W (255-C6A) - Shift Left Long 1 Word,

The Sum (S) bus (00-30) is shifted left 1 bit and the GPR 00 bit is permitted through the RM (00).

SLL4A (255-C6B) - Shift Left Long 4 Arithmetic,

The Sum (S) bus (00-26) is shifted left 4 bits and a sign bit (31) is generated. GPR (00-03) is permitted through the RM (00-03).

SLL4W (255-C5A) - Shift Left Long 4 Word,

The Sum (S) bus (00-27) is shifted left 4 bits and the GPR (00-03) is permitted through the RM (00-03).

SLS1W (255-C3A) - Shift Left Short 1 Word,

The Sum (S) bus (00-30) is shifted left by 1 bit.

SLS4W (255-C3B) - Shift Left Short 4 Word,

The Sum (S) bus (00-27) is shifted left by 4 bits.

SRL1W (255-B8A) - Shift Right Long 1 Word,

The Sum (S) bus (01-31) is shifted right by 1 bit and the GPR (03) is permitted through the RM (31).

SRL2W (255-B7B) - Shift Right Long 2 Word,

The Sum (S) bus (02-31) is shifted right by 2 bits and the GPR (02-03) is permitted through the RM (30-31).

SRL4W (255-B6A) - Shift Right Long 4 Word,

The Sum (S) bus (04-31) is shifted right by 4 bits and the GPR (00-03) is permitted through the RM (28-31).

SRS1A (255-B5B) - Shift Right Short 1 Arithmetic,

The Sum (S) bus (01-31) is shifted right by 1 bit (sign included) and the sign is generated (31).

SRS1W (255-B4A) - Shift Right Short 1 Word,

The Sum (S) bus (01-31) is shifted right by 1 bit.

SRS2A (255-B3A) - Shift Right Short 2 Arithmetic,

The Sum (S) bus (02-31) is shifted right by 2 bits (sign included) and the sign bit is generated in both RM 31 and RM 30.

SRS2W (255-B3C) - Shift Right Short 2 Word,

The Sum (S) bus (02-31) is shifted right by 2 bits.

SRS4A (255-B2A) - Shift Right Short 4 Arithmetic,

The Sum (S) bus (04-31) is shifted right by 4 bits (sign included) and the sign bit is generated in RM (31, 30, 29 and 28).

SRS4W (255-C2B) - Shift Right Short 4 Word,

The Sum (S) bus (00-31) is shifted right by 4 bits.

4.2.8.8 Sign Box Commands

SYSTL (256-D8A) - Select Sign From Y (00-03) Least True.

TRSY (256-D8C) - Trigger Result Sign From Y 00 (P).

SEFC (256-C6D) - Set Final Carry.

SEIC (256-C4A) - Set Initial Carry.

REFC (256-C3A) - Reset Final Carry.

SDST (256-C7D) - Select DIS True.

SDSI (256-C7B) - Select DIS Inverse.

SRSD (256-C6E) - Select Result Sign From DR 31 (1).

SRSI (256-C5B) - Select Result Sign Inverse.

RERS (256-C4D) - Reset Result Sign.

SRSX (256-B4A) - Select Result Sign From X 00 (P).

TRSU (256-C3C) - Trigger Result Sign From UR 31 (1).

4.2.8.9 UCAD & UR Commands

RUC (257-C8A) - Reset UCAD.

SUCB (257-C7A) - Select UCAD Byte Address,

This command selects UCAD byte address from IB (00-01) to UCAD (01-02).

SUC7 (257-C6B) - Set all bits in UCAD,

This command sets UCAD (00-02).

TUCD1 (257-C5A) - Trigger UCAD Down 1.

TUCD2 (257-C6B) - Trigger UCAD Down 2.

TUCU1 (257-C4A) - Trigger UCAD Up 1.

TUCU2 (257-C3A) - Trigger UCAD Up 2.

TUCU4 (257-C2A) - Trigger UCAD Up 4.

DBTRDCUC (257-B8B) - Transfer DCAD to UCAD,

This command transfers the contents of DCAD (00-02) to UCAD (00-02).

RURW (257-B6C) - Reset UR Word.

SURM (257-B6D) - Select UR Most,

This command reads IB (16-31) into UR (16-31). Remaining bits (00-15) are not affected.

SURW (257-B4A) - Select UR Word,

This command reads IB (00-31) into UR (00-31).

4.2.8.10 Main Memory Commands

1. Main Memory Command Permit Strobe, (Permit Strobe to Banks A, B, C, & D respectively).

   MMCPSA (258-C7A)

   MMCPSB (258-C7C)

   MMCPSC (258-C6A)

   MMCPSD (258-C5A)

2. Main Memory Command Execute, (Execute to Banks A, B, C, & D respectively).

   MMCEXA (258-C4C)

   MMCEXB (258-C3B)

   MMCEXC (258-C2A)

   MMCEXD (258-C2C)

3. Main Memory Command Regenerate, (Regenerate Banks A, B, C, & D respectively).

   MMCREGA (258-A7A)

   MMCREGB (258-A6A)

   MMCREGC (258-A6B)

   MMCREGD (258-A6C)

4. Main Memory Command Set Memory Register, (Set Memory Register for Banks A, B, C, & D respectively).

   MMCSMRA (258-A6D)

   MMCSMRB (258-B4A)

   MMCSMRC (258-B4B)

   MMCSMRD (258-B4C)

5. Inhibit Memory Address Register Reset, (Inhibit resetting Banks A, B, C, & D Memory Address Register).

   IMARRESA (258-AD4)

   IMARRESB (258-A3A)

   IMARRESC (258-A3B)

   IMARRESD (258-A3C)

MCROMAR (258-A3A) - Memory Command Readout Memory Address Register,

This command reads MA (00-01, 17-18) onto the IB (00-01, 17-18) respectively.

MMCNA (258-B2E) - Main Memory Commands Non-Addressing Area,

This command addresses the Shaded Memory portion of Main Memory.

4.2.9 INTERRUPT

4.2.9.1 Setting the PINT Flip-Flop

Permit Interrupt (PINT) allows the machine to go into the interrupt routine to determine what caused the interrupt and also to determine the value of the interrupt bit. This is dependent on the contents of the IMR (Interrupt Mask Register). If the IMR is reset, then machine returns control back to staticizing without checking on the interrupt bit.

If PE (Parity Error) or PF (Power Failure) or ADEX (Addressing Exception) occurs at any time except in the PINT routine or in an I/O instruction, the machine goes directly into the PINT routine with a 4G STL set in the STLR. 4G is the first STL of the PINT routine. For all other interrupts the PINT flip-flop (drawing 318) is set and 4G STL is selected out of 5X1 (first STL of Staticizing). See drawing 318 for the description below:

GATE C6A sets PINT flip-flop if 4G STL is being executed and PE/PF/ADEX (Addressing Exception) has occurred.

Gate C5A sets PINT flip-flop during 5C (2nd STL of Staticizing) if OPEX (Instruction Exception) occurs.

Gate C5E sets PINT flip-flop out of any Staticizing status level which selects the first STL of any instruction after staticizing if ADEX is set.

Gate C5B will set PINT flip-flop during 5X1 STL if CHIN-FF is set, LIINT FF is reset and any one of DCEX, IOIP, NIP, PIP or SCAN-1P is high. Each of these is described below.

CHIN FF (Check for Interrupt) is normally set, but can be reset to inhibit taking interrupt in two cases:

1. If Program Test is used (interrupt is inhibited to allow execution of one instruction).

2. If Execute is used (interrupt is inhibited so that execute can proceed to the instruction being executed without being interrupted).

LIINT FF inhibits PINT during the LOAD function which occurs when the load button is depressed.

DCEX is high when another computer asks for service from this computer and hence, PINT is set.

IOIP is high when the I/O requests that the Processor enter the PINT routine during termination.

NIP is high at Elapsed Time exception, Console Interrupt, Supervisor Call exception and when Program test mode is initiated.

PIP is high for Addressing exception, Data exception, Exponent Overflow exception, Divide exception, Specification exception, Exponent Underflow exception, Decimal Overflow exception, and Fixed Point Overflow exception.

SCAN-1P is high when Program Control instruction does not set the program test bit and Load scratch pad instruction does have N counter equal to the Interrupt Mask Register. The SCAN FF is set when SPAD addresses the Interrupt Mask Register.

4.2.9.2 Interrupt Flip-Flops

OPEX (319-A8A) - The OP Exception flip-flop is set if the instruction code is not legitimate.

DM (319-C5A) - The Debug Mode flip-flop is set in the program control instruction to indicate that the program test bit is set.

EOEX (319-C2C) - The Exponent Overflow Exception flip-flop is set to indicate that the 7 bits of the N counter have become zero from all ones in a floating point instruction.

SEEX (319-A5A) - The Significance Error Exception flip-flop is set to indicate that the result mantissa of the floating point add or subtract instruction is zero if PMR 00 (Program Mask Register) is set.

SCEX (319-A4A) - The Supervisor Call Exception flip-flop is set to indicate that the Supervisor call instruction has been executed.

EUEX (319-A3A) - The Exponent Underflow Exception flip-flop is set to indicate that the 7 bits of the N counter have become all ones from all zero in a floating point instruction if PMR 01 (Program Mask Register) is set.

OVEX (319-A3B) - The Fixed Point Overflow Exception flip-flop is set to indicate that an overflow has occurred in the result of a fixed point instruction.

ADEX (320-C6D) - The Addressing Exception flip-flop is set to indicate that an illegal address has been addressed.

DEX (320-A5A) - The Data Exception flip-flop is set if an invalid digit or sign code is encountered.

DOEX (320-B4B) - The Decimal Overflow Exception flip-flop is set if the result field of an Add Decimal, Subtract Decimal or Zero and Add instruction is too small to contain the overflow data if PMR 02 (Program Mask Register) is set.

DIEX (320-C2C) - The Divide Exception flip-flop is set if the quotient exceeds the register size in DIVIDE, or if the result exceeds 31 bits in Convert to Binary for Fixed Point Instructions; if the quotient is greater than the specified data field, including division by zero, or if the dividend does not have one leading zero for Divide Decimal Instruction; if division by zero is attempted for Divide Floating Point Instruction.

LIINT (320-A4A) - The Load Inhibit Interrupt flip-flop is set during Load to inhibit PINT until the first instruction has been executed.

CHIN (320-B2B) - The Check Interrupt flip-flop is reset when DM flip-flop is set to inhibit PINT. See DM description at the beginning of this section. Further description of CHIN can be found in the previous subsection (4.2.9.1).

NECK (320-B2C) - The Normal Error Check flip-flop is set except during I/O initiation or termination. When reset, it causes errors (MMPE/FMPE) to set appropriate CSB flags, instead of causing machine error interrupt.

FMPE (321-D7B) - The Fast Memory Parity Error flip-flop is set to indicate that a scratch pad parity error has occurred.

MMPE (321-D6D) - The Main Memory Parity Error flip-flop is set to indicate that a main memory parity error has occurred.

ETEX (321-B7B) - The Elapsed Time Exception flip-flop is set to indicate that the elapsed time clock has counted from positive to negative.

CKMMPE (321-A6B) - The Check Main Memory Parity Error flip-flop is set to indicate that main memory parity error can now be checked.

ETR (321-B5C) - The Elapsed Time Register flip-flop is set to indicate that the elapsed time routine will now be entered.

MESP (321-C4A) - The Machine Error Stop flip-flop when set, resets RUN flip-flop and also inhibits the contents of PSTLR (drawing 290) from dropping into STLR. Resetting RUN flip-flop shuts off the mode control (drawing 289) which effectively stops the machine.

PF (321-C1A) - The Power Failure flip-flop is set when power failure occurs and forces the machine to take the interrupt path.

COIN (321-B2A) - The Console Interrupt flip-flop is set when COIN button is depressed on the console, and console interrupt takes place which notifies the program that the operator desires some operation.

SMASP (321-A4C) - The Staticizing Memory Address Stop flip-flop is set when the address of the word containing the Op-codes matches the word address of the memory address switches on the maintenance panel.

IOMASP (321-C4B) - The Input Output Memory Address Stop flip-flop is set when the servicing word address matches the word address of the memory address switches on the maintenance panel.

EMASP (321-C3A) - The Execution Memory Address Stop flip-flop is set when the word address during the execution of any instruction (Normal Mode) matches the word address of the memory address switches on the maintenance panel.

In these three cases (SMASP, IOMASP, EMASP) the Processor comes to a normal stop after execution of the first interruptable status level.

4.2.10 MANUAL OPERATIONS

4.2.10.1 Scratch Pad Addressing

Contents of any scratch pad location can be displayed on the maintenance panel. For example, to read the contents of the P counter of program state 1, the digi switch should be set to 4 and the strip switch #2 is depressed. This will place the contents of the P counter in DR register for display. Every numbered (0-7) button of the FM (Fast Memory) strip switch when depressed activates FMONSW-P (see drawing 387). The right most button of the FM strip switch when depressed activates FMOFFSW-P (see drawing 387). When FMOFFSW is depressed the contents of DR register will be regenerated into the location indicated by the digi switch and FM strip switch. See Table 4-3 for the Scratch Pad Layout and the switch selections for addressing them.

1. FM Read from Maintenance Panel

   When FMONSW is depressed, SETFMC1-P (322-D4B) is high for the mechanical delay of the switch. This sets FMC1 flip-flop. When FMONSW-P goes high COSTA-P triggers the 170ms delay (322-C4F). This is to allow the scratch pad address generated by the switches to settle down because of switch bounce. The setting of FMC2 and the read of scratch pad is shown in Figure 4-7.

2. FM Write from Maintenance Panel

   For the write case, FMOFFSW is depressed and the whole sequence is the same as for the read case. The only exception is the generation of WRFM-P (243-B2B) which generates IS-P (256-B7C). This inhibits the contents of scratch pad from destroying the contents of DR. Contents of DR are regenerated into scratch pad.

Table 4-3. Scratch Pad Layout

DIGI SWITCH SETTING (4 most significant bits)	STRIP SWITCH (3 least significant bits)							
	7	6	5	4	3	2	1	0
0	D2A	D1A	UTY6 (NMCTR3)	UTY5 (NMCTR2)	UTY4 (NMCTR1)	UTY3 (NMCTR0)	UTY2	UTY1
1	GRF-P4	PC-P4	IS-P4	IM-P4	GRB-P4	GRA-P4	GR9-P4	GR8-P4
2	XAR3	MUTY2 INIT (CAR)	MXER SDB	MXER TERM3 (CCR1)	MXER TERM2 (CCR2)	MXER TERM1 (CAR)	MUTY1 INIT (CCR2)	MUTY0 INIT (CCR1)
3	IOS-CH1 (N.U.)	IOS-CH1 (N.U.)	IOS-CH1 (ASR)	(CCR1)	(CCR2)	IOS-CH1 (CAR)	RDM/WRM	UTY8 (N.U.)
4	GR7-P3	PC-P2	IS-P2	IM-P2	I.F.	PC-P1	IS-P1	IM-P1
5	GRF-P3	GRE-P3	GRD-P3	GRC-P3	GRB-P3	PC-P3	IS-P3	IM-P3
6	IOS-CH2 (N.U.)	IOS-CH2 (N.U.)	IOS-CH2 (ASR)	(CCR1)	(CCR2)	IOS-CH2 (CAR)	UTY10	UTY9
7	IOS-CH3 (N.U.)	IOS-CH3 (N.U.)	IOS-CH3 (ASR)	(CCR1)	(CCR2)	IOS-CH3 (CAR)	UTY-P3 (N.U.)	PAR
8	GR7-P2							GR0-P2
9	GRF-P2							GR8-P2
A	IOS-CH4 (N.U.)	IOS-CH4 (N.U.)	IOS-CH4 (ASR)	(CCR1)	(CCR2)	IOS-CH4 (CAR)	UTY12	UTY11
B	IOS-CH5 (N.U.)	IOS-CH5 (N.U.)	IOS-CH5 (ASR)	(CCR1)	(CCR2)	IOS-CH5 (CAR)	UTY-P2 (N.U.)	SAR
C	GR7-P1							GR0-P1
D	GRF-P1							GR8-P1
E	FPR7							FPR0
F	IOS-CH7 (N.U.)	IOS-CH7 (N.U.)	IOS-CH7 (ASR)	(CCR1)	(CCR2)	IOS-CH7 (CAR)	UTY-P1 (N.U.)	UTY13 (N.U.)

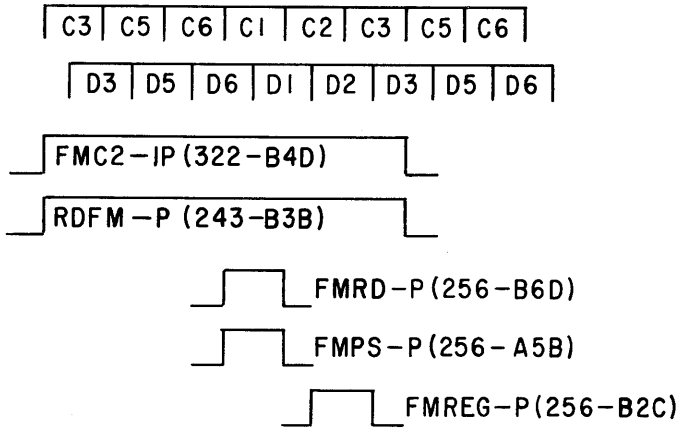


Figure 4-7. Scratch Pad Manual Read Timing

4.2.10.2 RDM/WRM

In the Read Main Memory or Write Main Memory manual operation, a Scratch Pad Memory cycle is required. The Main Memory Address (to read from, or write to) is loaded in FM location 31. When loading the address, bits 2^0 and 2^1 have no meaning because the RDM-WRM function always obtains a full word from the memory (i.e., full word address 00, 04, 08, 0C, etc.).

In the Read Memory operation, setting the RDM switch and pressing the START button on the maintenance panel will cause Main Memory contents of the address which has been put in FM location 31 to be displayed in the DR (maintenance panel data display indicators).

In the Write Memory operation, the information to be written into Main Memory must be set up in the DR (data display on maintenance panel). Setting the WRM switch and pressing the START button will cause this information to be written into the Memory Address which has been put in FM location 31.

In Read or Write, the Memory Address in FM location 31 will be incremented by 4 unless the AMI switch is set on the maintenance panel.

The sequence of logic for Read/Write Memory is shown in Figure 4-8.

4.2.10.3 Register Selection and Display (see Figure 4-9)

The Register Select Switches are a nine position gang switch located on the Auxiliary Maintenance Panel. Their purpose is to select hardware registers whose contents are to be displayed or modified by the Data/Display Switches. Figure 4-10 indicates the specific registers displayed by each Register Select Switch.

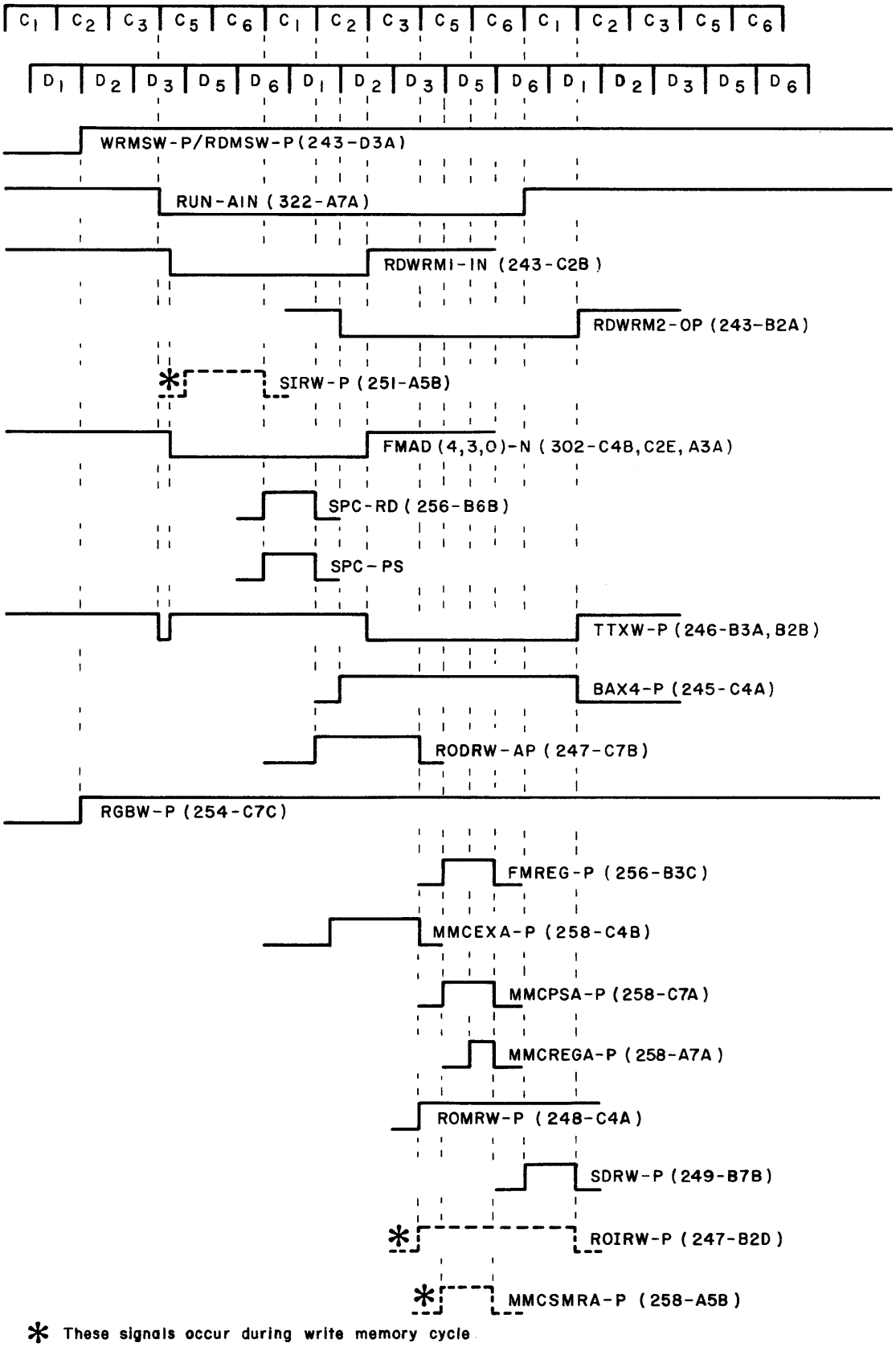
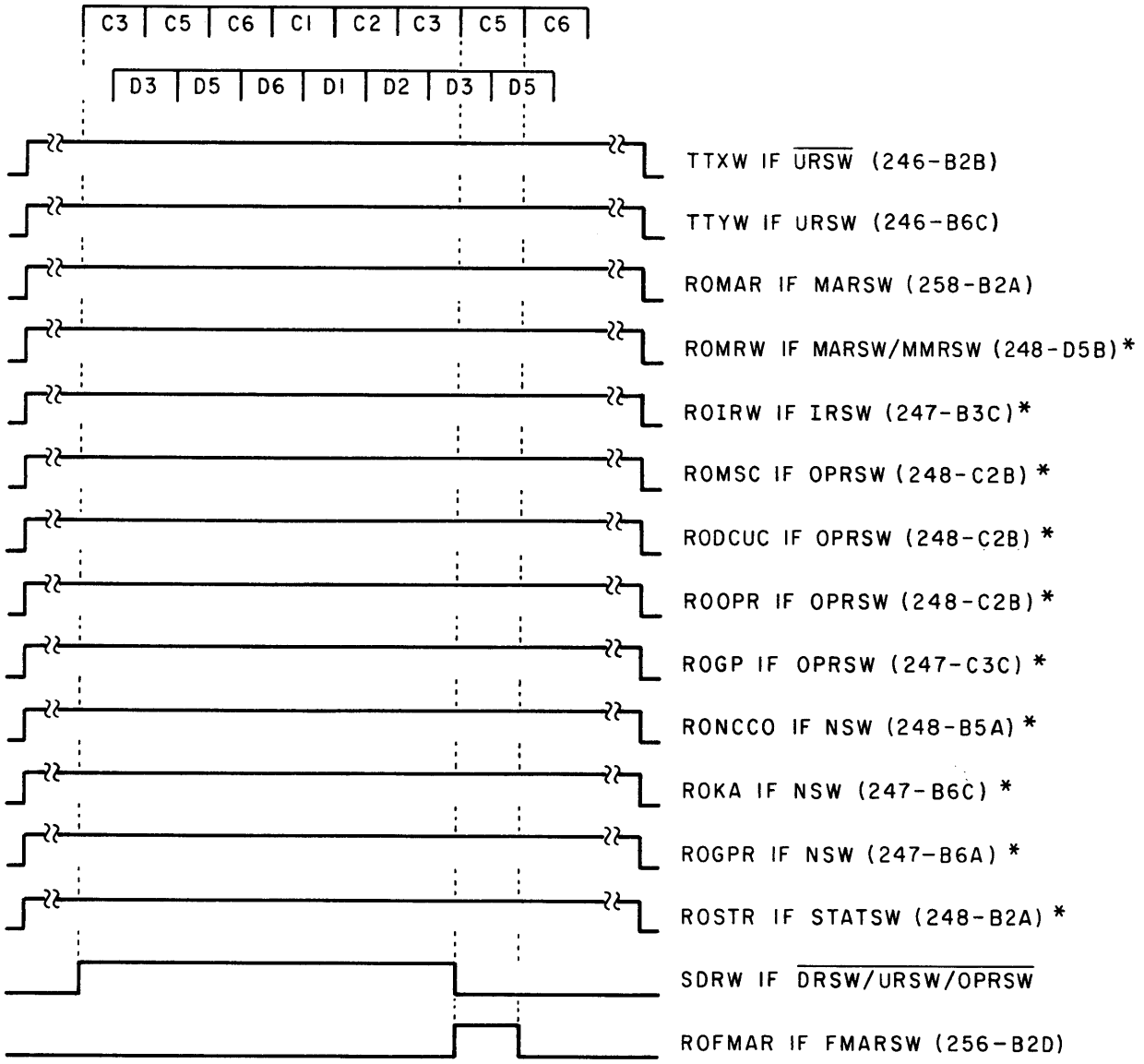


Figure 4-8. Read/Write Memory Timing



NOTE

* IF SET REGSW/RUN

Figure 4-9. Display Register Timing

1. Register Display

The 32 bits of the Data/Display switches display the selected register from the S Bus (output of the Adder) which drives 32 lamp drivers (D00-LT-D31-LT, drawings 215-219). The normal data path for a display function is accomplished by transferring the selected register to the Data Register and since the command TTXW (Transfer True X Word) is permissive when the processor is not running (246-B2B), the Adder output (which is displayed) is the same as the DR contents.

Register Select Switches	P	C0		C1		C2		C3
FMAR Fast Memory Address Register								FMAR03
							FMAR06	FMAR02
							FMAR05	FMAR01
							FMAR04	FMAR00
MAR Main Memory Address Register					MAR15	MAR11	MAR07	MAR03
				MAR18	MAR14	MAR10	MAR06	MAR02
				MAR17	MAR13	MAR09	MAR05	MAR01
				MAR16	MAR12	MAR08	MAR04	MAR00
MR - Main Memory	x 31	x 27	x 23	x 19	x 15	x 11	x 07	x 03
URx- Utility Register	x 30	x 26	x 22	x 18	x 14	x 10	x 06	x 02
IRx- Intermediate Register	x 29	x 25	x 21	x 17	x 13	x 09	x 05	x 01
	x 28	x 24	x 20	x 16	x 12	x 08	x 04	x 00
OPR Operation Code Register	ILC-1	xPMR03	UCAD02	DCAD02	xOPR07	xOPR03	xGPM03	xGPL03
	ILC-2	xPMR02	UCAD01	DCAD01	xOPR06	xOPR02	xGPM02	xGPL02
	xCCR01	xPMR01	UCAD00	DCAD00	xOPR05	xOPR01	xGPM01	xGPL01
	xCCR00	xPMR00			xOPR04	xOPR00	xGPM00	xGPL00
N N Counter		x N03	xKR03	x A				GPR03
	x N06	x N02	xKR02		MDR02	FC		GPR02
	x N05	x N01	xKR01		MDR01	IC		GPR01
	x N04	x N00	xKR00	xNPRIV	MDR00			GPR00
STAT	PSTLR7	PSTLR3	STLR7	STLR3	FTT2	RS	CFF8	CFF4
	PSTLR6	PSTLR2	STLR6	STLR2	FTT1	CFF11	CFF7	CFF3
	PSTLR5	PSTLR1	STLR5	STLR1	ZFF	CFF10	CFF6	CFF2
	PSTLR4	PSTLR0	STLR4	STLR0	DS		CFF5	CFF1

x Can be modified through Register Select Switch & Set Register Function

Figure 4-10. Register Selection And Display

When the IR Register select switch is depressed, signal DIRSW-P (247-B3C) goes high and generates ROIRW-AP which is powered up to become ROIRW-AN, BN, CN, & DN on drawings 239, 240, and 241. These four command signals permit the read out of the IR on the IB (Input Bus). This data is read into the DR by enabling signal SDRW-P (249-B7D). Gate B7D receives its final prime from signal CODR-N which is generated at 322-B4B. On drawing 322, gate D5B is primed with the depression of any register select switch since signals SELREGSW-P and SELRESSW-P both go low during the travel time of the register select reset switch. The COSET flip-flop (322-C5A) is set, partially priming gate

C4B which is completely primed by signal SETCOSET-P going low due to the turn off of gate D5A by SELREGSW-P. The output of gate C4B triggers a two stage one-shot developing a 1 micro-sec. negative signal (COST-N) after a 170 milli-sec. delay to allow for switch bounce. COST-N permits the set of COSIT flip-flop (322-B5C) which permits the generation of CODR-N. Signal CODR-N is the final prime necessary to read the IR data now on the IB into the DR. COSIT being set permits the reset of COSET which then resets COSIT. The IR data is now in the DR and since the processor is not running, TTXW is permissive allowing the DR contents through the Adder to the data display switch indicators.

When the MR Register Select switch is depressed, signal DMRSW-P (248-D5B) generates ROMRW-P and N. The contents of a Memory location will be in the MR only on a Machine Error Stop or immediately after a Memory Addressing Status Level in SFSP since the readout control of the memory data to the Bus Separator is dropped after a successful Memory Read. ROMRW-P and N opens the Bus Separator permitting the MR data on the IB after which the DR read in is accomplished as described above for the IR Register Select switch.

When the FMAR Register Select switch is depressed, signal DFMARSW-P (256-B2B) generates ROFMAR-N. DFMARSW-P inhibits SDRW-P at 249-B7D, but enables RDRW-P at gate 249-D6B, which is completely primed by signal CODR-N occurring 170 milli-sec. after depressing the switch as described earlier for the IR Select Register switch. Signal ROFMAR-N permits the direct transfer of the FMAR to the DR which is then displayed. Signal RDRW-P is necessary to clear extraneous bits that may have been in the DR.

When the MAR Select Register switch is depressed, signal DMARSW-P (258-B2A) generates MCROMAR-AP, -BP, -CP, & -DP. These signals are sent to the MM and permit the transfer of MAR to MR. MCROMAR-AP also drives an inverter (258-A3D) whose outputs are MROMAR-AAP and MCROMAR-AN. Signal MROMAR-AAP generates the ROMRW-P/N (248-D5B) and inhibits the MR00 & MR01 bits at the Bus Separator (238-C6A) and the MR17 & MR18 bits at the Bus Separator (240-C1A, C3C). The 00, 01, 17, & 18 bits are the byte address bits and the bank address bits, and are not stored in the memory bank but rather in four flip-flops of the BPU called MA00, MA01, MA17, and MA18. These four address bits are permitted through the Bus Separator by signal MCROMAR-AN on drawings 238 and 240. The total address is thus permitted through the Bus Separator, through the DR to the Adder. The display is similar to that described for the IR Register Select switch.

When the N Register Select switch is depressed, signal DNSW-P (247-B6C) generates ROKA-P which is inverted (240-B8A) to become ROKA-AN and ROKA-BN. ROKA-AN opens the Bus Separator for the IC, FC and MDR. ROKA-BN opens the Bus Separator for the Code Mode (A), NPRIV, and the Key Register. ROKA-P also generates RONCC0-P (248-B5A) which is inverted at 240-A2A and permits the

N Counter through the Bus Separator. ROKA-P also generates ROGPR-P (247-B6A) which is inverted (240-B3A) to permit the GPR through the Bus Separator. The display path from this point is the common one described for the IR Register Select switch.

When the OPR Register Select switch is depressed, signal DOPRSW-P (248-C2B) generates ROOPR-N and ROMSC-P, and also generates ROGP-N/P (247-C3C). These control signals open the Bus Separator to permit the specific bits detailed on the Figure 4-10.

When the STAT Register Select switch is depressed, signal DSTATSW-P (248-D2A) generates ROSTR-P. Signal ROSTR-P is power inverted on drawings 239, 240, and 241 to generate ROSTR-AN, BN, CN, and DN which open the Bus Separator to permit the specific bits detailed on Figure 4-10.

Since there is no data path from the UR to the IB, the UR Data Display is mechanized somewhat differently.

When the UR Select Register switch is depressed, signal DURSW-P (246-B6C) generates TTYW-P and inhibits TTXW-P (246-B2B) to inhibit SDRW-P (249-B7D). The contents of the UR are transferred through the Adder and displayed direct.

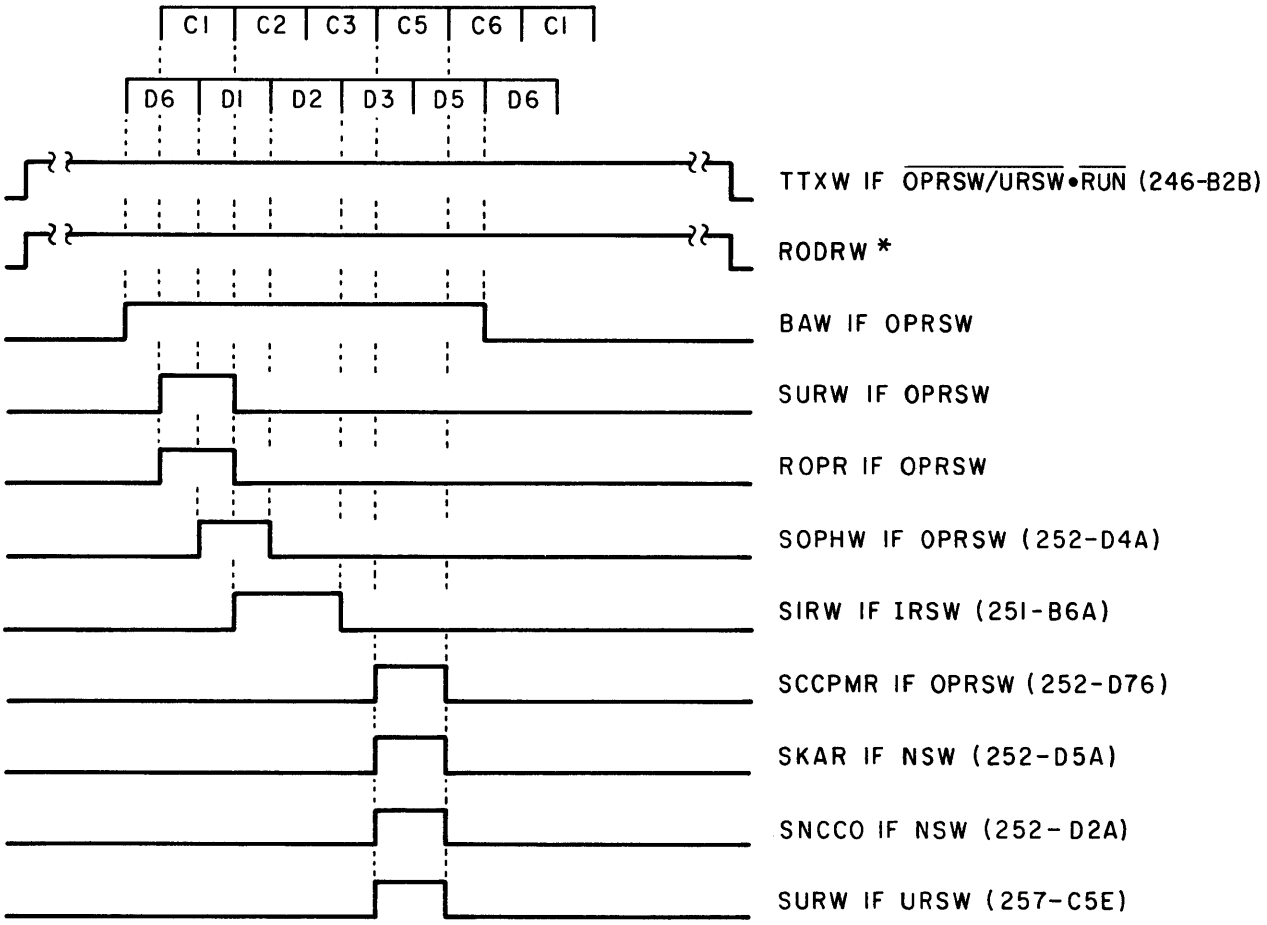
Since the IB normally sits low and some Register Select switches do not display a full word, an inhibit signal must be present on some IB bits to prevent setting of extraneous DR bits. ROC-P (240-B4A) is generated for all partial byte read commands to accomplish this.

2. Register Modification (see Figure 4-11)

Some registers which can be displayed, cannot be modified through the Register Select switches. Those which can be modified are indicated with X on Figure 4-10. Depression of a Data Display switch-indicator sets that specific bit in the DR. To delete a bit, the DR byte must be cleared and those bits to be retained must be re-entered. Depression of the Set Register switch transfers the contents of the DR to the Selected Register. The altered contents of the Selected Register are then re-displayed to insure positive modification. Modification of Registers via the OPR Select Register switch destroys the contents of the UR.

Modification of the UR register must be treated as a special case since the Data Display switch-indicators are indicating the contents of the UR rather than the DR when the UR Select Register switch is depressed.

When the UR is displayed, the DR is reset, and since depression of the Set Register switch transfers DR to UR, the UR would then be reset. The entire word of the UR must be entered into the DR prior to depression of the Set Register Switch. Any modifications entered to the DR will not be visible since the DR is not being displayed. Depression of the Set Register Switch will



NOTES

*PRESENT AS LONG AS "SET REG" SWITCH IS HELD DEPRESSED.

DISPLAY REG CYCLE IS EXECUTED WHEN "SET REG" SWITCH IS RELEASED.

Figure 4-11. Set Register Cycle

transfer the altered DR to the UR which is then displayed for visual confirmation.

After the modified data has been properly entered in the DR, depression of the SETREGSW will set flip-flop CSET1 (322-C2A). Signal CSET1-1P will enable the bus command RODRW-P (247-C6B) permitting the modified data on the bus. The Read In commands are enabled by signal CSET2-0P (for example see 251-B6A and 252-D4A). When the SETREGSW is released, CSET1 is reset generating signal CODI-P (322-C3C) which sets COSET and permits the redisplay of the selected register as described earlier in the description of the IR Register display.

4.3 INPUT-OUTPUT OPERATION

The repertoire of the 70/55 Processor includes four I/O instructions. They are Start Device, Halt Device, Test Device and Check Channel. These instructions are executed by the Processor and the results, in the form of condition codes are available upon instruction completion.

After initiation, the input/output operations are executed by the selected channel and are independent of normal processor operation. When the device control electronics is ready to send or receive a data byte, the channel asks the processor for a service request. If the next processor status level is not NI (Non-Interruptable), the channel status levels take control of the processor for the data transfer. See the mode control logic (4.2.4) for a further description of mode selection and priority.

The 70/55 IOU Block Diagram is shown on Figure 4-13. This diagram contains representations of the Input-Output areas of logic. Abbreviations are used to identify the logic and reference numbers indicate the last three digits of the drawing on which that logic is shown.

4.3.1 MUX SERVICE SCANNER AND CONTROL

At the completion of servicing a byte, the MSCNCPT FF (332-B5B) gets set. If certain other conditions are present, this will permit MSP-AN; BN signals. This is the beginning of preparations for servicing the next Service Request (SR).

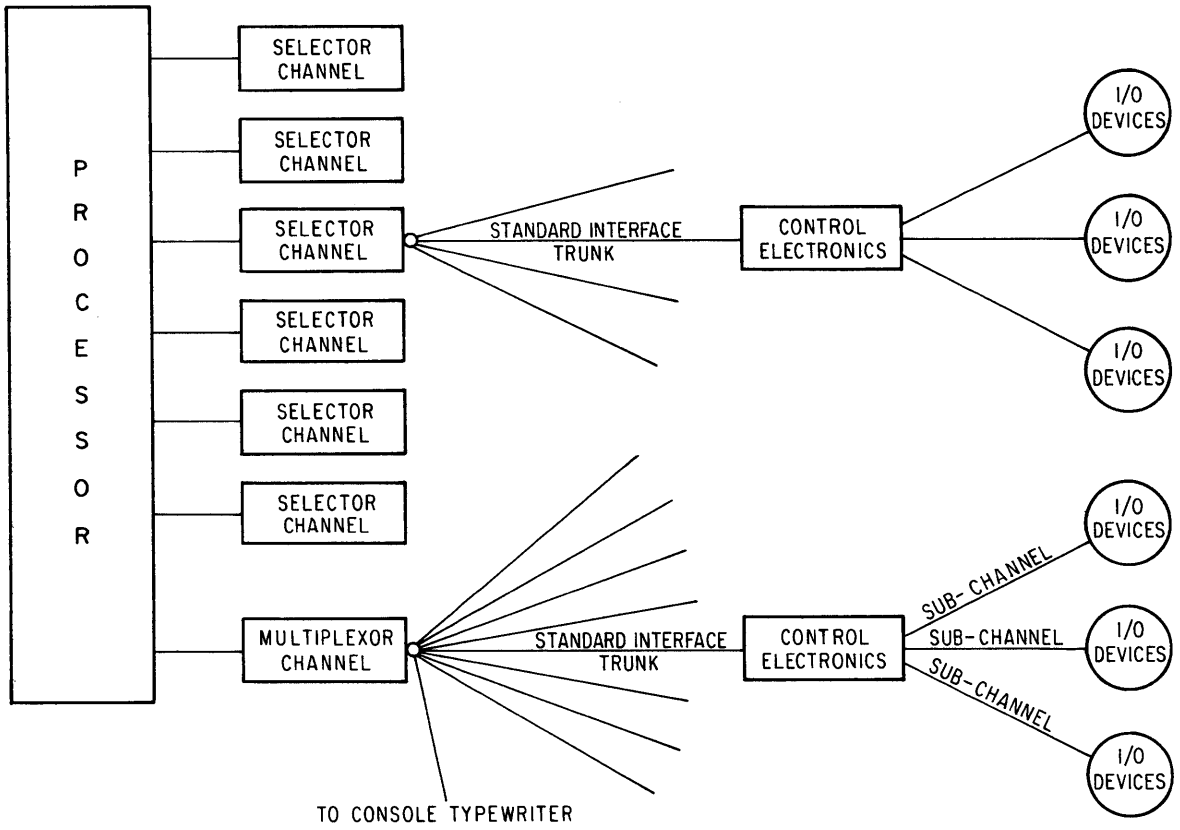


Figure 4-12. 70/55 Input-Output Channels

The MUX Service Scanner is shown on drawings 331 and 354. The MSP-AN; BN signals are fed into the jam set/reset input gates of the MTXSCAN FFs (331-B7C and 354-B7A), these in turn are primed by the MT(X)ULSC FFs which are set by a SR (Service Request) arriving on a previously initiated trunk. If more than one MT(X)ULSC FF is set, only the trunk with the highest priority will have its MTSCAN FF set. The priority is from trunks 1 to 9 inclusive with 1 having the highest priority. This is accomplished by the MTXULSC - 0N lines from trunk 1 on up to 8, inhibiting all of the remaining MT(X)SCAN set input gates. When the MT(X)SCAN FF gets set, it develops the MT(X)SEL lines which are used for selective trunk gating throughout the MUX logic.

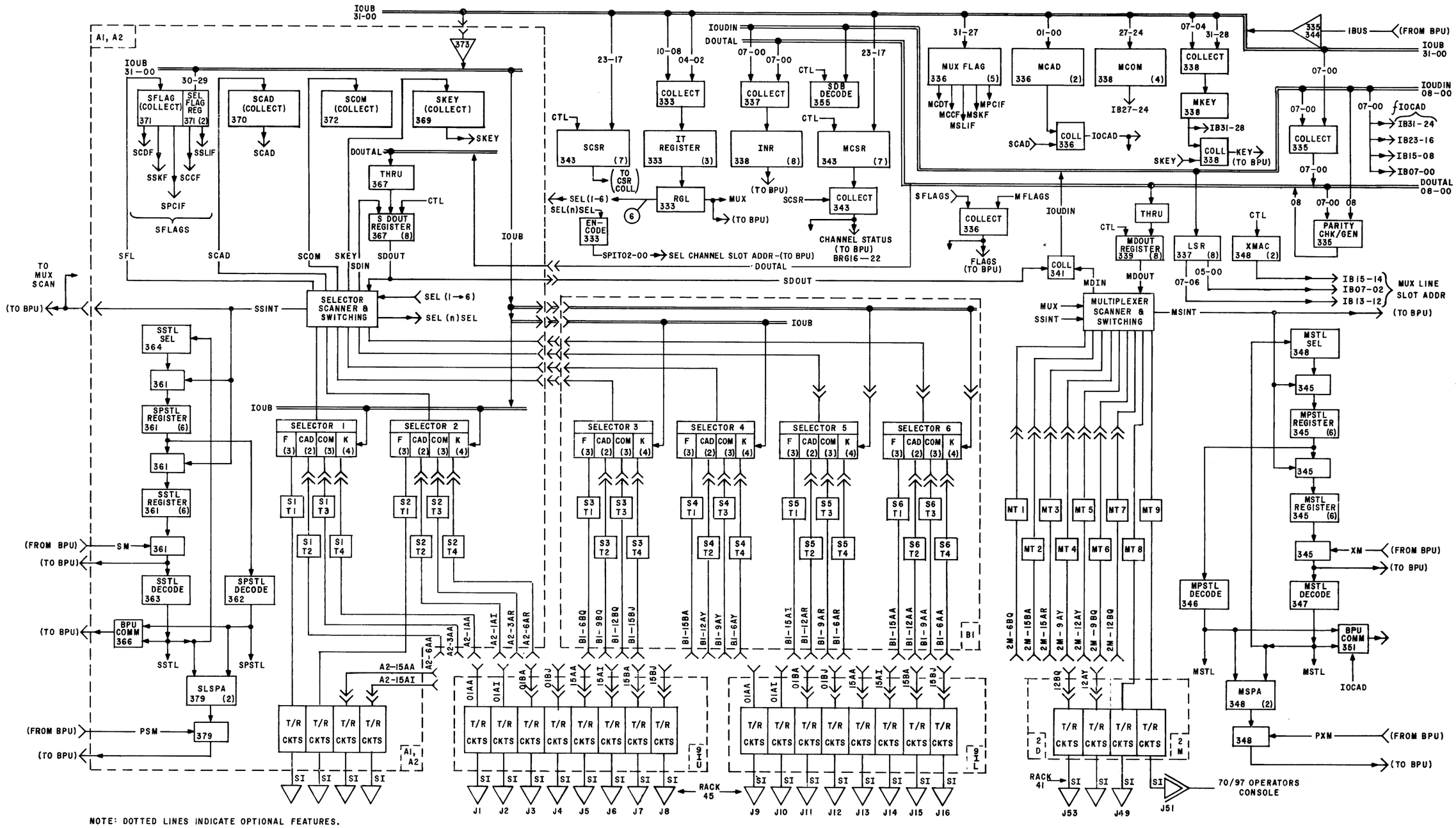
The Multiplexor signals the BPU that it wishes to do Servicing by sending MSINT (332-B7C). This signal is formed by the OR'd output of all the MT(X)ULSC FFs thereby saying that one or more Service Requests have arrived on one or more MUX trunks and the BPU was not executing a Non-Interruptable STL (NI) in the Normal Mode. MSINT is sent to Mode Switching Control (289-D3B and D4B) where it will set PXM provided a Selector Service Request (SPSM) is not present. PXM in turn will allow the XM flip-flop (289-B4A) to get set. These two flip-flops will drive power inverters to supply all the required PXM and XM mode status levels necessary to allow the machine to operate in the MUX Mode. At D1 time of the first STL of MUX Servicing, the XAC flip-flop (289-C8C) is set. The purpose of this flip-flop is to remind the BPU to return to MUX Servicing after this has been broken into by Selector Servicing (which is of a higher priority).

As long as any Selector Channel Service Requests are still present at the end of each Selector Channel Servicing of a byte, the machine will continue in Selector Channel Servicing and the continuation of the MUX Servicing will be held off. The Scanner Control logic works as follows: At the last status level of MUX Servicing (4BM2), the MSCNCPT flip-flop (332-B5B) will be set. If there are no errors (STMCSR-1P) or $\overline{\text{NI}}/\overline{\text{DINHSP}}$, MSP-AN; BN (332-A5A) will be generated to start the servicing of the next byte (provided that these conditions are not present). Regardless of BURST, MSP-N is developed which pre-selects the 3BM1 status level (348-D7A). This is the first status level of MUX Servicing. Also generated is MSP-P which goes to reset the XAC flip-flop (289-C8C). There are also 2 other gates that develop MSP-P. One if $\overline{\text{CATSUP}}$ (332-B6A) and the other one generates MSP-P in 4BM2 status level if no errors exist (332-B6B). The DINHSP signal is developed on 326 at C5C/C4D. If during a Start Device Initiation a STCSR or ADEX error occurs, the MSP pulse must be inhibited to prevent entering servicing until the appropriate action can be taken on these errors while still in Normal mode.

4.3.2 MUX STATUS LEVELS

When MUX Servicing is allowed, the first STL (status level) of Servicing must be developed. Once this STL (3BM1) is formed, all of the remaining status levels are pre-selected by the exit conditions of their immediate predecessors. The development of MUX status levels is as follows:

1. The 3BM1 status level is generated (348-D7A) by MSP which was described in the previous sub-section (MUX Service Scanner and Control).



NOTE: DOTTED LINES INDICATE OPTIONAL FEATURES.

Figure 4-13. 70/55 IOU Block Diagram

2. The current status level develops the MSXXnxMn signals on drawing 348 where the MS = MUX Servicing; XX = Setting of MSPA and XMAC respectively; nxMn = the MUX (M) STL designation (for ex., 5ZM1). MSPA is MUX Scratch Pad Address and XMAC is Shaded Memory Address. These are further explained in the Scratch Pad and Shaded Memory Sections respectively.

3. The MSXXnxMX signals (if required) go to set XMAC and MSPA flip-flops on 348. The MSXXnxMX signals are used on drawing 345 to gate (directly or by forming SnxM (n) signals along top of drawing) the setting of MPSTLXX. These are the MUX Pre Status Level Register. They are set at C6M time of the STL just finishing. The 1N outputs of the MPSTL Register gate the setting of MSTL XX Register at DD6 time of the same STL if the MESP FF is not set.

4. The 1P and 0P outputs of the above two Registers are sent to drawings 346 and 347 for decoding of the PSTLs and STLs. On 346, the MPSTL XX signals develop the MPSTLXXX signals. These in turn develop the PSTLs at the top of the print. The same scheme holds true on 347 for the MUX STLs. The Pre and regular STLs are used throughout the machine to gate signals used in the execution of the STLs. The PSTLs are used when signals must be developed early for the incoming STL. They are available from D6 time of the exiting STL until D5 time of the incoming STL. The STLs are available (firm) from D1 thru C6 time of its STL.

The first STL of MUX Servicing (3BM1) is developed by the MSP-N signal generating MSXX3BM1-P (348-D7A) which pre-selects the 3BM1, by using S3BM-P (345-D8A). This in turn, primes the input gates for MPSTL05 (345-C7A) and MPSTL03 (345-C5A). All that is required now is the XM-AAN signal (345-C8B). This will occur upon the arrival of a SR and development of MSINT as explained under the previous section (MUX Scanner & Control) which also explains the MSP signal.

The FRSW (Function Repeat Switch) button (344-C8A, C8B) when depressed will prevent the resetting and setting of the MPSTL Register. Thus the machine can be cycled on the same STL. Along the bottom of drawing 345 are the gates that feed the STL display lights on the Console (MUXD0 - MUXD5). The XM-0P level on the priming gate (A7A) says that the machine must be in MUX mode to display its MSTL Register. Table 4-4 contains the Multiplexor Status Levels and their standard functions.

4.3.3 SCRATCH PAD USE, LOCATIONS AND MSPA

The Scratch Pad Locations 20 through 27 are allocated to Multiplexor operations. (Scratch Pad Addresses are designated as they would be selected by the maintenance panel digi and strip switches.) Locations 22, 23, 24, and 25 are used exclusively for termination storing of the CAR, CCR words and the Standard Device Byte. Locations 20, 21 and 26 are used only for MUX Servicing. They are used, respectively, to store the CCR1, CCR2 and CAR words. Functionally, location 27 contains the word being transferred (during 5BM1 and 5BM4 status levels) to a device (byte at a time) in the Write case and in the Read case shows whether each byte has gone to main memory as the following SR is being serviced. During Servicing, the CCW1 word is brought from its Line Slot in Shaded Memory as a function of the

Table 4-4. Multiplexor Status Levels

Type	PSTLR/STLR Bit Display 5	4	3	2	1	0	Standard Function
3AM1	1	0	0	0	0	0	Information to Scratch Pad
3AM3	1	0	0	0	1	0	" " " "
3BM1	1	0	1	0	0	0	Information does not go to Scratch Pad
3BM2	1	0	1	0	0	1	" " " " " "
3YM1	1	1	1	0	0	0	Info. to or from Shaded Memory
3YM2	1	1	1	0	0	1	" " " " "
3YM3	1	1	1	0	1	0	" " " " "
3YM4	1	1	1	0	1	1	" " " " "
3YM5	1	1	1	1	0	0	" " " " "
4AM1	0	1	0	1	0	0	Shaded Memory to Scratch Pad
4AM2	0	1	0	1	0	1	" " " "
4BM1	0	1	1	0	0	0	Scratch Pad to DR to Shaded Memory
4BM2	0	1	1	0	0	1	" " " "
4DM1	0	1	1	1	0	0	Update CCR's or CAR and Results to
4DM2	0	1	1	1	0	1	Scratch Pad
4DM3	0	1	1	1	1	0	" " " " "
4DM4	0	1	1	1	1	1	" " " " "
5AM0	0	0	1	0	0	0	Scratch Pad to Hardware Reg. to modify CAR. Results to Scratch Pad; Used in chaining or Transfer in Channel.
5BM1	0	0	0	1	0	0	Read: DIN to MR
5BM2	0	0	0	1	0	1	Load: CCR1 to Scratch Pad
5BM3	0	0	0	1	1	0	Command Code 2^4-2^7 to IOU Burst Mode only - sets Burst FF.
5BM4	0	0	0	1	1	1	Write: MR to DOUT
5ZM1	0	0	1	1	0	0	Shaded Memory to Scratch Pad
5ZM2	0	0	1	1	0	1	" " " "
6AM1	0	1	0	0	0	0	CAR(in Scratch Pad)to Shaded Memory
6AM2	0	1	0	0	0	1	Command Code (2^0-2^3) to IOU

device number and put in location 20 which is designated as MUTY1. This is accomplished by the 3YM1 and 3AM1 STLs. Similarly, the CCW2 is stored in location 21 (MUTY2) by 3YM2 and 4DM1 STLs. They are now in position to be more quickly accessed for the remaining STLs of the Service Request Processing. If Data or Command Chaining is called for, the CAR word is brought from Shaded Memory and stored in location 26 (MUTY3) by the 3YM5 and 4AM2 STLs.

The format of the Scratch Pad locations used for MUX Servicing is the same as that of the Selector, except that CCR1 contains the keys in 0→3 bit locations (for the MUX) and there is no Assembly Status Word for the MUX.

The MSPA logic (348-B3D, etc.) designates which of the four MUX Servicing SP locations is to be selected. MSPA1-P develops FMAD1 and 2-N while MSPA0-P develops FMAD0-N (302-A5A, A2A). MUX Servicing is indicated by the signal PXM-AAP which in turn develops the FMAD4-N signal. Thus the 2 of the 2(X) location is available to combine with the 0, 1, 6 or 7 formed by the MSPA(X)-P lines. The MSPA addressing scheme is as follows:

MSPA(1-0)	FMAD6	FMAD5	FMAD4	FMAD3	FMAD2	FMAD1	FMAD0	Word Addressed
00	0	0	1	0	0	0	0	MUTY 1
01	0	0	1	0	0	0	1	MUTY 2
10	0	0	1	0	1	1	0	MUTY 3
11	0	0	1	0	1	1	1	XAR

4.3.4 SHADED MEMORY LOCATIONS

A set of three 32 bit registers for each device on the Multiplexor is contained in Shaded Memory. They are used to service devices on the Multiplexor Channel. Each device has a CAR, CCR1 and a CCR2 location in which is stored the CAW, CCW1 and CCW2 words. There are 256 sets of these words. The addressing of these words is done by sending the device address and the XMAC bits to MAR (Memory Address Register) and also setting the NA (Non-Addressable) flip-flop at the same time as the MMC-EX (MM Execute) command is given.

These Shaded Memory contents are fetched and restored during Initiation, PINT and for each SR except in BURST/CATSUP cases. Shaded Memory Contents are fetched once for the entire BURST operation and once for each group of CATSUP SRs.

Shaded Memory Addressing is accomplished by the LSR (Line Slot Register) and XMAC.

4.3.4.1 Line Slot Register And XMAC

When a Service Request is present from a MUX trunk not in BURST or CATSUP, the DIN lines contain the Device Address. This address is stored in the LSR (Line Slot Register) (see drawing 337) in the first STL of Servicing. The XMAC Register (348-A7D) consists of two flip-flops which are set up during servicing to specify which of the three words in Shaded Memory to select, the CAR, CCR1 or CCR2. During the Shaded Memory addressing STLs, the LSR and XMAC bits are sent to the memory to address the specified word. The addressing scheme is as follows:

LSR 2^0 --- 2^5 goes to MAR Bit Positions 2^2 --- 2^7
LSR 2^6 & 2^7 goes to MAR Bit Positions 2^{12} --- 12^{13}
XMAC 01 & 00 goes to MAR Bit Positions 2^{15} & 2^{14}

Manual addressing of Shaded Memory for Read or Write requires the following addressing scheme which is helpful in describing the LSR and XMAC functions. In the following example the YY in 2^{15} and 2^{14} select which of the three words is to be addressed. In a normal servicing flow, YY is the XMAC output. For manual Shaded Memory addressing, the bit configurations shown must be inserted to address CAR, CCR2 or CCR1.

	C2								C3							
	2^{15} Y	2^{14} Y	2^{13} X_2	2^{12} X_2	2^{11} 0	2^{10} 0	2^{9} 0	2^{8} 0	2^{7} X_2	2^{6} X_2	2^{5} X_1	2^{4} X_1	2^{3} X_1	2^{2} X_1	2^{1} 0	2^{0} 0
CAR	1	1	0	1	0	0	0	0	1	0	0	1	0	0	0	0
CCR2	0	1	0	1	0	0	0	0	1	0	0	1	0	0	0	0
CCR1	1	0	0	1	0	0	0	0	1	0	0	1	0	0	0	0

The $X_2X_2X_2X_2$ and $X_1X_1X_1X_1$ hexadecimal digits represent the device number. In normal servicing this portion of memory address comes from the LSR. The examples above show the bit configuration for addressing CAR, CCR2 or CCR1 for MUX device number $(64)_{16}$.

Manual Shaded Memory addressing also requires the setting of the maintenance panel switch, ASM.

4.3.5 MULTIPLEXOR GENERATED BPU COMMANDS

During MUX Servicing, the Multiplexor generates the BPU Commands. They can be grouped into four types, Main Memory, Scratch Pad, Adder Commands and Bus Commands. There are also three miscellaneous commands not falling into these categories.

1. Main Memory Commands

   REG (351-B4A) - Regenerates the MR (Memory Register) contents back into MM.

   SMR (351-B3C) - Sets bits into MR from the bus.

   PS (351-B2A) - Permits Strobing out the word on a MM Read Command.

2. Scratch Pad Commands

   RGXW (351-C8B) - Regenerates the DR word into the SP.

   GEPA (351-C3A) - Generates Parity during the RGXW time.

   FMRD (351-C2B) - Read Command to the SP.

   IS (351-C5B) - Inhibits Strobe during FMRD Command.

   IORGQ (351-C5A) - Allows regeneration of C_0 byte from DR and C_1, C_2 and C_3 bytes from the output of the Adder (Sum Bus).

   IORGH (351-B7A) - Same as IORGQ except DR C_0 and C_1 and Adder C_2 and C_3 bytes.

   IRDR27 (351-B2C) - Inhibits the regeneration of DR27 bit. This is used to prevent storing of the PCI Flag bit in SP since its function has already been performed and the bit must now be eliminated.

3. Adder Commands

TTXW (351-B7C) - Permits transferring of the true DR word through the Adder unaltered.

TTXK (351-B2E) - Permits transferring of one particular byte from DR through the Adder. This byte is specified by the IOCAD (MCAD) setting.

BAX1 (351-B6B) - Binary Adds count of one to DR word.

BAX4 (351-B8B) - Binary Adds count of four to DR word.

BSX1 (351-B4B) - Binary Subtracts count of one from DR word.

4. Bus Commands

RODRW (351-C3C) - Reads out to bus the DR outputs.

$RODRC_0$-C_3 (351-A7D to A6B) - Reads out to bus the DR output of one of the four bytes as specified by IOCAD. The IOCAD develops the CSC(X) logic as shown on the bottom center section of 351.

RODIN0→3 (351-A5F to A4F) - Reads out the DIN byte specified by CSC(X) logic onto the bus.

ROMRWA(& WB) (351-B2B and C4B) - Two Commands which read out the MR outputs onto the bus.

ROMXSAD (351-B5B) - Reads out the outputs of the Line Slot Register (LSR) and the XMAC onto the BUS. This information is the device address of the device being serviced and the particular word location in the slot being accessed.

The three miscellaneous commands are SENI (351-C6D) which sets the NI (Non Interruptable) flip-flop which prevents the Selector Channel from breaking into the MUX Servicing at the end of the status level in progress; RRUN (351-B6C) which resets the RUN flip-flop in the BPU and SDRC0 (351-B3A) which allows the setting of DR Character 0 ($2^{31} \longrightarrow 2^{24}$) only from the bus.

4.3.6 INTERFACE CONTROLS

The Interface Control signals control the sending of the Interface signals to the Control Electronics (CE). The MACT flip-flop (349-C7B) (MUX Activate) is set by the first STL of Servicing (3BM1). This tells the CE that the SR has been accepted. MACT is also set by 5ZM1 STL to handle BURST and/or CATSUP since the flow does not return to 3BM1 in these modes of operation.

The MSEL flip-flop (349-C5B) (MUX Select) is set in 3YM4 STL for Servicing and at various other times during Initiation and Interrupt processing. Its purpose is to indicate to the CE to place the Address of the device requesting service on the DIN lines. All other Interface control lines should be 0 at this time.

The MTRAC flip-flop (349-C2B) MUX TRAC is set in 6AM2 STL (for servicing) to indicate that a Command is being Strobed on the DOUT lines. All other Interface control lines must be 0 except STROBE which must be 1.

The TERM flip-flop (350-C7D) is set (during servicing) by any of three different occurrences.

1. Count has reached 0 and Chain Data is not called for (350-D7A).

2. A MTERANY type error has occurred (350-D8A).

3. A HALT instruction was issued while the MUX was operating in BURST mode (350-C8C).

When the TERMINATE Interface line is raised, it signals the CE that the last data byte has just been transferred to or from the device. The CE responds by raising the END Interface line with its next SR. STROBE must be present and ACTIVATE must have been previously sent. All other control lines are 0 at this time.

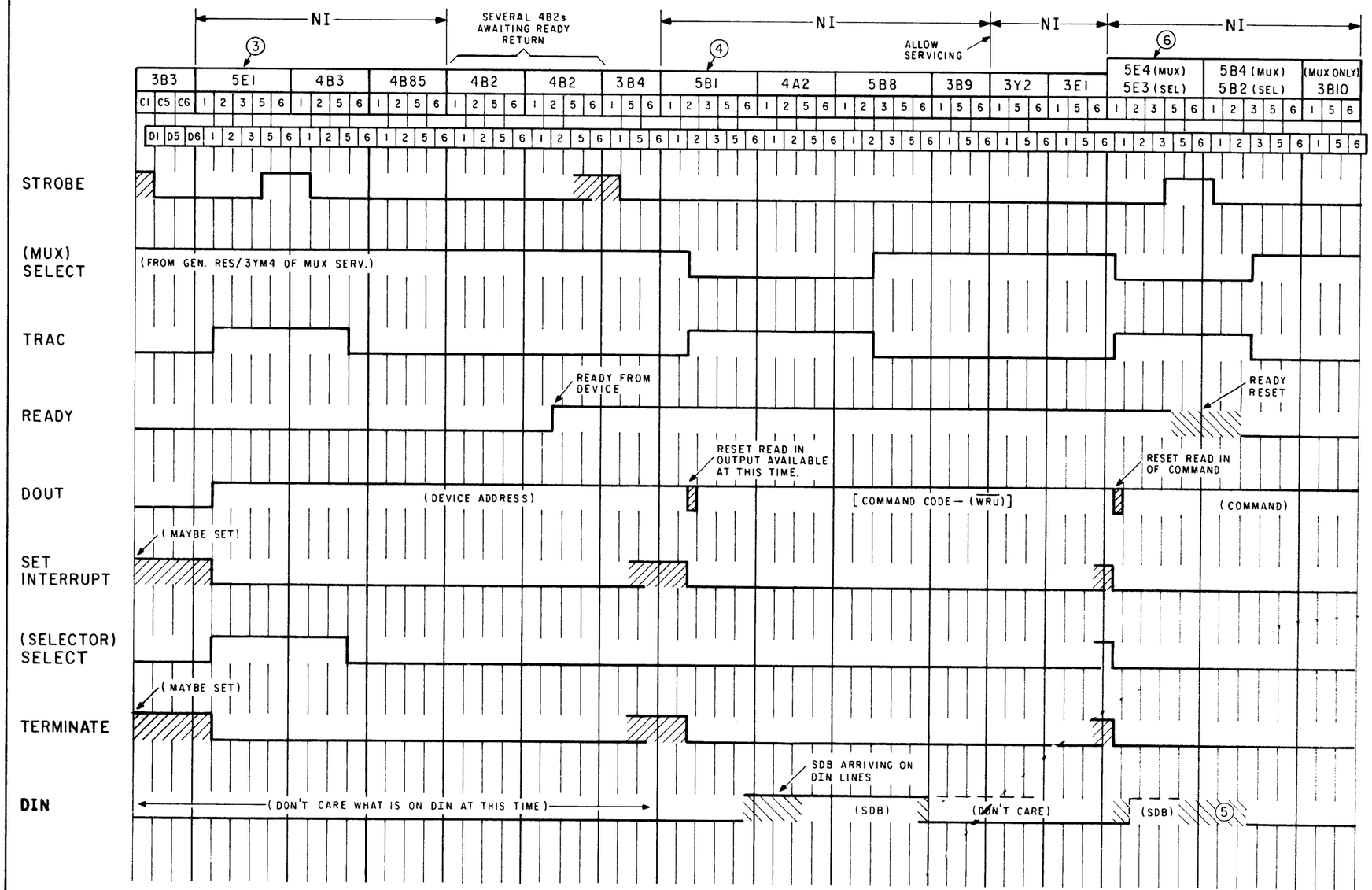
The SETI flip-flop (350-C5D) indicates that a PCI Flag bit has been recognized in a CCW2 word. This flip-flop will be set by the first Servicing STL containing STROBE following storing, for the first time, into Shaded Memory the above mentioned CCW2 word. It is used by the programmer to indicate when a particular set of CCW words have been reached during processing. This line is sent out under STROBE, and ACTIVATE as previously been sent. The CE responds by raising the INTERRUPT line.

The MSTR flip-flop (350-C3B) MUX STROBE, is set in servicing to allow the CE to change its internal state. During Read, it indicates that the byte on DIN has been accepted by the Processor and can be removed by the CE.

During Write, STROBE indicates that the information on the DOUT lines is firm and can be accepted by the CE. This is true for both a Data or Command byte. The STROBE flip-flop is usually set at D5 time and reset by the following C2/C4/C5 time. This results in a 300ns pulse (nominal) going across the Interface from the processor end.

Along the bottom of drawings 349 and 350 are shown the transmitters to drive each of the 9 MUX Trunk Interface lines for the associated FF set. In all of the cases except STROBE and ACTIVATE these lines are ungated. On 350 (bottom right) the STROBE is gated by the MT(X)SEL line of the trunk being serviced and on 349, ACTIVATE is similarly gated. Only the trunk that receives STROBE or ACTIVATE will take any permanent action on any of the other five Interface Control lines or on the DIN or DOUT lines.

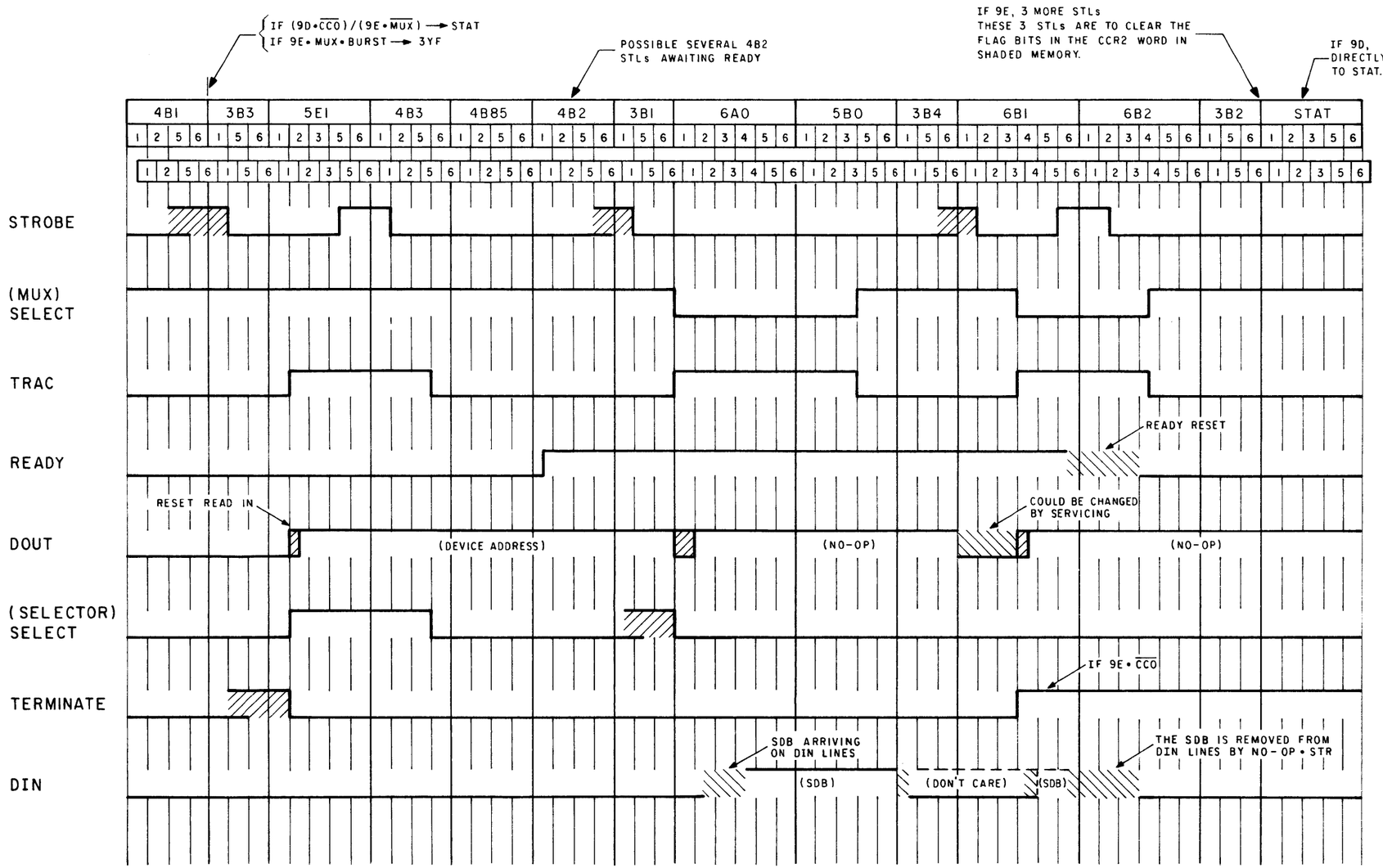
Figures 4-14, 4-15 and 4-16 show the relative timing of the interface control signals during the Initiation or Interrupt Routines of the Instructions.



NOTES:

1. ALL TIMINGS INDICATED BY ////// ARE APPROXIMATE AT BPU END OF INTERFACE.
2. //////└ INDICATES A CONDITION THAT COULD HAVE EXISTED FROM SERVICING HAVING BROKEN INTO THE FLOW.
3. 5E1 STL BROADCASTS DEVICE ADDRESS TO ALL TRUNKS.
4. SENDS COMMAND TO ALL TRUNKS WITH $\overline{\text{STROBE}} \cdot \text{TRAC} \cdot \overline{\text{SELECT}}$. THIS REQUESTS SDB ON DIN.
5. SDB CAN BE REMOVED FROM THE DIN LINES AT THIS TIME AND 2^4 AND 2^5 BITS WILL BE ADDED TO SDB IN CE.
6. SENDING COMMAND TO DEVICE (CE) BEING INITIATED. $\text{STROBE} \cdot \text{TRAC} \cdot \overline{\text{SELECT}}$.

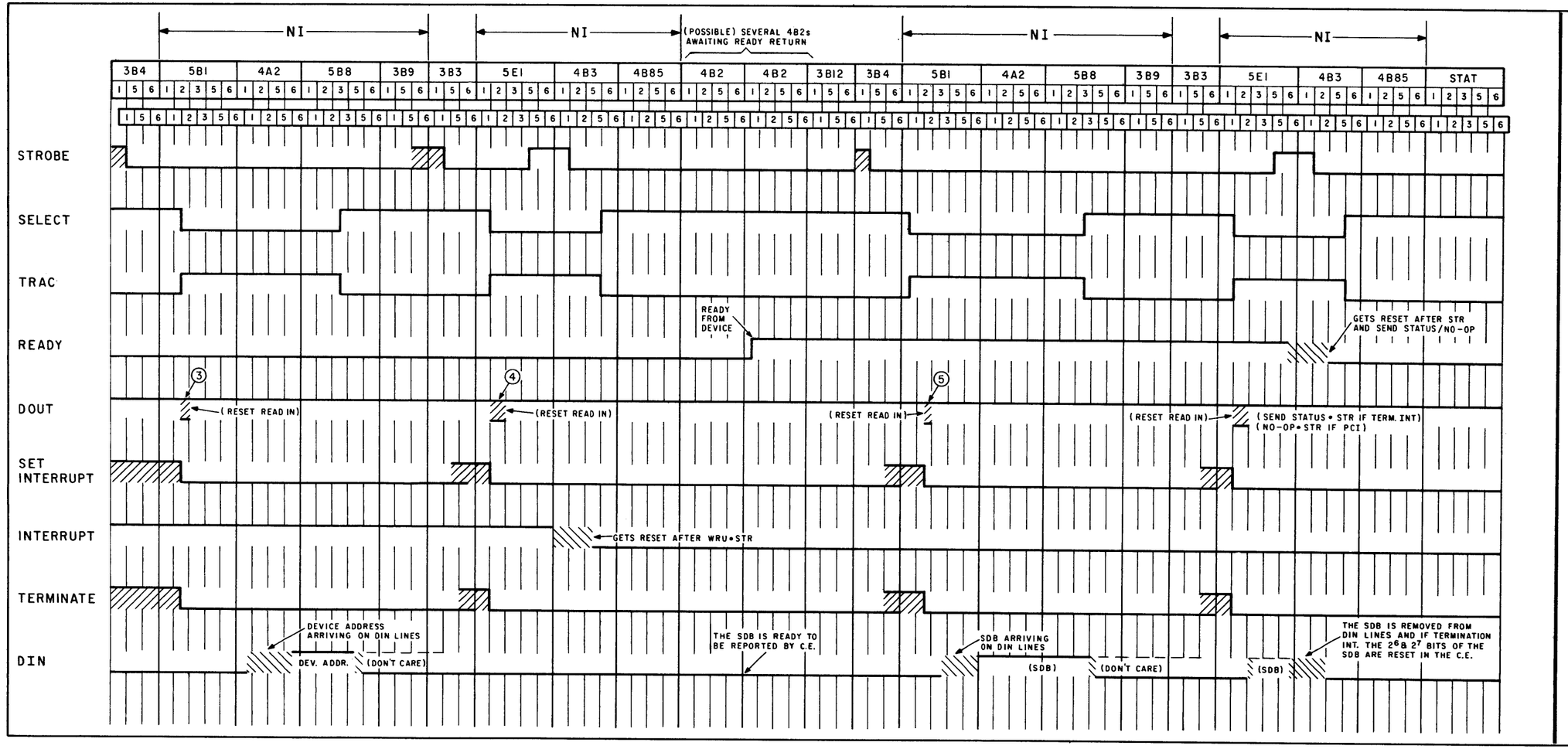
Figure 4-14. Start Device Interface Timing



NOTES:

1. 9E = HALT I/O. 9D = TEST DEVICE.
2. ALL TIMING INDICATED BY ▨ ARE APPROXIMATE AT BPU END OF INTERFACE.
3. ▨ INDICATES A CONDITION THAT COULD HAVE EXISTED FROM SERVICING HAVING BROKEN INTO THE FLOW.

Figure 4-15. Interface Timing, Halt I/O and Test Device



NOTES:

1. NI = NON-INTERRUPTABLE.
2. ALL TIMING INDICATED BY ////// ARE APPROXIMATE AT BPU END OF INTERFACE.
3. WRU • $\overline{\text{STR}}$ REQUEST THE DEVICE ADDRESS ON DIN LINES.
4. WRU • STR REQUEST THE CE TO PREPARE TO REPORT SDB (AWAITING READY).
5. SEND STATUS AND $\overline{\text{STR}}$. THIS REQUESTS THE CE TO PUT SDB ON DIN.
6. //////⌐ INDICATES A CONDITION THAT COULD HAVE EXISTED FROM SERVICING HAVING BROKEN INTO THE FLOW.

Figure 4-16. Pint, Interface Timing

4.3.6.1 READY and END

Interface controls also include the READY and END Receivers and associated logic (see drawing 353). When its END line is raised by a CE, a signal is received by a MUX receiver for the particular trunk involved. The output of this receiver is gated against a MT(X)DIP line which is an Interface line. This DIP (Device Power) line when true indicates that power is on in a CE and that signals on that CE to BPU lines are valid. The output of this receiver gate is conditioned by a MT(X)SEL line so that the resulting output of MTXEND-P signal reflects an END condition on the Trunk currently being serviced. All of these signals are ORed together to form the END-N & P signals (353-B2C). These are used for gating during servicing. The END-P is also ORed with END-SAP from the Selector Channels to form ENDA-N which is used to develop the MRE signal (355-B7B). The END-N signal is also used to light the MEND light on the Console (see 353-A2A). The operator can determine which trunk is being END Serviced (when the machine is stopped in MUX Mode) by observing the MAR address in a SFSP (Single Function Stop) operation on any of the 3YM(X) addressing STLs. This will give the Line Slot address of the Device and this coupled with the knowledge of what Devices are on what Trunks will determine the trunk whose END condition is lighting the MEND light.

When the READY line is raised by a CE, the signal is gated with the MT(X)DIP signal exactly as is the END signal. This is a check to indicate to the BPU that this is a valid signal. The MRDY flip-flop (353-C2B) is set as a result of the READY signal.

The READY condition is tested during Status Level 4B2 to choose the next course of action by the processor. READY or $\overline{\text{READY}}$, the Condition Code, the Instruction, Interrupt Condition and the N Counter are combined to choose the succeeding Status Level.

4.3.6.2 DIN & Control

When information is to be received from an I/O device, (either data, Sense or Standard Device Byte) the particular trunk on which this device is operating has its DIN lines opened exclusively. This is accomplished by the PMDIN logic on drawing 335. The particular STL allows the priming of all the PMT(X)DIN gates (335-B4B) but only the one being Serviced will have an output. This is controlled by the MT(X)SEL signal which is generated by the Service Scanner. The Permit signal is PMT(X)DN which is used to gate in the particular trunk's DIN lines (see Drawing 342) coming off the Receiver outputs. The ORed outputs of the MUX Receivers are called the IOUDIN(XX) lines (see drawing 341). The removal of PMT(X), DN is controlled by D5-BZN (355-B4G) so that no interference with memory addressing occurs in the next status level.

4.3.6.3 MDOUT Register and Transmitters

MDOUT is an eight bit register plus parity bit which is used to transmit Command Code byte, address byte or data byte to a Control Electronics and on to a device. The Control Electronics will interpret which of the three it is by sampling the TRAC and SELECT lines.

The outputs of the MDOUT flip-flops (drawing 339) feed transmitters which are connected to the Interface lines. During Initiation, the MDOUT 2^3 bit can be set directly if a NO-OP condition exists. During termination, either

2^5 (SET INTERRUPT) or 2^6 (SWITCH END) bits can be set directly if either of their respective conditions exist. While performing Interrupt processing, NO-OP (2^3) can also be set at this time. Also the SEND STATUS (2^1 & 2^2) bits can be set directly as well as 2^7 for the WHO ARE YOU condition. These separate sets are shown as SNDOUT 0(X) and SMDOUT 0(X) signals on drawing 339.

4.3.7 MULTIPLEXOR DATA BUS SCHEME

The lBUS is the data link between the BPU and I/O. The 32 bits are fed through inverters to form the IOUBXX lines. These are shown on drawings 335 and 344. DOUTAL (00-08) signals are developed from the IOUDIN (00-08) lines when a 5BMl STL (Read Data Move) is not in progress. DOUTAL (00-08) is also inhibited by a Selector Channel signal, INHIOUB-SP (335-D8B) which can be generated by any status level checking parity on incoming data. The I/O Commands that send data to the BPU IBUS are RODIN (351-A5D) and RODRP (351-B8C). These are both combined with the CSC logic (Character Select) which is formed from the IOCAD logic (see 351-A5C, etc.). The LSR, XMAC and INR are non data registers which also communicate with the BPU via the IBUS.

Figures 4-17 and 4-18 are simplified logic diagrams which trace the data from I/O to memory during a READ operation and from Memory to I/O during Write operations.

4.3.7.1 Parity Checker/Generator

Information arriving from a device in READ is received on the DIN lines and among other places this is sent to the Parity Checker (335). The DOUTAL0(X) signals are decoded and checked for odd parity. If the number of bits is even, IOPE (335-B7D) is generated and if the operation is not a SENSE (see 335-B5B) then the IOPE flip-flop (335-A4B) is set during the 5BMl STL (Read Data Move). The IOPE light will light and if ALI is on nothing else will happen. If ALI is not on, IOERR will be generated (335-A5B) and sent to 321-D5D where it will set MESP flip-flop if the MESP switch is on. This will stop the machine by allowing RUN FF to be reset at C6 time (322-B6D). If the MESP switch is off, the MESP FF will not be set and the machine will continue to run but the MDATACK flip-flop (343-C6A) will get set as a result of MERRl-P being generated (335-B6A) due to the parity error and ALI off. In the Write case, parity is checked while the byte is on the lBUS (335) on its way to the MDOUT Register. If the number of bits is even, the 2^8 parity bit is generated as DOUTAL 08 (335-A7A) which is also sent to MDOUT.

The IOERR signal also forces all bits (2^0 - 2^7) on the IOUDIN lines to give the indication of an FF representing a parity error (see drawing 341).

4.3.7.2 Multiplexor Channel Status Register, MTERANY & STMCSR

The Multiplexor Channel Status Register (MCSR) consists of seven flip-flops (drawing 343) used to store various error, terminating and program controlled conditions. The individual flip-flops are set independently by several different STLs during Servicing, depending on what conditions are being checked. There is a time when all will have a common gating pulse attempting to set them. This occurs during the 4DMl STL when the CCW2, arriving from shaded memory, is stored in the MUX Scratch Pad Servicing location for the word. The Cl character of this word contains the accumulated

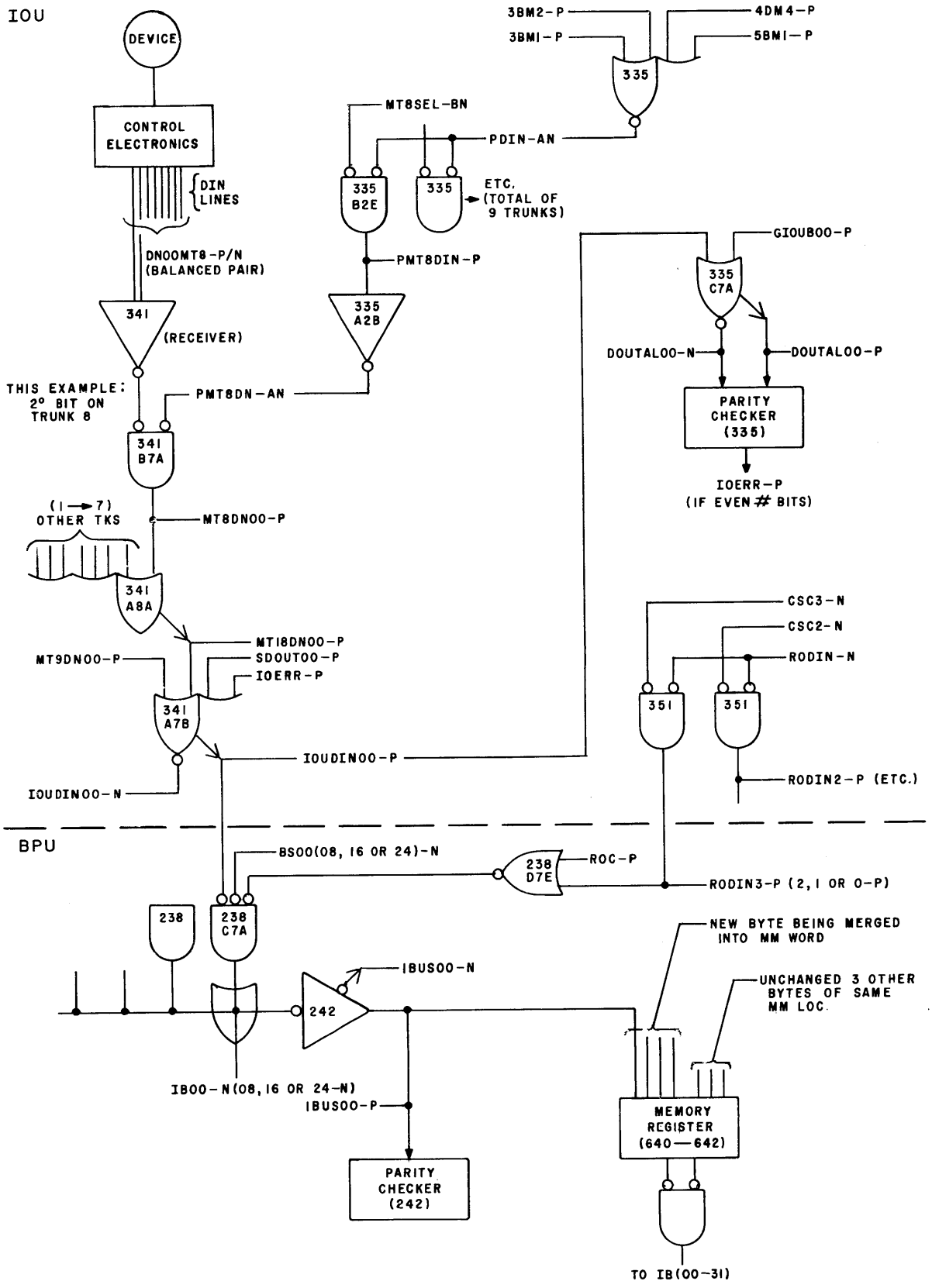


Figure 4-17. Multiplexor Read Data Flow

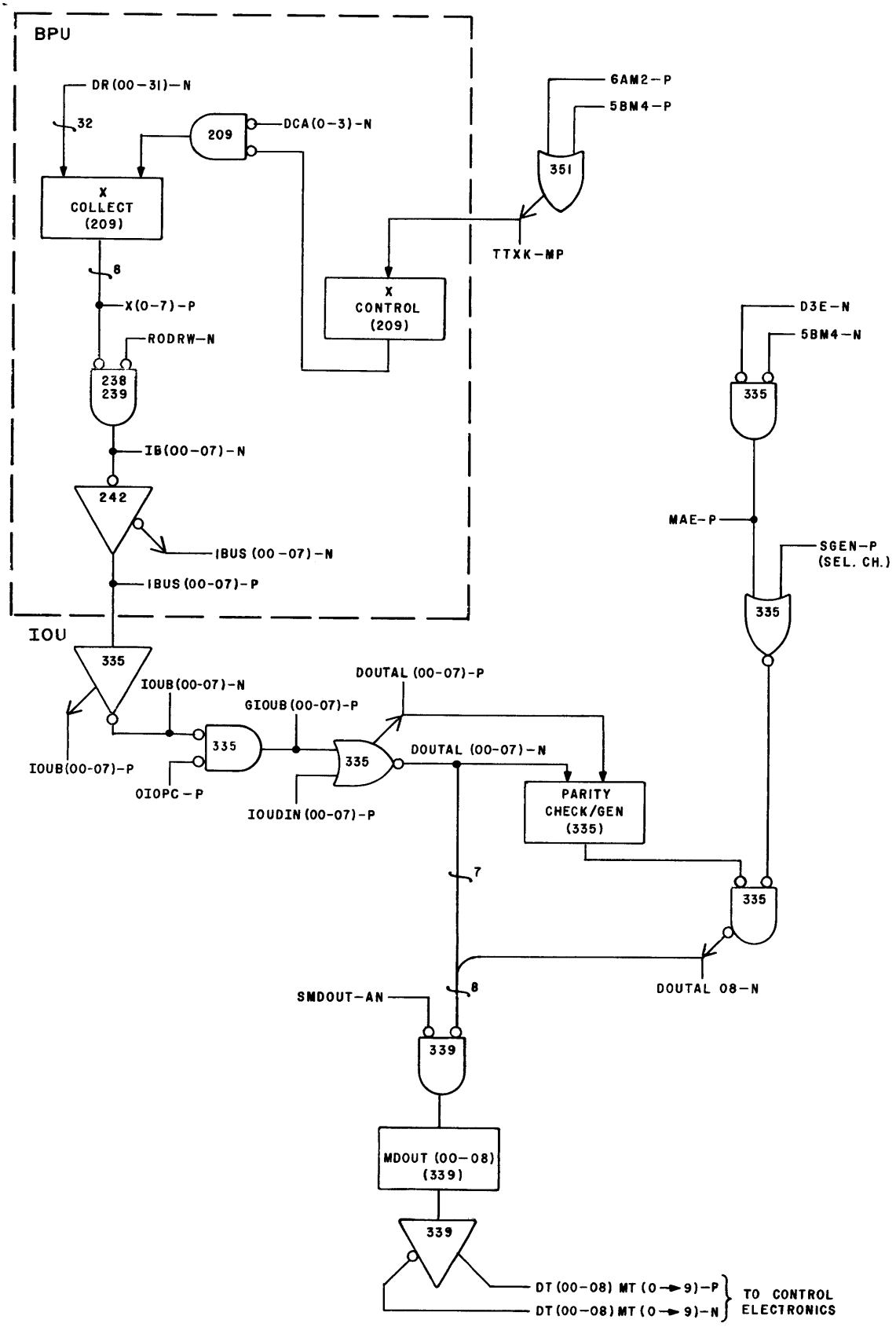


Figure 4-18. Multiplexor Write Data Flow

Channel Status Byte bits up to this point in servicing the particular instruction. These bits are gated into the MCSR from the bus, IOUB(XX). Any additional bits added during Servicing will be superimposed and the entire group stored back in the CCR2 location in shaded memory at the completion of each byte of Servicing.

A brief explanation of the meaning of each FF in the MCSR follows:

1. MEND (343-C7A) is set whenever a Set Interrupt Command is to be sent to a device. It says that the Interrupt was a termination type.

2. MPC1 (343-C7B) is set whenever the PCI Flag bit (2^{27}) is contained in the CCW2 word being fetched from main memory in the case of BURST/CATSUP or from shaded memory in regular Servicing. MPCI is not set when MUX END signal is present.

3. MDATACK (343-C6A) is set by a MMPE (Main Memory Parity Error) during either Data Move STL (5BM1 or 4) or by a parity error on the data arriving from an input device.

4. MINCLTH (343-C5A) is set if during END Servicing a check is made in the 4DM1 STL or 4DM4 STL (for BURST/CATSUP) for a count other than zero remaining in CCR2 word or CD (Chain Data) flag bit set. If there is a count or CD bit present, MINCLTH FF will be set when not in BURST/CATSUP provided the SLI Flag bit is not present and the operation is not a LOAD. In BURST, this FF will be set only if MSE (0) (MX Switch End condition not present).

5. MPROTCK (343-C4A) will be set during the Data Move Main Memory Addressing STL (5ZM1) if the Key bits disagree with those previously set up in memory. This only occurs if the Memory Protect feature is installed. If the Keys associated with the current processor state and those related to main memory block are equal or either is zero, the main memory block accepts a data store.

6. MCONTCK (343-C3A). If either a SPME (Scratch Pad Memory Error) or a MMPE (Main Memory Parity Error) occurs when reading out a CCW1, CCW2 or CAR, this FF will be set. This is checked in all the STLs that perform SP and MM Reads.

7. MPROGCK (343-C2A) is set in the 5ZM1 and 2 STLs if the memory is addressed beyond its maximum location. It can also be set in 4AM2 STL (CAR SP Store) if the CAW (Channel Address Word) contains any bits in 2^0, 2^1 or 2^2 which says that the address contained in the CAW is not a double word address specifying the next CCW1 word location. The 5AM STL (Transfer in Channel) will set this for the same reason as 4AM2, since the address portion of a Transfer in Channel CCW1 word contains the address of the real CCW1 (or another Transfer in Channel word).

MTERANY (MUX Terminate Any) (344-C6A) is generated if any of the following conditions exist: MPROTCK, MPROGCK, MCONTCK, MDATACK and WRITE or END, and END with MINCLTH.

MTERANY signifies that an error has occurred of the type that makes it necessary to stop the operation since the results will not be valid.

1. In 5BM1, 3YM3 and 4AM2 STLs, TERMINATE will be Strobed out if MTERANY is present.

2. In the Command Chaining path, SET INTERRUPT Code will be Strobed out in 6AM2 STL if MSE (0) and MTERANY (1).

3. If the MUX is operating in BURST or CATSUP and MTERANY occurs, the BURST/CATSUP STL loop will be broken and forced to take the normal exit path thru 3YM3, 4BM1, etc. where TERMINATE will be Strobed out in 3YM3.

The STMCSR flip-flop (344-C2B) can be set by either 3YM4 or 4BM2 STL provided there is a SPME or SMPROGCK-NP, the latter of which is formed by the fact an area of memory was addressed which does not exist on the particular system. When STMCSR is set, the MUX will not return to Normal out of 4BM2 status level, but selects 3YM4 STL. This STL does a Store Status function, e.g., it takes all the bits contained in the MCSR and stores them into C1 character of the CCW2 word. The 4DM1 STL also performs a Store Status function as explained above under MCSR, MTERANY and STMCSR. Since these two STLs (4DM1 & 3YM4) perform natural Store Status functions during Servicing, the only conditions required to set the STMCSR flip-flop are those which would set a bit into the MCSR when it is too late to be stored in the CCW2 word by the 3YM4 STL. This would occur in the 4BM2 STL (which follows 3YM4) and also if the 3YM4 STL itself has a SPME or $\overline{\text{MIP}}$ condition which will arrive too late to set the MCONTCK FF in time to be stored into the CCW2 word.

4.3.7.3 FLAG, COMMAND, KEY And MCAD Registers

The command code is contained in C0 of the CCW1 word (2^{31} -- 2^{24}). There are seven possible I/O Commands and they are specified by bits 2^{24} -- 2^{27} or the least significant digit of C0. The Command Code Operations are shown below. The M bits are the modifier bits used by the CE and the B bits indicates that if the specific device is connected to the Multiplexor Channel, it is to be operated in the BURST mode. This bit is checked only in initiation, however and is ignored afterwards in chaining, etc.

Command Code	Operation
MMMM 0001	SENSE
MMMB 0010	READ REVERSE
MMMB 0011	WRITE
MMMB 0100	WRITE ERASE
MMMB 0101	READ
MMMM 0111	WRITE CONTROL
MMMM 1001	TRANSFER IN CHANNEL

During Servicing of each byte (except in BURST or CATSUP), the Command Register (drawing 338) is set up by the right most 4 bits. The decoded outputs of the 4 Command Register flip-flops specify whether the operation is a MUX SENSE, READ or REVERSE (REV). A Write, Write Control or Write Erase will have no decoded output. These outputs or the lack of them are used for gating during servicing. Indicators on the Maintenance Panel show which decoded command is present. During Data Chaining these flip-flops are used to insert the current Command Code into the new CCW1 word arriving from main memory. This is done in the 5BM2 STL (Chaining Fetch A STL). During the time the new CCW1 is on the bus (ROMRW Command) in this STL, the MT/C (336-A2A) (MUX Transfer in Channel) flip-flop will be set if the decoded output of the IOUB equals 1001 which is the T/C Command Code. The outputs of this flip-flop are used to control the selection of the T/C STL (5AM0). The Key Register flip-flops (338) are set from IOUB31 -- 28 at the time the CCW1 word is being stored in Scratch Pad from Shaded Memory. The purpose of these bits is to ensure that data is not being transferred to a protected memory area. This only applies if the memory protect feature is installed in the system. If it is not installed in the system, these Key bits must be zero.

The Flag bits are contained in 2^{31} -- 2^{27} of the CCW2 word. They have the following significance:

2^{31} -- Chain Data Flag (CD), allows using different sectors of main memory in the same operation.

2^{30} -- Chain Command Flag (CC), when set indicates that at least one more I/O command is to follow

2^{29} -- Suppress Length Indicator Flag (SLI), if set, will not permit an indication of an incorrect length upon termination.

2^{28} -- Skip Flag (SKF), inhibits the transfer of data to main memory. Can be used only with Read, Read Reverse or Sense Commands.

2^{27} -- Program Controlled Interrupt Flag (PCI), causes a channel interrupt to occur when servicing the first byte after having fetched the CCW2 word from main or shaded memory.

These bits are set into the Flag Register (336) when the CCW2 word is brought from shaded memory for storage into Scratch Pad.

The MCAD Register consists of two flip-flops on drawing 336. Its function is to specify which byte of a word is being transferred to or from memory so that this byte can be selected from or merged into the remaining three bytes. The register is set from IOUB00--01 of the memory addressing STL (5ZM1) since these are the two bits which specified the byte address of a word. When both are reset (00), character 0 is specified; 01 = character 1 and so forth. These flip-flops are indicated at the Console by the "IOCAD" lights when the machine is in MUX Servicing.

4.3.7.4 Miscellaneous Control Flip-Flops & Termination Status Decode

The MCC, MSE, MSI & MSM flip-flops are set during END Servicing when the SDB (Standard Device Byte) is decoded. If Command Chaining is called for, MCC will be set. MSE is set for a Switch END condition, MSI for a Set Interrupt condition and MSM if the Status Modifier bit (2^0) is contained in the SDB. The DIN lines (see drawing 355) are decoded and set the MCC, MSE, and MSI flip-flops as explained above.

A brief explanation of the meanings and reasons for these conditions is as follows:

1. MCC (352-C7B) - Command Chaining will be permitted only if all of the following conditions are fulfilled: (a) CC and $\overline{CD}$ flag bits (b) $\overline{Load}$ and (c) Device End condition is reached which is 2^3 bit on the SDB and not 2^1 or 2^2 bits which are Device Inoperable and Secondary Indicator bits respectively.

2. MSM (352-C4A) - If all the above conditions are met and the SDB contains 2^0 bit (Status Modifier) MSM will be set and the new CCW words will be taken from a location whose address is two words higher in MM than the one which is in the CAR word at the beginning of the Chaining operation.

3. MSE (352-C5A) - If the SDB contains 2^5 bit and $2^{\overline{1}}$ and $2^{\overline{3}}$ and $\overline{LOAD}$ the device is busy and the MSE condition is recognized. This signals the CE to do a Switch End which means to drop the END line and bring it up again later with another SR when the Device End condition has been reached (for example a Tape Device in rewind).

4. MSI (352-C5B) - This is developed by various combinations of bits on the SDB along with CCF or $\overline{CCF}$ conditions (see 355-A6A, etc.). This MSI condition, when later Strobed out in 6AM2 STL, will signal the CE to raise its INTERRUPT line because the current SR has been completely finished.

The MHALT flip-flop (352-C2B) is set during Initiation of a HALT DEVICE Instruction. It is used normally to condition the setting of TERMINATE during Initiation. However if the MUX is operating in BURST mode, the TERMINATE flip-flop (350-C7D) is set during the next SR Servicing (see 350-D7B).

MZ (352-B7C) is the Multiplexor Zero which is normally set in either 4DM1 or 2 status levels if the byte count has gone to zero. MZ is also set during END Servicing of a LOAD function if the SDB has the 2^2 bit set (Secondary Indicator). The reason is that the MZ flip-flop is used in 4BM2 STL to cause the setting of IOPE and the resetting of RUN and LOAD flip-flops during a LOAD since the entire LOAD is considered bad if a Secondary Indicator occurs.

A/T flip-flop (352-B6F) refers to an old designation of CCW1 word being called the A word and CCW2 the T word. It is set in the 5ZM2 if 2^2 bit is present in the Main Memory Addressing bits. Since all CCW1 words must be located in a double word address, the CCW2 word will be a single word address in which 2^2 bit is present ($2^{\overline{0}}$, $2^{\overline{1}}$). The 5ZM2 STL is used to address both the CCW1 and 2 words in successive passes through this STL and the

condition of the A/T flip-flop determines whether to select the Fetch A (5BM2) or Fetch T (3AM3) STL. This flip-flop also conditions the sending of STROBE, SET INTERRUPT and TERMINATE signals in the 4BM1 STL (Store A). The reason is that if A/T is set at 4BM1 STL time, the MUX has just been through the Chain Data/Chain Command Servicing loop and would have sent the aforementioned Interface signals for the SR during the 4AM2 STL of this loop.

INHINCL (352-C6A) is used to condition the setting of the MINCLTH (343-C5A) during the 4DM4 (Command Decode) STL. If during BURST operation, an MSE condition is decoded during the 4DM4 STL, the INHINCL flip-flop will be set, inhibiting the generation of COND4DM4 (352-C6B) and preventing the MINCLTH flip-flop from getting set.

4.3.8 BURST & CATSUP

The Multiplexor can be made to service a device in BURST by the BURST bit being contained in the CCW1 word at the time of initiation. Whenever a device is being operated in BURST, all other devices on the MUX are blocked out and cannot be serviced until that operation is terminated. However, any Selector Channel can break into the BURST with a SR at the completion of each byte transfer.

The BURST flip-flop (332-B5A) is set during initiation if the BURST bit (2^4 of C0 of CCW1 Word) is present. The setting of BURST causes the following:

(1) Inhibit generating MSINT by the ROLLS path (332-B8B).

(2) Permit MSINT by the ROYCE path (332-B7B).

(3) Inhibit MSP-AN; BN (332-A5A).

(4) Raise the BUSY line (332-B4B).

The MSCANSER signal (332-B7A) is used for BURST and CATSUP operation. MSCANSER indicates that for BURST there is a SR on the trunk in BURST, or for CATSUP there is another SR on the trunk still being serviced which arrived at or before the Data Move STLs (5BM1 or 5BM4). When this latter condition occurs, the CATSUP flip-flop (332-B2A) gets set.

At initiation time the MT(X)SCAN will get set for the trunk being initiated (BURST or $\overline{\text{BURST}}$). If the BURST is set, it inhibits any MSP-AN; BN (332-A5A) pulses for the entire BURST operation. Thus the MT(X)SCAN flip-flop for the trunk in BURST will remain set awaiting the arrival of a SR at any time to develop the MSCANSER signal (332-B7A).

Once either BURST or CATSUP flip-flop is set, the 4DM2 STL is selected out of the 5BM1 or 5BM4 (Read or Write) STL. The STL will decrement the count by one and Strobe out the byte. Out of this STL, Normal is selected in the BURST case and 5ZM1 preselected or 5ZM1 (Data Move Main Memory Address, STL) in the CATSUP case since this has another SR awaiting Servicing.

If an Interrupt is still pending on any MUX Trunk at the time a BURST is being initiated, the BURSTP flip-flop (352-C8A) is set. This will force

a condition code of 2 which will set CFF2 and prevent the BURST FF from getting set later in the Initiation flow. This flip-flop will be reset automatically at the beginning of the Initiation flow each time, and if there are no MUX Interrupts still pending, BURST will be allowed.

4.3.9 MULTIPLEXOR OPERATIONS

4.3.9.1 Load Function

In order to store the Program into main memory, the LOAD function is normally used. This is accomplished by setting up the Channel and Device number on the DIGI switches on the Operators' Console, and after hitting GENRES, pushing the LOAD button. Functionally:

1. Processor initiates a READ Command.
2. The Memory Address is set to 0.
3. The CCR2 word count is set to maximum (all 0).
4. The CCR1 & 2 words are stored in Shaded Memory and the Device is started.

This portion of the process is the initiation. Logically, the LOAD button sets the LOAD flip-flop (352-C2A) and during Initiation the LIP (Load In Process) flip-flop (352-B4D) gets set. The LIP-1P signal inhibits the setting of PNM (289-D3B) until the Load is complete. LIP flip-flop is reset during the last STL of END Servicing if a SET INTERRUPT (MSI) condition was recognized. The LOAD flip-flop is reset by two different paths in the MUX. On 352, D2A gate will reset the LOAD flip-flop if an error occurred during the Servicing of a LOAD. On gate D2C, the RNLOAD-P signal (generated at 326-D1A, etc.) is used to reset the LOAD flip-flop under either of two conditions:

1. LOAD was completed normally and the next instruction staticized will generate HKRE which generates the RNLOAD signal.
2. An error or incorrect Condition Code was detected during the Initiation of a LOAD or START DEVICE Instruction. This also develops RNLOAD.

When SRs arrive, they are handled the same as in non-Load operations. The Device will continue until a gap is reached in the case of Tape Stations, Drum, Disc, etc. or until one card has been read in the case of the Card Reader. At this point, the END line is raised by the CE along with SR. Since the maximum count of all 0 was set in the CCR2 word, there will be a residual count remaining when END is raised. In order to avoid an incorrect length indication (setting MINCLTH flip-flop), the gating of the setting of MINCLTH flip-flop is inhibited (343-D5D) by LOAD-P. If any errors occur during the Load, the 2^2 bit (Secondary Indicator) will be contained in the SDB. The SDB is sampled during END Servicing and this along with the signal MRE-N (355-A7A) and the signal RIMIR (352-B8A) will set the MZ flip-flop (352-B7C). The MRE signal is developed because END was received during a LOAD.

4.3.9.2 Multiplexor Servicing

Once a device has been Initiated, all the conditions necessary to accept Servicing have been prepared in the I/O area of logic of the BPU. The CAR, CCR1 and CCR2 words have been stored in Shaded Memory in the Line Slot of addresses associated with that particular device. The machine now awaits the arrival of a Service Request (SR) to start the Servicing flow. Functionally, the order of events with the arrival of a SR on the Multiplexor is as follows:

1. The SR is stored in the MT(X)ULSC flip-flop associated with its trunk. A signal (MSINT) is sent to the BPU.

2. If the Selector Channel is not being Serviced, the highest priority Trunk on the MUX with a SR stored in its ULSC flip-flop will be accepted for Servicing. This will start at the end of the next interruptable STL ($\overline{NI}$) in the Normal Mode. If a Selector Channel had been in Servicing at the arrival of a MUX SR, the MUX would be held off until the completion of Selector Servicing and also any SRs awaiting Servicing from any of the other Selector Channels.

3. Upon entering the Servicing flow, the ACTIVATE signal is sent to the CE to suppress the SR. The device address is on the DIN lines and it is stored in the LSR (Line Slot Register).

4. The LSR and XMAC information is sent to Shaded Memory first to fetch the CCR1 word and then the CCR2 word. These are stored in Scratch Pad in the MUX Servicing locations. At the same time the MUX Key, Command and Flag Registers are being set from the information contained in the two words. Also, the CSB (Channel Status Byte) contained in the CCR2 word is stored in the MCSR (MUX Channel Status Register). If the PCI Flag bit is present, a special PCI flip-flop in the MCSR will be set at this time. The SELECT line is reset so that Data can be placed on the DIN lines if the operation is a READ.

5. The data address contained in the CCR1 word is shipped to Main Memory and if a READ is indicated, the data byte on DIN is merged into the word brought from Main Memory, if the SKIP flag is not set. The byte is placed in the character location specified by the CSC logic (351-A5B, etc.) and the entire word is returned to Main Memory. If WRITE is indicated, the CSC logic determines which byte to select from the Main Memory word which is sent to the device on the DOUT lines accompanied by STROBE. When STROBE is sent in the READ case, it signifies to the CE that the data byte has been taken from the DIN lines and DIN may be changed.

6. During the STL in which the DATA is being moved to or from Main Memory (5BM1 or 5BM4) the ULSC (Upper Level Scan) flip-flop of the Trunk being Serviced is checked for the arrival of the next SR. If present, the CATSUP flip-flop (332-B2A) is set. If CATSUP is set, or the operation is being done in BURST, then a special Status Level loop is entered. The 4DM2 STL is selected (Non-Interruptable) which subtracts one from the byte count, in advance, from

the CCR2 word. 4DM2 selects the 5ZM1 STL (Data Move MM Addressing) and if in BURST, resets the XAC flip-flop (289-C8C) to permit return to Normal mode processing, awaiting the next SR. If in CATSUP, the next SR on this Trunk is immediately Serviced unless a Selector Channel breaks in for Servicing. In BURST, this loop will continue until the operation is completed. In CATSUP, this loop will continue only as long as the CATSUP continues to get set by the conditions mentioned above.

7. The 3YM3 STL will be selected out of the Data Move STL (5BM1 or 5BM4) for the following cases:

   (a) $\overline{\text{BURST}}$, $\overline{\text{CATSUP}} \cdot \overline{\text{MZ}}$ (not 0 count);

   (b) At the completion of the BURST;

   (c) The count has been decremented to "0" (MZ gets set) and $\overline{\text{CD}}$;

   (d) MTERANY type error occurs;

   (e) or a HALT Instruction is Initiated to the same device.

   The last four STLs of MUX Servicing (3YM3, 4BM1, 3YM4 and 4BM2) takes the CCR1 and CCR2 updated words out of the Scratch Pad and stores them back into Shaded Memory. The MCSR (MUX Channel Status Register) is stored in the CCR2 word and the SELECT flip-flop is set during the 3YM4 STL. Thus, the accumulated results of all the SRs to date are maintained in the CCR2 word and the CE is alerted to prepare to have the device address on the DIN lines (with the next SR) by the raising of the SELECT line.

8. If the Chain Data Flag bit (CD) is present and the count goes to zero, the path out of the Data Move STL (5BM1 or 5BM4) is into the Data Chaining Loop of STLs starting with 3YM5. Functionally, the following occurs:

   (a) CAR word fetched from Shaded Memory and stored into Scratch Pad. (3YM5 & 4AM2).

   (b) The address portion of the CAR word is used to address Main Memory and fetch the new CCW1 word which is stored in Scratch Pad with the Command and Key Registers being inserted into C0 location (5ZM2 & 5BM2). The Command Code of this new CCW1 is examined to see if Transfer in Channel (T/C) Command is indicated. If it is, this word is stored in the CAR Scratch Pad location (5AM0) and the address portion of this word is sent to Main Memory and another new CCW1 is stored in Scratch Pad, again checking for a T/C Command. If $\overline{\text{T/C}}$, the now updated address of the CAR word is used to fetch the new CCW2 word and store it in Scratch Pad. (5ZM2 & 3AM3).

   (c) The CAR word is stored back in Shaded Memory with the device word inserted into C0 location (3YM5 & 6AM1) and both the new CCW words are stored back in Shaded Memory with the regular 4 STL store path mentioned under 7.

9. When the count goes to zero and CD, the TERMINATE flip-flop (350-C7D) is set and is strobed out with STROBE (350-C3B). The next SR will come with the END line raised. The END could have been raised by the device CE if, for example, a gap had been reached on Tape during a READ or one card read in from the Card Reader etc. If the END is a result of the BPU (MUX) signalling the CE or if it is raised by the device when not operating in BURST or CATSUP, the regular servicing flow is entered, e.g. through the 3BM1 (Dummy) STL. If the END is raised by the device while in BURST or CATSUP, the path is different as explained below:

   (a) Regular End Servicing - The usual SR flow is 3BM1, 3YM1, 3AM1, 3YM2 to 4DM1. This group, fetches the CCR1 & 2 words from Shaded Memory. With END, however, the byte count subtraction is inhibited in 4DM1 and the END Dummy STL (3BM2) is selected. When the SR and END arrived, the DIN lines contained the device address. During 3YM1 STL, the SELECT line was reset thus indicating to the CE to remove the device address and place the SDB on DIN. In the 3BM2 STL, this SDB is decoded for such conditions as CC, SE, SI etc., and the appropriate flip-flop is set. From 3BM2 STL, if $\overline{CC}$, 6AM2 is selected which strobes out the command. If in $\overline{BURST}$, the regular 4 exit STLs are then selected to store the CCR words in Shaded Memory. If the CC (Command Chaining) condition is decoded in 3BM2 STL, the path is now the same as explained under (8) for the CD path. If, however, during 3BM2 the Status Modifier (SM) bit was present in the SDB (2^0 bit), the MSM flip-flop is set. In the 4AM2 STL with MSM set, the CAR address has 4 added to it (1 word). Out of 4AM2 the 4DM3 STL (CAR +4) is selected for this case only and the CAR word is advanced 1 more word. This now permits obtaining the new CCW words from a location 2 word addresses higher in Main Memory. The remainder of this path is the same as the CD path. The 6AM2 STL sends out the new Command to the device.

   (b) BURST/CATSUP END Servicing - If while in the loop (5ZM1, 5BM1/4 and 4DM2) the END is raised by the device, the exit from 5ZM1 will be to 4DM4 (Command Decode STL). Also in 5ZM1, the END condition will prevent incrementing (forward) or decrementing (reverse) the address. In the 4DM4 STL, the SDB is decoded and the count is incremented by one (CCR2 word) because in the 4DM2 STL (T-1 STL) the count was decremented in anticipation of servicing another byte and thus the count must now be corrected. Next, if not CC the 6AM2 STL is selected and the Command is Strobed out. If Command Chaining, the same apply as for (a) above. If in BURST, 5BM3 STL is selected; its main purpose is to reset TRAC in time to allow the CE to get data on the DIN lines (or SDB in case of Switch End) in time to be used in the BURST/CATSUP loop.

   CATSUP will be reset at this time since this occurred in 5ZM1 just before selecting 4DM4 STL. Thus, even if this path had been entered due to CATSUP, from 6AM2 STL the regular 4 exit STLs will be selected (3YM3, 4BM1, etc.).

4.3.10 SELECTOR SERVICE SCANNER AND CONTROL

Prior to servicing the Selector, the SSCNCPT flip-flop (359-B7A) must be set. This happens at GENRES or at the completion of a previous servicing. If other conditions are met, such as the NI (Non-Interruptable) flip-flop is not set or the FR (Function Repeat) switch is not in the ON position, the SSP-N signal (359-B7C) is generated.

The Selector (1 through 6) Service Scanner is shown on drawing 360. Only the individual channels are scanned since only one of the four trunks permissible on a channel will have its SXTXRDY flip-flop set. The SXTXRDY along with a service request (SR) from that trunk are the requirements for setting the SXULSC flip-flops. The SSP-N signal gates the jam set/reset input gates of the SXSCAN flip-flops which are primed by the SXULSC flip-flops. The priority is from Selector 1 through 6 inclusive with Selector 1 having the highest priority. The priority is established by the SXULSC flip-flop which is set and which has the highest priority inhibiting the lower priority channels (using the SXULSC-1P to inhibit all the lower order SXSCAN set input gates). When the SXSCAN flip-flop gets set, it develops the SXSEL-AN:BN:CN:DN:AP:AAN:BAN signals which are used for gating throughout the Selector logic.

The Selector will signal the BPU that it wishes to do Servicing by sending a signal called SPSM-N and P (360-A2A). This signal is formed by the ORed output of SXULSC flip-flops gated with NI-1P (indicating a normal or Multiplexor Non-Interruptable Status Level) and SRTINH1-1P (359-C3B), whose function will be described later. SPSM goes to the Mode Switching Control (289-D6A, D5A, D3B) where it sets the PSM flip-flop and inhibits the PXM and PNM. PSM in turn allows the SM (Selector Mode) to get set and these two flip-flops drive power inverters to supply all the required PSM and SM mode levels necessary to cause the machine to operate in the Selector Mode. At C1 time of the first STL in the Selector Mode, the SSCNCPT flip-flop is reset.

The output of the SSCNCPT flip-flop is inhibited from exiting from SM if an error was detected during the servicing which caused the QSTCSR flip-flop (359-C2A) to be set. During the storing of the new Channel Status in the 4AS3 STL, the SSCNCPT flip-flop is set again. Providing that the FR switch is not on, the RSM-P pulse resets the PSM flip-flop (see 289-C6B).

If during servicing either the STERM or SSETI flip-flops are set for any reason, the SRTINH1 flip-flop (359-C3B) is set in the same status level as STERM or SSETI. This has the effect of inhibiting the scanner for one status level if that status level was the one which would set the SSCNCPT flip-flop. This is done by inhibiting SPSM if SRTINH1 is set. If the status level was not the last one before exiting from servicing, then no scan time loss would be involved.

This logic allows time for the standard device byte (SDB) (in the case of the Set Interrupt or the SR in the case of the Terminate) to be transferred across the interface, change information or state in the Control Electronics and also have time to echo back to the I/O. This is accomplished by setting the SRTINH1 flip-flop at C5M time of the STL (gates 359-C4A, C4B) in which SSETI or STERM were set. At D1L time of the next STL the SRTINH2

flip-flop (359-B3B) is set if SRTINH1 is set. The SRTINH1 FF is reset at C1M time if SRTINH2 is set (359-C3A).

The Selector Scanner is different from the MUX scanner in one respect. Each SXSCAN flip-flop has an associated SXSTRC flip-flop which sends the STROBE to the trunk on the channel which is being serviced. By using this flip-flop to control the STROBE, the SXSCAN flip-flop can be reset to service another Selector while sending the STROBE to the one previously serviced. The SXSTRC flip-flops are set at D2M time if the SXSCAN is set. All SXSTRC flip-flops are reset at C2M time of any STL that sends STROBE (360-B2C).

4.3.11 SELECTOR STATUS LEVELS

When a SR arrives and develops SPSM and when Selector Servicing is allowed, the first STL of Servicing must be developed. Once this STL is formed, all of the remaining STLs are preselected by the exit conditions of their immediate predecessors. The development of STLs is as follows:

1. The current STL develops the SSXXnxSn signals (drawing 364):

   a. SS = Selector Servicing

   b. The first X of XX = Setting of SLSPA

   c. The second X has no significance

   d. nxSn = Selector (S) STL designation (for ex., 5ZS1).

   SLSPA (Selector Scratch Pad Addressing) is explained under the section Scratch Pad Use and Locations and SLSPA (see 4.3.12).

2. The SSXXnxSX signals are used to set the SLSPA flip-flops on drawing 379. The SSXXnxSX signals are also used for gating the setting of the SPSTLXX flip-flops. These form the Selector Pre-Status Level Register (see drawing 361). They are set at C6M time of the STL just finishing. The 1N outputs of the Register gate the setting of SSTL XX register flip-flops at DD6 time of the same STL.

3. The 1P and 0P outputs of the above two Registers decoded to form the PSTLs and STLs. On drawing 362, the SPSTL XX signals develop the SPSTLXXX signals. These in turn are combined to develop the actual PSTLs. The same scheme holds true for the actual Selector STLs (drawing 363). The Pre and Regular STLs are used throughout the Processor to gate signals used in the execution of the Selector STLs. The PSTLs are used when signals must be developed early for the incoming STL. They are available from D6 time of the exiting STL until D5 time of the incoming STL. The STLs are available (firm) from D1 thru C6 time of the STL.

The FRSW (Function Repeat Switch), when depressed will prevent the resetting and setting of the SPSTL Register (361-B8A). Thus the Processor can be cycled on the same STL. For Console display of the Selector Status

Levels the SM-OP signal on the priming gate (361-A8A) indicates that the Processor must be in Selector mode to display its SSTL Register. The SELD1 to SELD5 signals feed the display lights. The first STL of Selector Servicing can be any one of five, 4DS1, 2, 3, 5ZS1 or 2. Selection is a function of the following conditions:

1. Read/Write
2. Less than 4 Condition
3. Forward/Reverse
4. SCAD setting.

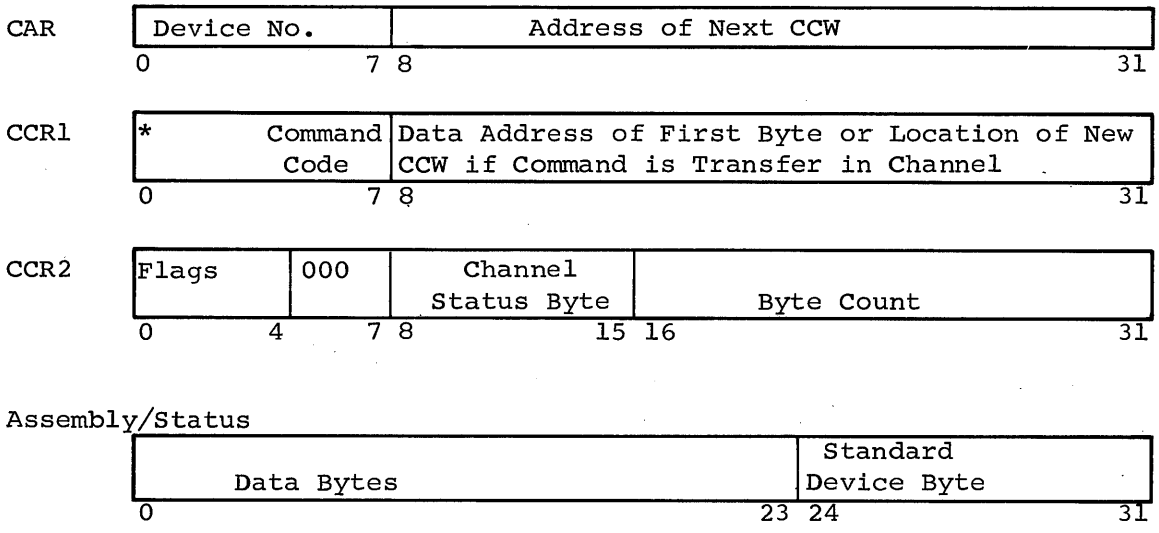
Since this selection must be done fast, the Selector PSTL Register is directly set by the SRSTLXX signals (364-B2D, etc.). This logic samples the above mentioned conditions whenever an SSP-AN is developed as explained under Selector Scanner and Control.

The Selector Status Levels, their Maintenance Panel indications and a brief functional description is shown in Table 4-5.

4.3.12 SELECTOR SCRATCH PAD REGISTERS

Each of the six Selector Channels has a group of four Scratch Pad words for use in Servicing and storing the Channel Status and Standard Device Bytes. These words are used to store the CAW, CCW1 and CCW2 words, and in the fourth location, to accumulate data, a byte at a time, during Selector Servicing cycles. In the Scratch Pad itself, these registers are referred to as the CAR, CCR1, CCR2 and the Assembly/Status register, respectively.

The contents of these four 32-bit registers is as follows:



* This is the Command Code unless data chaining was performed by the previous CCW, in which case these 8 bits will be ignored.

Table 4-5. Selector Status Levels

Type	PSTLR/STLR Bit Display 5	4	3	2	1	0	Standard Functions
3AS1	1	0	0	0	0	0	Move CCR1 from Memory to Scratch Pad
4AS1	1	1	1	0	0	0	Main Memory Write (DOUT ACTIVATE)
4AS2	1	1	1	0	0	1	Transfer in Channel (1st Status Level)
4AS3	1	1	1	0	1	0	Store Status
4AS4	1	1	1	0	1	1	CAR + 4 (1st Status Level)
4AS5	1	1	1	1	0	0	CAR + 4 (2nd Status Level)
4AS6	1	1	1	1	0	1	Move CCR2 from Memory to Scratch Pad
4BS1	0	1	1	1	0	0	Main Memory read
4DS1	0	1	0	0	0	0	CCR1 minus 1 (update byte count)
4DS2	0	1	0	0	0	1	CCR1 minus 1 (update byte count)
4DS3	0	1	0	0	1	0	CCR1 minus 1 (update byte count)
4DS4	0	1	0	0	1	1	CCR1 minus 1 (update byte count)
5AS5	0	0	0	1	0	0	Transfer in Channel (2nd Status Level)
5BS1	0	0	1	0	0	0	Read: DIN to Memory Reg. if less than 4
5BS2	0	0	1	0	0	1	Write: Memory Reg. to DOUT if less than 4
5BS3	0	0	1	0	1	0	Send Command to IOU. (2nd Status Level of terminate)
5ZS1	1	1	0	0	0	0	Main Memory Addressing
5ZS2	1	1	0	0	0	1	Main Memory Addressing
5ZS3	1	1	0	0	1	0	Main Memory Addressing
5ZS4	1	1	0	0	1	1	Main Memory Addressing
6AS1	0	0	1	1	0	0	Scratch Pad read
6AS2	0	0	1	1	0	1	Scratch Pad write
6AS3	0	0	1	1	1	0	Send Command to IOU (1st Status Level of terminate)
6AS4	0	0	1	1	1	1	DR to Main Memory (end of Main Memory read)

The Digi Switch/Strip Switch addressing for the six Selector Channels uses the same Strip Switch (3 least significant bits for the same particular register e.g. CCR1, CCR2, etc.) regardless of the Selector Channel number. They are as follows:

(x)2 = CAR	(x)4 = CCR1
(x)3 = CCR2	(x)5 = Assembly/Status

The (x) for the six selectors is as follows:

Sel. 1 = 3	Sel. 4 = A
Sel. 2 = 6	Sel. 5 = B
Sel. 3 = 7	Sel. 6 = F

This (x) represents the Digi Switch setting which supplies the 4 most significant bits of the SP Address.

The Selector Scratch Pad registers are set up during Initiation and are continually updated during Servicing of that Selector. In regular servicing, the CCR1, CCR2 and Assembly/Status words are updated for each byte serviced. In Chain Data and Chain Command, the CAR word is also updated. In the regular case, the CCR1 word has its address incremented (forward) or decremented (reverse) by four bytes during the Main Memory cycle handling of a full word (4DS1, 5ZS1 and 4BS1/4AS1 STLs). In the LT4 (less than 4) Cycle (4DS3, 5ZS2 and 5BS1/5BS2) this address is incremented or decremented by one byte. The CCR2 word has its count decremented by one byte regardless of the type servicing cycle (SP, MM or LT4). During Command or Data Chaining, the CAR word is incremented by 2 full words (or 4 full words in one case to be covered later) during the obtaining of the new CCW1 and 2 words.

The SLSPA logic designates (drawing 379) which of the four Scratch Pad locations is to be selected. The SSPA(2,1 & 0)-P lines are connected to the FM address Decoder (drawing 302). The SSPA0-P develops FMAD0-N (302-A3A), the SSPA1 develops FMAD1-N (302-A5A) and SSPA2 develops FMAD2-N (302-A7A). These three signals will supply the three least significant bits of the SP address.

The SPIT logic is developed as a function of which of the six Selector Channels is being serviced by the S(x) SEL-AP lines. The SPIT(0,1 & 2)-N lines also go to the FMAD decoder (drawing 302) where the 0 goes to develop FMAD3-N, the 1 for FMAD5-N and the 2 for FMAD6-N. All of these are gated against SPAG4-P (302-D3A) which is formed by the PSM-AAP level which is present when the Processor is in Selector Mode. The SPAG4-P level develops FMAD4-N (302-C4B) all the time in Selector mode, the reason is that this bit is used in all six Selectors in the high order four bits (most significant) required for the address.

4.3.13 SELECTOR GENERATED BPU COMMANDS

The Selector generated BPU Commands can be grouped into four types of Commands: Main Memory, Scratch Pad, Adder Commands and Bus Commands.

1. Main Memory Commands

REG (366-B8A, B7A) - Regenerates the MR (Memory Register) contents back into MM.
SMR (366-A7B, A6A) - Sets bits into MR from the bus.

2. Scratch Pad Commands

RGXW (366-B6A, etc.) - Regenerates the DR word into the SP.
GEPA (366-D5C) - Generates Parity during the RGXW time.
FMRD (366-D5B) - Read Command to the SP.
IS (366-D1A) - Inhibits Strobe during FMRD Command.
IORGQ (366-D4D) - Allows regeneration of C0 byte from DR and C1, C2, and C3 bytes from the output of the Adder (Sum Bus).
SIORGH (366-D4C) - Same as IORGQ except DR C0 and C1 and Adder C2 and C3 bytes.
SIRDR27 (366-D2A) - Inhibits the regeneration of DR27 bit. This is to prevent the storing of the PCI Flag bit in SP since its function has already been performed and the bit must now be eliminated.

3. Adder Commands

TTXW (366-A5A) - Permits transferring of the true DR word through the Adder unaltered.
TTXK (366-A6B) - Permits transferring of one particular byte from DR through the Adder. This byte is specified by the IOCAD (SCAD) setting.
BAX1 (366-D8A) - Binary Adds count of one to DR word.
BAX4 (366-D7A) - Binary Adds count of four to DR word.
BSX1 (366-D6A, D6B) - Binary Subtract count of one from DR word.
BSX4 (366-D5A) - Binary Subtract count of four from DR word.

4. Bus Commands

RODRW (366-B3A, etc.) - Reads out to bus the DR outputs.
RODIN (366-B5A, B5B) - Reads out to Bus the IOUDIN lines.
RODRP (366-B5C, B4A) - Reads out to Bus the three bytes in DR not specified by the CSC(X) logic.
ROMRWA (& WB) (366-B2A, B2B) - Two Commands which read out the MR outputs onto the bus.

The other command which does not fall in the above mentioned categories is:

RRUN (366-A7A) - Resets the RUN flip-flop in the BPU.

4.3.14 SELECTOR INTERFACE CONTROLS

Selector Interface Controls consist of six flip-flops which control the sending of the various Selector Interface signals to the Control Electronics (CE).

1. SACT (Selector Activate) (377-B7A) is set by the first STL of servicing 4DS1, 2, 3, 5ZS1 or 2). This indicates to the CE that the SR has been accepted and can now be dropped.

2. SSEL (Selector Select) (377-C2A) is set only during Initiation when the device address is broadcast to all CE's on the selected channel.

3. STRAC (Selector TRAC) (377-C4A) is set (Servicing) in 6AS3 STL to indicate that a Command is being STROBED on the DOUT lines. All other Interface Control lines must be 0 except STROBE which must be 1.

4. STERM (Selector TERMINATE) (378-B2A) is set (Servicing) by any of the following three occurrences:

   a. Count has reached 0 and Chain Data is not called for.

   b. A STERANY type error has occurred.

   c. A HALT instruction was issued.

   When the TERMINATE Interface Line is raised, it signals the CE that the last data byte has just been transferred to or from the device. The CE responds by raising the END Interface line with its next SR. STROBE must be present and ACTIVATE must have been previously received.

5. SSETI (Selector Set Interrupt) (378-D5A) indicates that a PCI Flag bit has been recognized in a CCW2 word. This flip-flop will be set by the first Servicing STL containing STROBE following Storing (for the first time) into Scratch Pad CCR2 location the above mentioned CCW2 word. PCI is used by the programmer to indicate when a particular set of CCW words have been reached during processing. This line is sent out with STROBE: ACTIVATE has previously been received. The CE responds by raising the INTERRUPT line.

6. SSTR (STROBE) (378-C7C) - in servicing, is set to allow the CE to change its internal state. In Read, this indicates that the byte on DIN has been accepted by the Processor and can be removed by the CE.

   In Write, STROBE indicates that the information on the DOUT lines is firm and can be accepted by the CE. This is true for both a Data or Command byte. The STROBE flip-flop is usually set at C5 time and reset by the following C2/C4/C5 time. This results in a 300ns pulse (nominal) going across the Interface.

4.3.14.1 DIN-DOUT Controls, Receivers and Transmitters

When information is to be received from an I/O device (either data, sense or SDB), the particular trunk on the servicing Selector on which this device is operating has its DIN lines opened, exclusively. This is done by SPDIN (381-C7B) in any one of four conditional status levels. Since in the selectors, the DIN information is placed in the SDOUT register until it is

used, the SPDIN-AP is one of the conditions for generating the 60ns RSDOUT-P (381-D4C) signal.

The SPDIN signal is gated with the Selector scanner output on 381/1017 to form the GSXDIN-N signals (381-C7C, C6D and 1017-B7A, etc.). These prime the gates for the four trunks on the selected channel. The servicing trunk will have its SXTXRDY flip-flop set so that the PSXTXDIN-P signal goes to the interfaces. The outputs of the nine DIN receivers are ORed together on a bit basis in groups of two Selectors, i.e. 12DINXX-P, 34DINXX-P and 56DINXX-P on 367, (see drawings 1000 and 1011). These signals go directly to set the SDOUT register after being ORed together (see drawing 367) with the SSDOUTXX-P signal.

The SDOUT data is placed on IOUDINXX (drawing 341) by gating out the register with a ROSDOUT-SN (381-C5B, C5A) command. This occurs in any STL where either data or the SDB are required for storage or status decoding. The outputs of the gates are the SDOUTXX-P signals which feed directly into the IOUDINXX OR gates.

The SDOUT register (drawing 367) is used also for the DOUT information transmitted from the Selector Channels to the Control Electronics (Devices) during Write Commands. The data is placed into DR from the Scratch Pad or Main Memory depending whether a SP or MM cycle write is in progress. From here it is transferred to the SDOUT Register. The SDOUT drives the SDOUT transmitters which sends the byte over the Interface DOUT lines.

4.3.14.2 END Receivers

When an END signal is sent by a CE, this signal is received by a Receiver for the particular trunk involved. The output of this Receiver is gated against a S(X)T(X) DIP line which is an Interface line (see 376-B8A, etc.). This DIP (Device Power) line when true indicates that power is on in a CE unit and that signals on CE to BPU lines are valid. The output of this Receiver gate is conditioned by a S(X)T(X)RDY-IN line so that the resulting output of S(X)T(X)ENDG-P signal reflects an END condition on the Selector and Trunk currently being serviced. Selectors 1/2, Trunks 1, 2, 3 or 4 are shown on drawing 376. All of these signals are ORed together to form the 12 END-N & P signals (376-A6A). These in turn are ORed with 34 END-P and 56 END-P. These are formed in a similar manner (for Selectors 3, 4, 5, and 6) on drawing 3661008. The resulting outputs (376-A6B) of END-SN and END-SP are used as follows:

1. The END-SN gates the setting of the END at 367-B2C. The outputs of this flip-flop are used to condition gates required for status level selection. The END flip-flop holds the END condition of the exiting Selector Channel until C1 time of the first STL of the newly arriving Selector Channel.

2. The END-SP line is used on 378-D7B to condition the setting of SSTR (378-C7C) (STROBE) during 5ZS1 and 5ZS2 STLs. Setting SSTR is through MMADRCXW-N (378-C7D) which permits exit to Normal thus being the last STL of Servicing.

3. The END-lN (flip-flop output) develops END-SAP at 364-A5B and this in turn is sent to the Mux at 353-A2A where it is ORed with the Mux signal, END-P.

4. The resulting output of ENDA-N is used at 355-B7B to develop the MRE-N signal when doing a LOAD.

5. END-IN also goes to the Console to light the SEND light.

4.3.15 SELECTOR DATA BUS

The BPU communicates with the I/O by way of 32 inverters which connect the BPU IBUS to the IOUB. The 00-08 inverters are shown on drawing 335; the 09-31 inverters are shown on drawing 344.

Another set of inverters connects the IOUB00-IOUB31 to a Selector IOUB00-A -- IOUB31-A (see drawing 373). Only 00-03 and 24-31 are used to load or sample certain Selector registers.

The 70/55 IOU Block Diagram, Figure 4-13, includes the various busses and registers. Their approximate relationships are also indicated.

Figures 4-19 and 4-20 show the logic paths of the data during read and write, respectively.

4.3.15.1 Parity Checker/Generator

The Selectors and the Multiplexor use the same Parity Checker/Generator. Inputs to the parity checker are gated from the IOUB01-IOUB08 inverters. The gating signal is OIOPC (Open I/O Parity Checker, 335-D8B). During Selector servicing, this signal is generated by INHIOUB (374-B3A) which in turn is generated by either 6AS1, 4BS or 5BS1 status levels. If an error occurs, the SDATACK flip-flop (343-B5C) will be set instead of the MDATACK flip-flop which can be set during Multiplexor servicing.

More Parity Checker/Generator information can be found in paragraph 4.3.7.1.

4.3.16 SELECTOR REGISTERS

4.3.16.1 Command Registers

Each Selector Channel has a three flip-flop Command register. Selectors 1 and 2 Command registers are shown on drawing 372. Command registers for all other Selectors are on drawing 1004. The four least significant bits of the command byte are decoded into SXREAD, SXSENSE and SXREV (X represents the Selector Channel) during Initiation or Command Chaining and remain in the register as the command to be executed until changed by the next Initiation or Command Chaining.

All commands other than Read, Read Reverse or Sense look functionally the same to the Selectors and are treated as such with the exception of Transfer In Channel which is decoded in a common ST/C flip-flop (372-B2C).

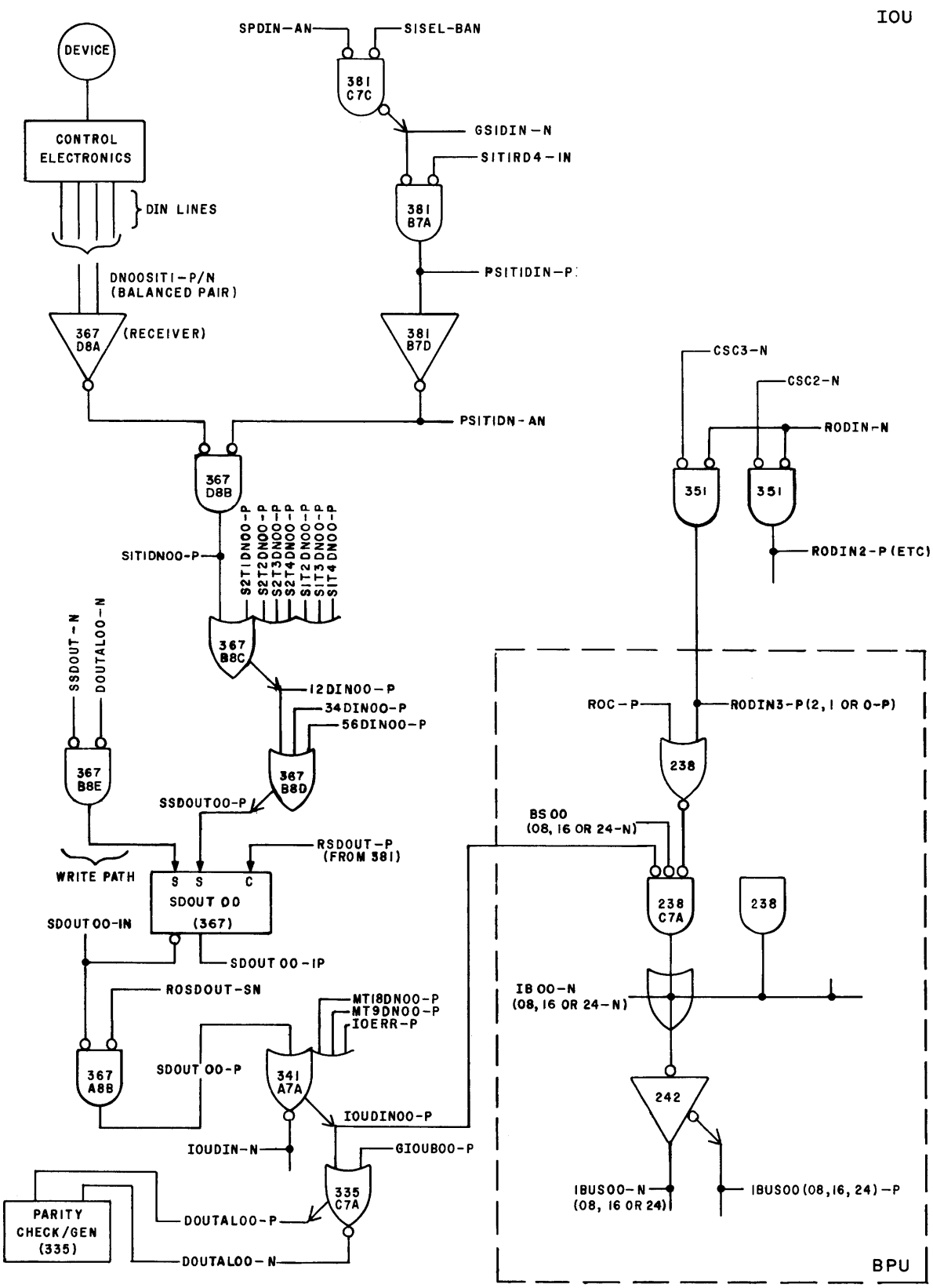


Figure 4-19. Selector Read Data Flow

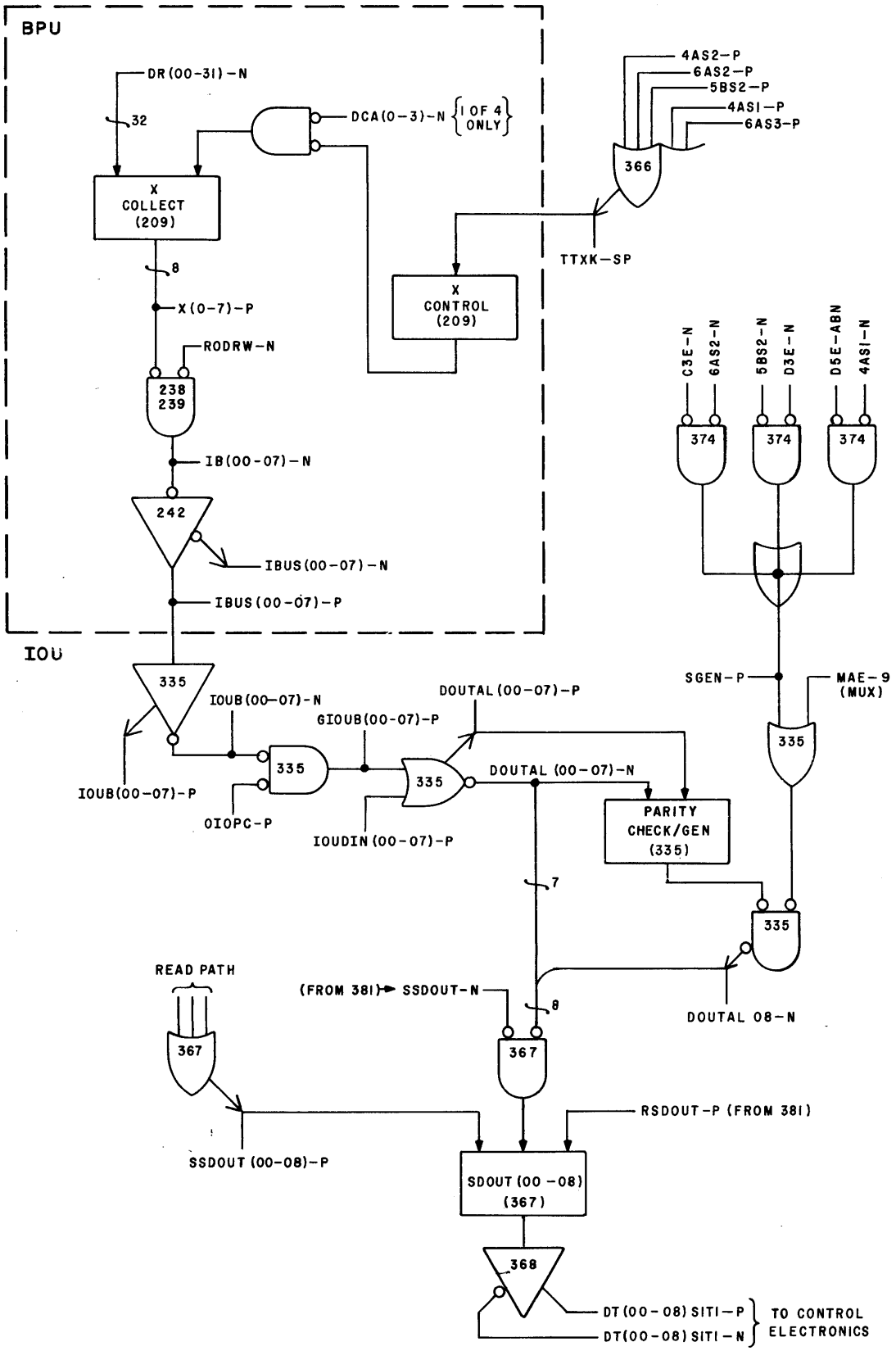


Figure 4-20. Selector Write Data Flow

The registers are reset at DIM time of 3AS1 STL if SCC(1) as a function of SXSEL by the RSCR-N (Reset Selector Command Register) Command (372-C3A). The setting of the registers is accomplished at D1 time of 3AS1 STL under the same conditions as the reset. The set command SSCR-N is generated at 372-D3B.

The ST/C flip-flop is set at D1L time of 3AS1 STL unlike the Command registers and is reset at C5 time of the 5AS STL which is the second T/C STL. The ST/C flip-flop is used to control the selection of the 4AS2 STL, the first T/C status level.

The outputs of the six channel command registers go to gates on 372 where they are gated with SXSEL. This generates the SREAD, SSENSE and SREV levels which are used to control the servicing for the particular channel selected.

4.3.16.2 KEY Register

The Key registers for the Selector Channels consist of four flip-flops per channel which are set during initiation with a reset-read-in from IOUB28-31 (refer to drawings 369 and 1003). The SSKR-AN command (369-D2A) sets the Channel Key register as a function of the Channel being initiated. The reset for the same register is generated by using the first 60ns of the SSKR to create the RSKR-N pulse (369-C2B).

The outputs of the six Channel Key registers are gated with SXSEL signals. This generates the SKEY (0-3)-P levels (369-A7A, A6A, A4A, A2A) which are ORed with the gated output of the MUX key register to be used for a zero check if the Memory Protect option is not installed or be used for Memory Protect check.

4.3.16.3 FLAG Registers

The Flag Bit Registers for the Selector Channels consists of a three bit register for each channel. The Flags SXCDF, SXPCIF and SXSKF are required for normal servicing control. A two bit common register for SSLIF and SCCF which are only needed during Command chaining operations. The significance of the flag bits is as follows:

1. 2^{31} - CD (Chain Data), allows using different sections of Main Memory in the same operation.

2. 2^{30} - CC (Chain Command), when set, indicates that at least one more I/O command is to follow.

3. 2^{29} - SLI (Suppress Length Indicator), if set, will not permit an indication of incorrect length upon termination.

4. 2^{28} - SK (Skip), inhibits the transfer of data to Main Memory. This flag can be used only with Read, Read Reverse or Sense commands.

5. 2^{27} - PCI (Program Controlled Interrupt), causes a channel interrupt to occur when servicing the first byte after having fetched the CCW2 word from Main Memory. This flag is used by programmers so that he will know when a particular device is serviced.

The registers have a reset-read-in of which the first 60ns of the set command is the reset by RSFBR (371-C3B). The read-in uses the SSFBR command (371-D3C) which is generated during initiation, 4AS6 (Fetch T STL) and 4DS4 (End Status Decode STL).

The set and reset pulses of the Channel Flag registers are gated against the channel being serviced. The SXPCIF must have special resets, RSPCIF (371-B2D), which are gated to insure that the reset is to the proper channel (see 371-D5C, C5E).

The outputs of the six channel flag bit registers are gated with SXSEL. This generates the SCDF (371-A7A), SPCIF (371-A5A), SSKF (371-A4A) signals which are used to control the servicing for the particular channel selected.

4.3.16.4 Selector CAD, Busy and Halt Registers

The two bit CAD registers (Character Address) for each channel is used to specify which byte of a word is being transferred to or from Scratch Pad or Main Memory so that this byte can be selected from or merged with the remaining three bytes.

The CAD register is set from IOUB00-01 either during initiation or at D1 time of 3AS1 (Chaining Fetch A STL) with the SSCAD command (370-D5D). The first 60ns of this command is formed into a reset, RSCAD (370-C5A). These two commands are gated against the selector being serviced to allow the proper Channel register to be selected.

The outputs of the six S(X)CAD registers are gated with SXSEL. This generates SCAD00-SN (370-A7A) and SCAD01-SN (370-A6A). At DD6 time of the status levels where the SCAD is used (see 370-A3A, A3B), the SCADXX-SN is set into the SCAD200/201 flip-flops (374-C7A/B) where the gated output is used for byte selection as SCAD00/01-P. The SCAD200/201 flip-flops are reset at each C6 time in every STL in selector mode. Therefore the CAD setting for a given selector is not displayed on the maintenance console.

The SCAD00/01 flip-flops cannot be used directly because when the CAD settings are needed, these flip-flops are being triggered up or down one. Triggering is controlled by TUSCAD (382-A4B) and TDSCAD (382-B3A) which are gated with the channel select (370-D5B, D4C) to form trigger up command (TUSXCAD) and trigger down command (TDSXCAD).

The BUSY flip-flops for each channel (see drawing 370 and 1005) are used to indicate to any I/O Instruction that the Channel is presently executing an operation. The HALT flip-flops tell the device to halt operation as a result of a Halt Device Instruction. These are shown on drawings 370 and 1005. Both are set in Processor Normal Mode Status levels as a function of the Channel being serviced. The BUSY flip-flop is reset at the end of the termination interrupt routine for that channel.

The outputs of the six channel BUSY flip-flops are gated with SXSEL to generate SBUSY-P (370-B4A, etc). This signal in turn generates BUSY (332-B4B) which sets a Condition Code (355-C5B). The HALT flip-flop outputs are gated with the Channel Select to generate SHALT (370-A2A). These are used to control whether to send out a TERM level during the next service request on the selected channel.

4.3.16.5 Selector Channel Status Register, STERANY & STCSR

The Selector Channel Status Register (SCSR) consists of seven flip-flops (drawing 343) which store various error, terminating and program controlled conditions. The individual flip-flops are set independently by several different STLs during Servicing depending on the conditions which are being checked. There is one common time when all will have a gating pulse attempting to set them. This occurs in any of the T-1 STLs, e.g. 4DS1, 4DS2, or 4DS3. During these STLs, the CCR2 Scratch Pad location for the particular Selector Channel being serviced is read out to the bus. The stored Channel Status bits contained in byte C1 of this word are read into the SCSR Register by the IOSSCSR-P Command (343-C7C) which gates these bits from IOUB (17 --- 23). If any additional bits are added during Servicing they will be superimposed and the entire group stored back in the CCR2 location at the completion of each byte of Servicing. This is accomplished by performing an extra STL called Store Status STL, 4AS3.

The meaning of each flip-flop in the SCSR follows:

1. SEND (343-B7C) is set whenever a Set Interrupt Command is to be sent to a device. It indicates that the Interrupt to be taken is a termination interrupt.

2. SPCI (343-B6B) is set whenever the PCI Flag bit (2^{27}) is contained in the CCW2 word being fetched from Main Memory. SPCI can also be set whenever a Set Interrupt, SSSETI (380-B3A) could occur depending on END(0). The SSPCI-P Command (374-A2A/B2E) is generated by these two conditions.

3. SDATACK (343-B5C) is set by either of three conditions:

   a. If an IOPE occurs on any of the three STLs (4BS1, 5BS1 or 6AS1) that read data (not SENSE) from the DIN lines.

   b. If an MMPE occurs in any of the STLs that read data from Main Memory (5BS1, 5BS2 or 4AS1).

   c. If a SPME occurs in any of the STLs that read data (SP Assembly Word) from Scratch Pad (4BS1, 3ES1, 6AS1 or 6AS2).

4. SINCLTH (343-B5D), during END Servicing a check is made in the 4DS4 STL for a count other than zero in CCR2 word or the CD Flag Bit present. If there is a count or CD, SINCLTH flip-flop will be set if the SLI Flag bit is not present and the operation is not a LOAD.

5. SPROTCK (343-B4B) will be set during the Main Memory Addressing STLs (5ZS1 and 5ZS2) in Read if the Key bits disagree with those previously set up in memory or if an address exception occurs (if the Memory Protect feature is installed). If the Keys associated with the current processor state and those related to Main Memory block are equal or either is zero, the Main Memory block accepts a data store.

6. SCONTCK (343-B3B) if either a SPME (Scratch Pad Memory Error) or a MMPE (Main Memory Parity Error) occurs in any non-data operation this FF will be set. This includes count decrementing, fetching and Command Chaining.

7. SPROGCK (343-B2C) is set in the 5ZS1, 2, 3 or 4 STLs if the memory is addressed beyond its maximum location. Also set in 5AS5 STL (Transfer in Channel STL #2) if the address of the CCR1 word containing the Transfer in Channel command contains any bits in 2^0, 2^1 or 2^2 which indicates that this is not a double word address specifying the next CCW1 word location.

STERANY (Selector Terminate Any) (344-C5A) is developed if any of the following conditions exist:

SPROTCK, SPROGCK, SCONTCK, SDATACK if WRITE or END, and END with SINCLTH. When STERANY is generated, it signifies that an error has occurred of the type that makes it necessary to stop the operation since the results will not be valid. That is effected in the following ways:

1. In 4DS1, 4DS2, 4DS3, 5ZS1 and 5ZS2 STLs, TERMINATE will be Strobed out if STERANY and END(0).

2. In 6AS2 STERANY unconditionally will set TERMINATE.

3. In the Command Chaining path, SET INTERRUPT Code will be Strobed out in 6AS3 STL if SSE(0).

The STCSR flip-flop (344-C5C) can be set by any of the conditions which set any of the SCSR Register flip-flops. (For ex. SSPRGCK-P, SSCONCK-P, etc.). This will cause a storing of the SCSR Register which is also used in Normal I/O execution as well as in Selector Servicing.

4.3.16.6 Selector Control Flip-Flops & Termination Status Decode

The SCC, SSE, SSI & SSM flip-flops are set during END Servicing when the SDB (Standard Device Byte) is decoded. If Command Chaining is called for, the SCC flip-flop will be set. SSE is set for a Switch End condition, SSI for a Set Interrupt condition and SSM if the Status Modifier bit (2^0) is contained in the SDB. On drawing 355, the DIN lines are decoded. The decoded outputs are used as follows: MSE sets SSE, MSI sets SSI and SCC sets SCC. The SSM flip-flop setting conditions are decoded on its read in gates on drawing 374. This is only set if Command Chaining is to take place and the 2^0 bit is set in the SDB.

A brief explanation of the meanings and reasons for these four conditions is as follows:

1. SCC (374-C4B); Command Chaining will be permitted only if all of the following conditions are fulfilled:

   a. CC and $\overline{CD}$ flag bits

   b. $\overline{Load}$ and

c. Device End condition is reached which is 2^3 bit on the SDB and not 2^1 or 2^2 bits which are Device Inoperable and Secondary Indicator bits, respectively.

2. SSM (374-D3D); if all the above conditions are met and the SDB contains 2^0 bit (Status Modifier) the new CCW words will be taken from a location whose address is two words higher in Main Memory than the one which is in the CAR at the beginning of the Chaining operation.

3. SSE (374-C5B); if the SDB contains 2^5 bits and $\overline{2^1}$ and $\overline{2^3}$ and $\overline{\text{LOAD}}$ the device is busy and the MSE condition is recognized. This signals the CE to do a Switch End which means to drop the END line and bring it up again later with another SR when the Device End condition has been reached.

4. SSI (374-C4A); this is developed by various combinations of bits on the SDB along with a CCF or $\overline{\text{CCF}}$ condition. These conditions are decoded on drawing 355. This MSI condition, when later Strobed out in 6AS3 STL signals the CE to raise its INTERRUPT line because the current operation has been completely finished.

5. SZ (374-D2E) is the Selector Zero flip-flop which is normally set in any of the T-1 STLs (4DS1, 2 or 3) if the byte count has gone to zero. SZ is also set during END Servicing of a LOAD function if the SDB has the 2^2 bit (Secondary Indicator). The reason is that the SZ flip-flop is used in 5BS3 STL to cause the setting of IOPE and the resetting of RUN and LOAD flip-flops when doing a LOAD since the entire LOAD is considered bad if a Secondary Indicator occurs. See gate B4E on drawing 374 which is the source of SIOPE-SN which uses SLOADSTP-N as a condition. SLOADSTP-N signal is generated by SZ-1P (see 374-B5A).

4.3.16.7 Selector LT4 and Miscellaneous Control

Each Selector Channel has a LT4 (Less Than 4) flip-flop. When set, it indicates that an initial data move will not be to or from an even word address or will be less than four bytes long. In Forward, the first byte will not be C0 and in Reverse the first byte will not be C3. The gated outputs of all the Selector LT4 flip-flops are ORed to form the LT4-N/P levels (380-B5D). Since they are gated against the S(X)SEL-N signals, the LT4-N/P will reflect the condition of only the Selector being serviced. These signals are used to condition the entrance STLs selection (see 364-A4D, B3A, etc.).

The FETCH flip-flop (380-C7C) is set whenever the count has reached zero and the Chain Data Flag bit is present. It is used to control STL Selection of the Fetch Main Memory Addressing STL (5ZS3) when the time comes to obtain new CCW words from Main Memory for the Chain Data continuation. FETCH set in the 4DS1 and 4DS3 (T-1) STLs at the time the count is actually going to zero (if CD). In the 5BS1 and 6AS2 STLs FETCH is set (if CD) as a result of the SZ flip-flop having been set in a previous STL when the count was being decremented to zero. The reason for the last two cases is that these are the STLs that would exit to Normal and not the STLs which actually decremented the count to zero.

The SSSETI-P Command (380-A8A) will set the SELECTOR SET INTERRUPT flip-flop (378-D5A). SSSETI is generated by the first servicing STL containing Strobe (with one exception) that occurs after the CCW2 word containing the PCI Flag bits has been fetched from Main Memory. The one exception is the 4DS2 STL (which also generates the RSPCICON-N gating signal) which does not contain Strobe. However, the next STL (Read) is 6AS1 which has Strobe. The RSETI-P signal (380-A7A) resets the SET INTERRUPT flip-flop. RSETI is formed earlier in all the STLs containing Strobe except 6AS1 for which it is done in 4DS2.

SSTRSTL-N/P (380-A4A) is formed by all the STLs containing Strobe except as explained in the previous paragraph.

SA/T flip-flop (380-D3C) refers to an old designation of CCW1 word being called the A word and CCW2 the T word. SA/T is set in the 5ZS3 if 2^2 bit is present in the Main Memory Addressing bits. Since all CCW1 words must be located in a double word address, the CCW2 word will be a single word address in which 2^2 bit is present (2^0 2^1). The 5ZS3 STL is used to address both the CCW1 and 2 words in successive passes through this STL and the condition of the SA/T flip-flop determines whether to select the Fetch A (3AS1) or Fetch T (4AS6) STL.

SSTER-P (380-B2D) is used to set the SELECTOR TERM flip-flop (378-B2A). SSTER is developed by three conditions:

1. Count goes to zero and $\overline{CD}$

2. HALT Instruction is initiated

3. A STERANY type error occurs when $\overline{END}$.

This Command is formed in the STLs containing Strobe with the same exception of 4DS2 and 6AS1 mentioned previously.

The S12P-P signal (382-A6B) is used during Initiation to signal that the system has Selectors 1/2. The S(X)SCANGND signals develop the same information relating to Selectors 3, 4, 5 and 6 on drawing 3661014.

TUSCAD-N and TDSCAD-N (382-A4B, B3A) are used in servicing to trigger up and down respectively the Selector CAD register by a count of one. TUSCAD and TDSCAD are gated against the S(X)SEL-N (see 370-D5A, D5B, D4B, D4C) signal for the Selector being serviced in order to develop the TU/D(S)(X)CAD-P/N for the specific CAD register to be triggered up or down. The triggering is always up during Write and the Read Forward. Triggering is down during Read Reverse only.

The IOCOMP-SP (383-B3B) is formed in 5BS3 STL if the SEND flip-flop is set. This signal indicates that Set Interrupt code was sent to the device or that a STERANY with SSE(0) error occurred. If the QSTCSR flip-flop was set thus requiring a Store Status before completion, then the IOCOMP-SP is inhibited in the 5BS3 STL and sent out instead in the 4AS3 Store Status STL.

This signal (IOCOMP-SP) is ORed with IOCOMP-MP from the MUX to form IOCOMP-N (289-C8B). This allows the resetting of the ISIM flip-flop (289-B7A) thus signifying that the I/O Instruction is completely finished and now

the Processor can return to Normal operation. This will only have significance if the machine had been operating with the ISIM button ON or in the ISIM mode. The ISIM switch causes the setting of the ISIM flip-flop each time the Initiation of a START DEVICE or LOAD Instruction was completed with a condition code equal to zero.

4.3.17 LOAD FUNCTION

In order to store the Program into Main Memory, the LOAD function is normally used. This is accomplished by setting up the Channel and Device number using the DIGI switches on the Operators' Console, and after hitting GENRES, push the LOAD button. Functionally the following things happen:

1. Processor initiates a READ Command
2. The address is set to 0
3. The CCR2 word count is set to maximum (all 0).
4. These CCR1 and 2 words are stored in the scratch pad locations for the particular Selector.
5. The Device is started.

Logically, the LOAD button sets the LOAD flip-flop (352-C2A). During Initiation the LIP (Load In Process) flip-flop (352-B4D) gets set. The LIP-1P signal inhibits the setting of PNM (289-D3B) until the Load is complete. LIP is reset during the last STL of END Servicing if a SET INTERRUPT (SSI) condition was recognized. The LOAD flip-flop is reset in the Selector by RSLOAD-P (374-B5C). This gate will reset LOAD if an error occurred during the Servicing of a LOAD function. On gate D2C, the RNLOAD-P (326-D2B, etc.) signal is used to reset the LOAD under these two conditions:

1. LOAD was completed and the next instruction staticized will generate HKRE which in turn generates the RNLOAD signal.
2. An error or incorrect Condition Code was detected during the Initiation of a LOAD or START DEVICE Instruction. This also develops RNLOAD.

When SRs arrive, they are handled the same as in non-Load operations as explained in the following section of this write-up. The Device will continue until a gap is reached in the case of Tape Stations, Drum, Disc, etc. or until one card has been read in the case of the Card Reader. At this point, the END line is raised by the CE along with SR. Since the maximum count of all 0 was set in the CCR2 word, there will be a residual count remaining when END is raised. In order to prevent getting an Incorrect Length Indication (setting SINCLTH flip-flop), the gating of the setting of SINCLTH (343-B5D) is conditioned by LOAD-EP (see 374-A5A). If any errors occur during the Load Function, the 2^2 bit (Secondary Indicator) will be contained in the SDB sampled during END Servicing and this along with the signal MRE-N will set the SZ flip-flop (374-D2E). The MRE (355-A7A) signal is developed because the END condition was received during a LOAD.

4.3.18 SELECTOR CHANNEL SERVICING (Refer to 70/55 Selector Channel Servicing Status Level Flow)

Before servicing can commence, the Device must be initiated and, in some cases, started moving. During Initiation of a START DEVICE or LOAD. instruction the following events take place in the registers, both Scratch Pad and hardware, of the associated Selector Channel: HW = Hardware; SP = Scratch Pad.

1. Command Register (HW) set with Command Code from CCW1.

2. Flag Register (HW) set with Flag Bits in CCW2.

3. SCAD Register (HW) set from least two significant bits of the data address portion of the CCW1 word.

4. Key Register (HW) set from the CAW word Key bits.

5. The count in the CCW2 word and the Data Address of the CCW1 word are examined to determine if a less than 4 condition exists. * If it does, the LT4 flip-flop of the Selector being initiated, is set.

* Count is less than 4 or first data byte address is not a boundary location.

6. The CAW word has its C0 character stripped of the Keys and replaced by the Device Number; this word is then stored in the CAR SP location.

7. The CCW1 word is stored in the CCR1 SP location.

8. The CCW2 word is stored in the CCR2 SP location.

9. The Assembly/Status word is reset in SP and the SDB is stored in C3 Character location. This SDB was returned by the CE as a result of sending the Device Number and, after receiving the READY return, sending the Command without Strobe.

10. Finally, the Command Code is sent to the Device with the Strobe and this starts the Device (if required).

Now the I/O logic awaits the arrival of a Service Request (SR) from the Device in order to begin the servicing flow. Functionally, the order of events with the arrival of a SR on a Selector Channel is as follows:

1. The SR is stored in the S(X)ULSC flip-flop (drawing 360) associated with the Selector Channel making the SR.

2. If more than one SR has arrived, the Selector Channel with the highest priority (priority is 1 -- 6 with 1 the highest) will be serviced first. This is accomplished by the higher priority S(X)ULSC (360-C6B, C6F, etc.) output inhibiting all those lower as explained under Scanner and Control (4.3.10).

3. Based upon the Command, SCAD, Forward/Reverse condition, and LT4 condition, the first STL of servicing is selected. These conditions were set in the hardware registers and flip-flops (associated with the particular Selector) during Initiation as explained earlier in this section.

4. The first STL of Selector servicing for the first SR will be one of four; every subsequent SR handled will be one of five possible entrance STLs. They are 4DS1, 2, 3, 5ZS1 or 2. The 4DS1 STL is the one exception that cannot be selected by the very first Service Request of an I/O Instruction. The 4DS2 STL is for the SP cycle; 4DS1 for the Main Memory Read; 4DS3 for LT4 Read Case; 5ZS1 for the Main Memory Write and 5ZS2 for the LT4 Write.

5. Upon entering the Servicing flow, the ACTIVATE signal is sent to the CE to suppress the SR.

6. The three ways of handling Selector Channel SRs are:

   a. In READ (4DS2 & 6AS1 STLs), the count is subtracted by one and the byte arriving from the device is inserted into the SP Assembly/Status Register word in the character location specified by the SCAD register setting. In the WRITE (4DS2 and 6AS2 STLs) the count is subtracted by one and the byte in the character location specified by SCAD 00-01 is sent to the device. In READ, there are normally three SP cycles before this data is sent to Main Memory. In WRITE there are always three SP cycles before a new word or byte (LT4 case) is obtained from Main Memory.

   b. A Main Memory cycle occurs when the right or left boundary character location is reached when processing a full word of data. In the Read Forward and Write cases it is the right boundary and the left boundary for the Read Reverse case. In the READ case the count is incremented by one if forward and decremented by one if reverse. The address is incremented by four if forward and if reverse, decremented by four. Then the byte arriving from the device is merged in the bus with the three bytes previously stored in SP, and the full word is sent to Main Memory.

      For the Write case, the count is decremented by one and the address incremented by four. Then a full word of data is brought from Main Memory and stored in the SP Assembly word. At the same time, the C0 byte is sent over the bus to the SDOUT Register and then out to the device.

   c. Less Than 4 occurs when processing an I/O Instruction whose total initial count is less than 4 or the initial data byte address is not a word boundary location. By this it is meant that the C0 location is not being addressed for the Forward or Write cases or the C3 location for the READ Reverse case. For the READ the count is decremented by one and the address incremented or decremented by one depending on whether forward

or reverse. The byte arriving from the device is placed in the SDOUT register temporarily. Meanwhile the Main Memory word, into which this new byte is to be placed, is brought from Main Memory and placed into the DR. At this point the three characters, which are not to be changed are read out on to the bus and merged with the new byte also being read out from SDOUT. This is controlled by the SCAD setting. The word with its new byte is returned to its original location in Main Memory.

For the WRITE, the count is decremented by one and the address incremented by one. Then the data word is brought from Main Memory and placed in DR. From here the byte to be sent to the device is sent to the SDOUT Register (and out to the device) as a function of the SCAD setting. The complete data word is returned unchanged, at its original location in Main Memory.

During all of the above SR handling, the various STLs are checked for such things as the LT4 condition, SP, MM or I/O Parity Errors, Zero Count, any other errors which set SCSR Register etc. If any of these errors occur, the SCSR outputs must be placed in the Channel Status Byte Character location of the CCR2 SP word before the STL flow is allowed to return to Normal. This is accomplished by the 4AS3 (Store Status) STL.

4.3.18.1 Data Chaining

If the Chain Data Flag bit (CD) is present and the count goes to zero, then Data Chaining is to take place before returning to normal in certain cases. First, the cycles that exit directly to the Fetch STLs for the regular data servicing cases, are SP Write, MM Read, and the LT4 Read and Write. Functionally, what occurs when in the Data Chaining cycle is as follows:

1. CAR word is read out of SP and the address portion is sent to Main Memory to fetch the new CCW1 word (from storage in the CCR1 SP location). While the new CCW1 word is on the bus, the Command portion is checked for Transfer in Channel (T/C) Command. If T/C is indicated, then this word is also stored in the CAR SP location and the address portion is sent to Main Memory and another new CCW1 is obtained and stored in SP, again checking for a T/C Command. If $\overline{T/C}$, the now updated address of the CAR word is used to fetch the CCW2 word from the next full word in Main Memory, and the CAR word is incremented again by 4 bytes and returned to its SP location. In addition, the Device Number is preserved and inserted into C0 location of this new CAR word.

2. The LT4 flip-flop is reset (unconditionally) and the new CCW1 and 2 words are examined for LT4 Conditions and, if present in either one, the LT4 flip-flop is set.

3. The SCAD Register is set from the two least significant bits of the CCW1 word.

4. The Flag Bit Register is set from the C0 Character of the CCW2 word and if the PCI bit is present, the SPCIF flip-flop is set. The SPCIF Flag bit is inhibited from setting into SP in order to ensure that the SET INTERRUPT line is raised only once for each PCI Flag bit.

5. If during the course of all of the above any SCSR Register flip-flops are set, then the Store Status STL (4AS3) is selected to put these bits in the CCR2 word (CSB location). If no SCSR bits, then Normal is selected as is also the case after the 4AS3 STL for the other conditions of SCSR bits.

4.3.18.2 Command Chaining

When the END line is raised along with SR, the DIN lines are checked (SDB) along with the CC Flag bit, for Command Chaining conditions. If Command Chaining is to be performed, the following takes place:

1. Various conditions are examined such as SCAD, READ/WRITE, FWD/REV, LT4, etc. to determine if the fetching of the new CCW1 & 2 words can be done immediately or if other STLs must be performed first. There are two other possible cases that could occur.

   a. The SDB contained the Status Modified bit of 2^0 and this requires that the new CCW words are to be obtained from an address two words higher than presently indicated by the CAR word address. Thus, the CAR word is incremented by eight bytes (4AS4 and 4AS5 STLs) before the fetching is performed.

   b. The operation was a READ which was concluded by the CE raising the END line independently (such as entering a gap on tape while a count still remains in the CCR2 word). If there are bytes (or a byte) in the SP Assembly Word which have not been transferred to Main Memory at END time, then two special STLs, 5ZS4 (END Main Memory Cycle Addr.) and 6AS4 (END Main Memory Read) are done to merge these bytes (or byte) into Main Memory.

2. During the fetching of the new CCW words all of the same checks and functions are performed as explained under Data Chaining with one important additional function. This is the setting of the Command Register by the new Command bits contained in the new CCW1 word.

3. Next, the 6AS3 and 5BS3 STLs are selected to send the new Command out over the DOUT lines to the device along with STROBE and TRAC. If no SCSR bits were set along the way, Normal is selected, otherwise 4AS3 and then to Normal.

4.3.18.3 END Servicing

When the count goes to zero $\overline{CD}$, the Selector TERMINATE flip-flop is set and is strobed out with STROBE flip-flop. The END could have been raised independently of the I/O if, for example, a gap had been reached on tape during a READ or one card read in from the Card Reader, etc. The Selector TERMINATE would also be set if a STERANY type error occurred during servicing or if a HALT Instruction is issued to this Selector.

When the SELECTOR TERMINATE flip-flop is set, the SR Terminate Inhibit logic (SRTINH 1 & 2) is activated to prevent servicing another SR. This logic performs the same function when the SELECTOR SET INTERRUPT flip-flop is set.

When the END line comes back with SR, one of the five entrance STLs will be entered. However, with END present, the following will be inhibited: Strobe; Set Interrupt; Set Terminate; Subtracting the byte count in T-1 STLs; Updating the address in the Main Memory or Data Move addressing STLs; or activating the SRTINH 1 & 2 logic.

Out of the entrance STLs, the END STATUS DECODE (4DS4) STL is selected whenever END line is present. In this STL the SDB, which is present on the DIN lines whenever END is received, is decoded. As a result of this decoding and other conditions (such as SCAD, REV, LT4, etc.) one of four possible STL paths is selected. A check is made to see if Command Chaining is to be performed. The requirements are as follows:

a. The SDB does not contain the Secondary Indicator (2^2 bit) or the Inoperable bit (2^1) and it does contain the Device End bit (2^3).

b. The CC Flag bit is set and the CD is not set.

c. The count is zero or the SLI (Suppress Length Indicator)Flag bit is set.

d. The operation being performed was not a LOAD.

e. There is not a STERANY type error.

f. A HALT Instruction has not been issued to this Selector Channel.

If Command Chaining is not called for, then the 6AS3 STL will be selected (possibly after the 5ZS4, 6AS4 pair for special case of END Main Memory Read covered under Command Chaining 4.3.18.2 and one of two possible Commands will be Strobed out along with TRAC. They are either SWITCH END if SSE (1)·SHALT or SET INTERRUPT if [SCDF(1)•SSE(0)] [STERANY/SCC(0)]/SSI(1)/ SHALT. In the following 5BS3 STL several clean up type functions are performed:

a. Generate I/O COMPLETE if SEND(1) QSTCSR(0)

b. Set SEND if STERANY•SSE(0)/SSI(1)

c. Set IOPE and reset RUN if [STERANY/SZ(1)] LOAD(1)

d. Reset LIP if SSI(1)

e. Reset LOAD if STERANY/SZ(1)

At the end of this STL, the Processor will return to Normal unless a Store Status is required QSTCSR(1) which will cause selection of 4AS3 STL first to perform this storing before returning to Normal.

4.3.19 OPTIONAL FEATURES

4.3.19.1 Memory Protect

The Memory Protect feature is packaged on a separate platter mounted in the Main Memory (Rack 42). The Engineering Logic Diagrams for the Memory Protect feature are: 3661577, 3661578, 3661583, 3661584, 3661587, and 3661588.

The Memory Protect platter includes a Memory Protect memory stack that is similar to the Scratch Pad memory stack. An address is set in the MPMAR (drawing 1588) where it is decoded to enable MP voltage switches (drawing 1577) and MP current drivers (drawing 1578). There are seven bit positions in the MPMAR that can provide a total of 128 addresses in the MP memory stack. The word length of an operand in the MP memory stack is 8 bits plus parity. A final addressing bit is clocked into the DIGIS flip-flop (1584-A4A), which selects either the odd or even half of the 8 bit word, thus providing a total of 256 separate 4 bit keys. Each key is applicable to a unique Main Memory block of 2,048 bytes.

Each of the 4 Program States has a separate Interrupt Status Register which includes, along its 32 bits, a 4 bit key. When an interrupt occurs or a Program Control Instruction is executed, the Memory Protection Key is extracted from this field of the state being initiated and placed in a machine hardware register (drawing 233). The hardware key register may also be set from the maintenance console through the N register Select Switch function (see 4.2.10.3).

In addition to the Normal Mode hardware Key Register, there is a MUX Mode hardware Key Register on drawing 338 and (6) Selector Mode hardware Key Registers on drawings 369 and 1003. The function of the hardware Key Registers is to provide a comparison field against which the Memory Protect Key is checked (drawing 1587). Depending on the Mode of operation the appropriate hardware Key Register is permitted through the Key Comparator logic. Whenever data is to be stored in Main Memory the four bit Memory Protect Key is compared with the four bit hardware key. If the keys are equal, or either is zero, the data storage is permitted.

The signal KEYSOK (258-B5B) provides an inhibit for signal MMCSMRX-P if an unequal Key Compare is recognized. This is to prevent destruction of a protected Main Memory block. Also signal MPKER-N (258-C5F) is generated which primes gate 320-C5F to set the ADEX flip-flop. ADEX (320-C6D) is set on recognizing Key inequality only during Normal Mode. In the Mux Mode or Selector Mode the recognition of Key inequality will set the PROTCK flip-flop which will appear as bit 11 in the Channel Status Byte (see 4.3.7.2 or 4.3.16.5).

The Memory Protect storage key can be changed by the Privileged Instruction, Set Storage Key and can be inspected by the Privileged Instruction, Insert Storage Key. To write into the Memory Protect Stack, the Set Storage Key instruction (I08) is used. There are three execute status levels in this instruction: the first is 5Y1 whose purpose is to check an ADEX condition if the least significant 4 bits of the general register holding the MP address is not zero. The second status level (5B0) transfers the four bit key from

a general register to the Memory Protect Memory Register (see drawing 1584). The four bit key is duplicated in both the odd and even half of the eight bit MP Memory Registers. The third and final status level (5Y2) reads out contents of the MP Stack into the Memory Registers but inhibits the Strobe on the addressed key as a function of the DIGlS flip-flop. The result is an eight bit word plus generated parity that is a merge of a new 4 bit key plus a 4 bit key from the stack in either the odd or even half word. The Memory Register is then regenerated back into the Stack.

To read out of the Memory Protect Stack for inspection or verification, the Insert Storage Key instruction (I09) is used. There are two execute status levels in this instruction; the first is 5Y0 whose purpose is to read a word out of the Stack and transfer it to the BPU. This is accomplished by selecting either the odd or even half of the MP Memory Register as a function of the DIGlS flip-flop and gating the outputs to set CFF(5-8). Since there is no path from the Memory Protect Platter to the Input Bus, the CFF(5-8) are used as a temporary storage register. In the second and final status level (5B0) the CFFs are read into DR digit six, and then regenerated into a Scratch Pad general register.

4.3.19.2 Direct Control

The Direct Control special feature is packaged on a separate platter mounted in the BPU rack 45. The Engineering Logic Drawings for the Direct Control feature are 3662890, 3662891, 3662892, and 3662893. The purpose of the Direct Control feature is to permit processor to processor transfer of control information in the form of an eight bit byte. Two privileged instructions are provided to accomplish this function. A Write Direction instruction (I84) implements the transfer of one eight-bit byte of control information from the transmitting processor. A Read direct instruction (I85) implements the acceptance of one eight-bit byte of control information at the receiving processor.

The first execution status level of the Write Direct instruction is 3Bl which reads out the trunk address from the GPML register into the DOUT register (see drawing 2890). The control byte is then fetched from Main Memory and placed in the DROUT register, (also on drawing 2890), during a 4BlSTL. During this STL the WROUT flip-flop is set to enable the gating out of the SOUT register on the SIGOUT lines. The next and final STL resets the WROUT flip-flop after permitting a minimum pulse of 600 nsec. on the SIGOUT lines. The control byte information in the DROUT register will not be altered unless another Write Direct instruction is executed. On drawing 2891 the DROUT register enables the STOUT transmitters for each of the six D.C. trunks.

The Read Direct instruction is normally issued in response to an external interrupt caused by a Write Direct from another processor. On drawing 2893 the EXS flip-flops are set by the occurrence of an appropriate SIGIN line. These lines are logically connected to the SIGOUT lines of the transmitting processor.

The first execution status level of the Read Direction instruction is 3Bl which reads out the trunk address from the GPML register into the SOUT register. The read in of the STIN lines (which are logically connected to the STOUT lines of the transmitting processor) is then gated by the SOUT

register to ensure an exclusive trunk read in. During the 5B1 STL the STIN lines are gated into the STIN Register which is later transferred to CFF(1-8). The CFFs are used as a temporary buffer for the control byte which is then transferred to DR and finally to main memory.

4.3.19.3 Elapsed Time Clock

The maintenance panel has a switch called INHETC (Inhibit Elapsed Time Clock). When the switch is in the ON state, the Processor cannot enter the elapsed time check loop. The INHETC switch breaks the ETOSC pulse line and thereby forces pin 4 of gate 321-C5D to stay low. This will inhibit SETETR (321-B5A) from setting the ETR flip-flop. If ETR flip-flop is not set, then the elasped time status levels can not be generated.

When INHETC is OFF, pin 4 of gate 321-C5D pulses at the line frequency of either 50 Hz (20 milliseconds), 60 Hz (16.6 ms), or 1 kHz (1 ms). In status level 5x1 (the first status level of staticizing), if the ET flip-flop (321-C5B) was set which in turn causes ETR flip-flop (321-B5C) to be set if EXEC (0), then the next status level generated is 3A2 which in turn generates status level 3Y1 (the first status level of elapsed time loop). In the elapsed time loop, the elapsed time count in Memory location $(50)_{16}$ is decremented once every 3.3 msec. The decrement count is 2^8 and 2^{10} bits for 60 Hz, 2^9 and 2^{10} bits for 50 Hz, or 2^0, 2^2, 2^3, and 2^6 bits for 1 KHz. When the result of the subtraction is negative, then the ETEX flip-flop (Elapsed Time Exception) 321-B7B, is set which will force the program to take an elapsed time interrupt.

4.4 DETAILED LOGIC DESCRIPTION

Appendix B, 70/55 Status Flows, is provided in Volume 3 of this manual to describe the detailed logic.

The information in Appendix B is organized in the following manner:

1. Functional Status Flow Diagrams
2. Machine Language Status Flow Diagrams
3. Op-Status Level Timing Sheets

4.4.1 FUNCTIONAL STATUS FLOW DIAGRAM

This is the high level Status Flow Diagram of an instruction or related group of instructions. Each status level box contains the name and maintenance panel display of the status level and a brief description of its function. Certain conditions which are tested to determine selection of the next status level are also shown.

The Functional Status Flow Diagrams are designed to show how the 70/55 Processor performs an instruction, using a non-technical language.

4.4.2 MACHINE LANGUAGE STATUS FLOW DIAGRAM

The Machine Language Status Flow Diagram presents the status level flow, using the logic language of the 70/55 Processor. Each status level box contains some of the processor internal operations, using the signal names found

on the logic block diagrams (Figures 4-3, 4-1 and 4-12). The status level name and Maintenance Panel display are also shown.

At the lower right corner of the status level box is the number of a page in the Op-Status Level Timing Sheets for that operation.

4.4.3 OP-STATUS LEVEL TIMING SHEETS

All the detailed logic of the 70/55 Processor is contained on the Op-Status Level Timing Sheets. Each Processor signal is plotted with respect to the TP generator. Each timing sheet is labelled with the Status Level and Instruction (or Instruction Group).

The timing of each signal or event is indicated by a bar on a grid which represents the TP's.

A key to a logic drawing is given with the signals. This key is an abbreviation which is used on the logic block diagrams (Figures 4-3, 4-1 and 4-12).

Each status level terminates with a Select signal. This term, Select, is a key to a logic drawing. All status level select logic is grouped in numerical order and are contained on drawings 268 to 282, 348 and 364.

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SECTION FIVE

MAIN MEMORY

5.1 GENERAL DESCRIPTION

The 70/55 Main Memory is a coincident-current system using one ferrite core per bit in a full switching mode. Memory word selection is achieved by means of X and Y currents coinciding at one core in each bit-plane. The minimum memory repetition rate is 840 nanoseconds and the access time is less than 380 nanoseconds after an execute command.

The memory is word oriented and has a 33 bit word length which is divided into four bytes and one parity bit (bit 32).

C0 - bits 24 through 31
C1 - bits 16 through 23
C2 - bits 08 through 15
C3 - bits 00 through 07

The full word is contained in two memory stacks -- bits 00 through 16 are in a "D" or 17 plane stack and bits 17 through 32 are in a "C" or 16 plane stack.

The basic memory contains 65,536 bytes (½ bank) and is expandable to 524,288 bytes (4 banks). The memory sizes are one-half bank, one bank, two banks and four banks. Banks one and two are contained in rack 42 and banks three and four are contained in rack 43. An additional 4096 bytes are contained in the "non-addressable" (NA) part of the memory. Only the first half of the first bank has the NA feature.

Each memory bank operates independently of the other banks. All the interface cabling between the basic processor and any one bank is completely independent of any other bank -- that is, there are no direct wire connections from any memory platter in bank I to any memory platter in banks II, III, or IV. Bank I receives interface signals from the basic processor platters through a number of interface cables directly to the edge connectors of the MM3CR and MM4CR platters in rack 42. All other interface connections from the basic processor to every other bank are routed through 75-pin connector blocks mounted on the processor side of rack 42.

5.1.1 MEMORY RACK ORIENTATION

The main memory is housed in a double rack as shown in Figure 5-1 (two banks are in one double rack). Tables 5-1 and 5-2 show a platter breakdown of the various memory sizes. Information flow at the platter level is shown in Figure 5-2. Several platters are designated with an R or L at the end; for example, MM3CR and MM3CL. Platters with this type designation (L or R) perform the same logical function but differ physically because of their mounting locations in the rack.

SECTION FIVE

MAIN MEMORY

5.1 GENERAL DESCRIPTION

The 70/55 Main Memory is a coincident-current system using one ferrite core per bit in a full switching mode. Memory word selection is achieved by means of X and Y currents coinciding at one core in each bit-plane. The minimum memory repetition rate is 980 nanoseconds and the access time is less than 380 nanoseconds after an execute command.

The memory is word oriented and has a 33 bit word length which is divided into four bytes and one parity bit (bit 32).

C0 - bits 24 through 31
C1 - bits 16 through 23
C2 - bits 08 through 15
C3 - bits 00 through 07

The full word is contained in two memory stacks -- bits 00 through 16 are in a "D" or 17 plane stack and bits 17 through 32 are in a "C" or 16 plane stack.

The basic memory contains 65,536 bytes (½ bank) and is expandable to 524,288 bytes (4 banks). The memory sizes are one-half bank, one bank, two banks and four banks. Banks one and two are contained in rack 42 and banks three and four are contained in rack 43. An additional 4096 bytes are contained in the "non-addressable" (NA) part of the memory. Only the first half of the first bank has the NA feature.

Each memory bank operates independently of the other banks. All the interface cabling between the basic processor and any one bank is completely independent of any other bank -- that is, there are no direct wire connections from any memory platter in bank I to any memory platter in banks II, III, or IV. Bank I receives interface signals from the basic processor platters through a number of interface cables directly to the edge connectors of the MM3CR and MM4CR platters in rack 42. All other interface connections from the basic processor to every other bank are routed through 75-pin connector blocks mounted on the processor side of rack 42.

5.1.1 MEMORY RACK ORIENTATION

The main memory is housed in a double rack as shown in Figure 5-1 (two banks are in one double rack). Tables 5-1 and 5-2 show a platter breakdown of the various memory sizes. Information flow at the platter level is shown in Figure 5-2. Several platters are designated with an R or L at the end; for example, MM3CR and MM3CL. Platters with this type designation (L or R) perform the same logical function but differ physically because of their mounting locations in the rack.

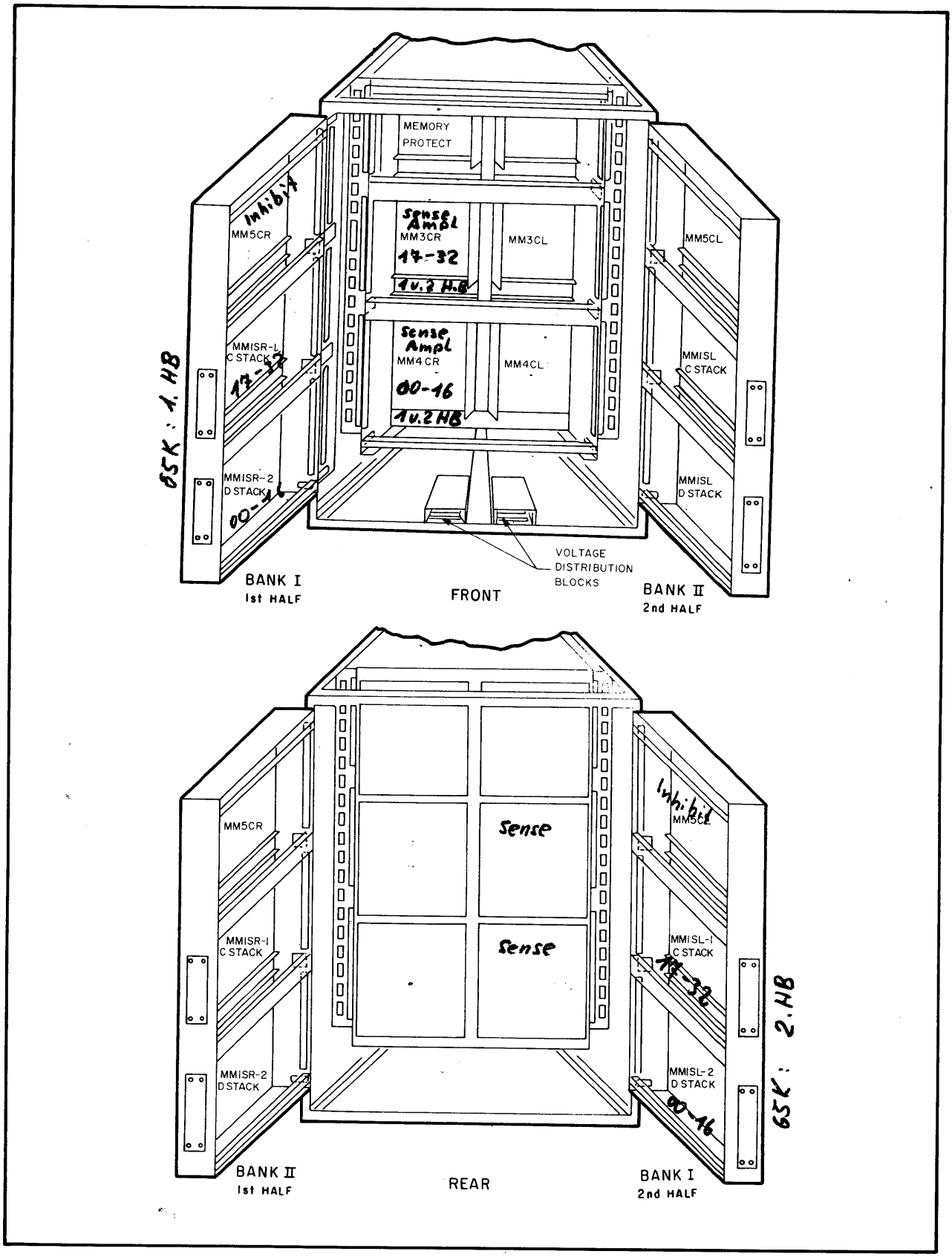

Figure 5-1. Model 70/55 Main Memory Platter Locations

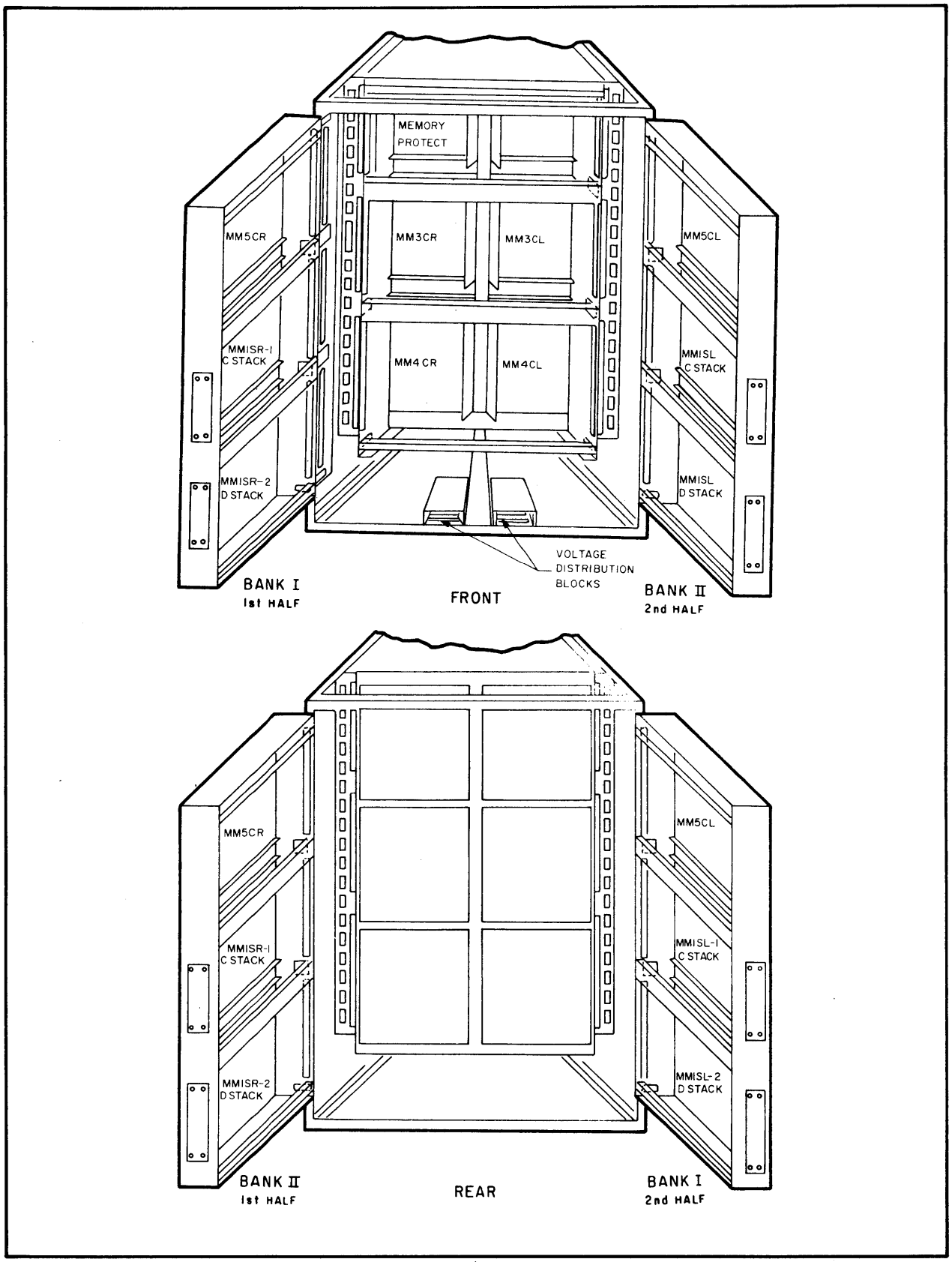

Figure 5-1. Model 70/55 Main Memory Platter Locations

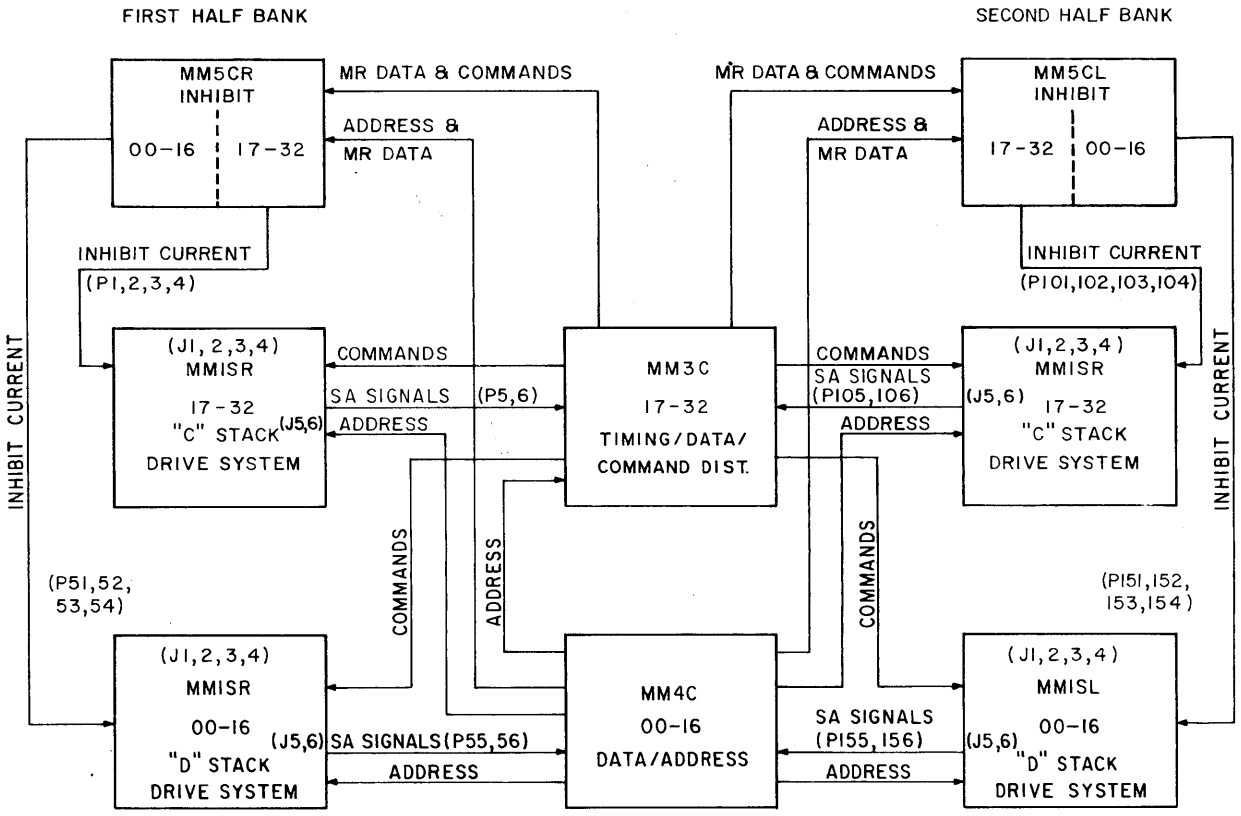

Figure 5-2. 70/55 Main Memory Internal Information Flow
(Full Bank)

5.1.2 PLATTERS

5.1.2.1 MM3CL and MM3CR Platters

The MM3CL and MM3CR platters contain all the control logic in the memory as well as registers and sense amplifiers for data bits 17-32.

Figure 5-3 shows the functional description of all the plug-ins on the platter. The MM3CL and MM3CR platters are identical in every respect except for the sense line cable dress; the cable dress on the MM3CL platter is to the left and the cable dress on the MM3CR platter is to the right.

5.1.2.2 MM4CL and MM4CR Platters

The MM4CL and MM4CR platters contain the memory address registers as well as registers and sense amplifiers for data bits 00-16.

Figure 5-4 shows the functional description of all the plug-ins on the platter. The MM4CL and MM4CR platters are identical in every respect except for the sense line cable dress; the cable dress on the MM4CL platter is to the left and the cable dress on the MM4CR platter is to the right.

Table 5-1. 70/55 Main Memory Platters

Platter Type	LOCATION Bank 1	Bank 2	Bank 3	Bank 4	Functional Description
MM5CR	42AA1A	42BA3A	43AA1A	43BA3A	Inhibit System
MM5CL	42BA1A	42AA3A	43BA1A	43AA3A	Inhibit System
MM1SR	42AA1B	42BA3B	43AA1B	43BA3B	Drive System and, "C" Stack
MM1SR	42AA1C	42BA3C	43AA1C	43BA3C	Drive System and, "D" Stack
MM1SL	42AA3B	42BA1B	43AA3B	43BA1B	Drive System and, "C" Stack
MM1SL	42AA3C	42BA1C	43AA3C	43BA1C	Drive System and, "D" Stack
MM3CR	42AA2B	-	43AA2B	-	Timing Generator, Sense Amplifiers and Memory Data Registers for bits 17-32, and Command Distribution logic.
MM3CL	-	42BA2B	-	43BA2B	
MM4CR	42AA2C	-	43AA2C	-	Sense Amplifiers and Memory Data Registers for bits 00-16, and Memory Address Registers
MM4CL	-	42BA2C	-	43BA2C	

Table 5-2. 70/55 Main Memory - Platter vs. Memory Size

Platter Type	Plug-In Logic Description	Memory Size (Bytes/Number of Banks) 65K/½	131K/1	262K/2	524K/4
MM5CR	Inhibit Drivers and Decoders	1	1	2	4
MM5CL	Inhibit Drivers and Decoders	0	1	2	4
MM1SR	X/Y Current/Voltage Switches/ Decoders ("C" Stack(s) (17-32) or "D" Stacks (00-16))	2 (2)	2 (2)	4 (4)	8 (8)
MM1SL	X/Y Current/Voltage Switches/ Decoders ("C" Stack(s) (17-32) or "D" Stacks (00-16))	0	2 (2)	4 (4)	8 (8)
MM3CR	Sense Amplifiers (17-32),	1	1	1	2
MM3CL	Delay Boards and Command Distribution Logic	0	0	1	2
MM4CR	Sense Amplifiers (00-16)	1	1	1	2
MM4CL	and Memory Address Register	0	0	1	2
	Total Platters (Total Stacks)	5 (2)	8 (4)	16 (8)	32 (16)

5.1.2.3 MM5CL and MM5CR Platters

The MM5CL and MM5CR platters contain the inhibit system decoding and the inhibit current drivers.

Figures 5-5 and 5-6 show the functional descriptions of all the plug-ins on the MM5CR and MM5CL platters respectively. Signal lines on both platters are identical but plug-ins at locations 6AT and 6AU and at 6BN and 6BO differ because of the functional orientation of the memory word. Bits 00-16 are on the right side of the MM5CL platter and bits 17-32 are on the left side. But on the MM5CR platter, bits 00-16 are on the left side and bits 17-32 are on the right side. Cable dress, as in the case of the MM3C and MM4C platters, has a left and right harness routing.

5.1.2.4 MM1SL and MM1SR Platters

The MM1SL and MM1SR platters contain the memory stacks, decoding for the current drive system and the current drive systems.

Figures 5-7 and 5-8 show the functional description of all the plug-ins on the MM1SL and MM1SR platters respectively. Both platters perform exactly the same function, but because of their locations in the rack, the memory stack mounting is different for both platters. The memory stack is mounted on the A side of the MM1SL platter and on the B side of the MM1SR platter.

5.1.3 CABLING

1. The following RCA Drawings listed in Table 5-3 specify the cable connections between the memory and the Basic Processor Unit (BPU).

Table 5-3. Main Memory and Processor Cable Drawings

From	To	Drawing No.
BPU	Memory Bank I	3682524
BPU	Memory Bank II	3682564
BPU	Memory Bank III	3682565
BPU	Memory Bank IV	3682566
Power Supply	Memory Rack #42	3670826-507
Power Supply	Memory Rack #43	3670826-509
Rack #42	Rack #42	3682689

2. The RCA Drawings listed in Table 5-4 specify the cable connections between the memory platters.

3. RCA Drawings 3662092 through 3662097 show the cable routing in memory racks 42 (Banks I and II) and 43 (Banks III and IV).

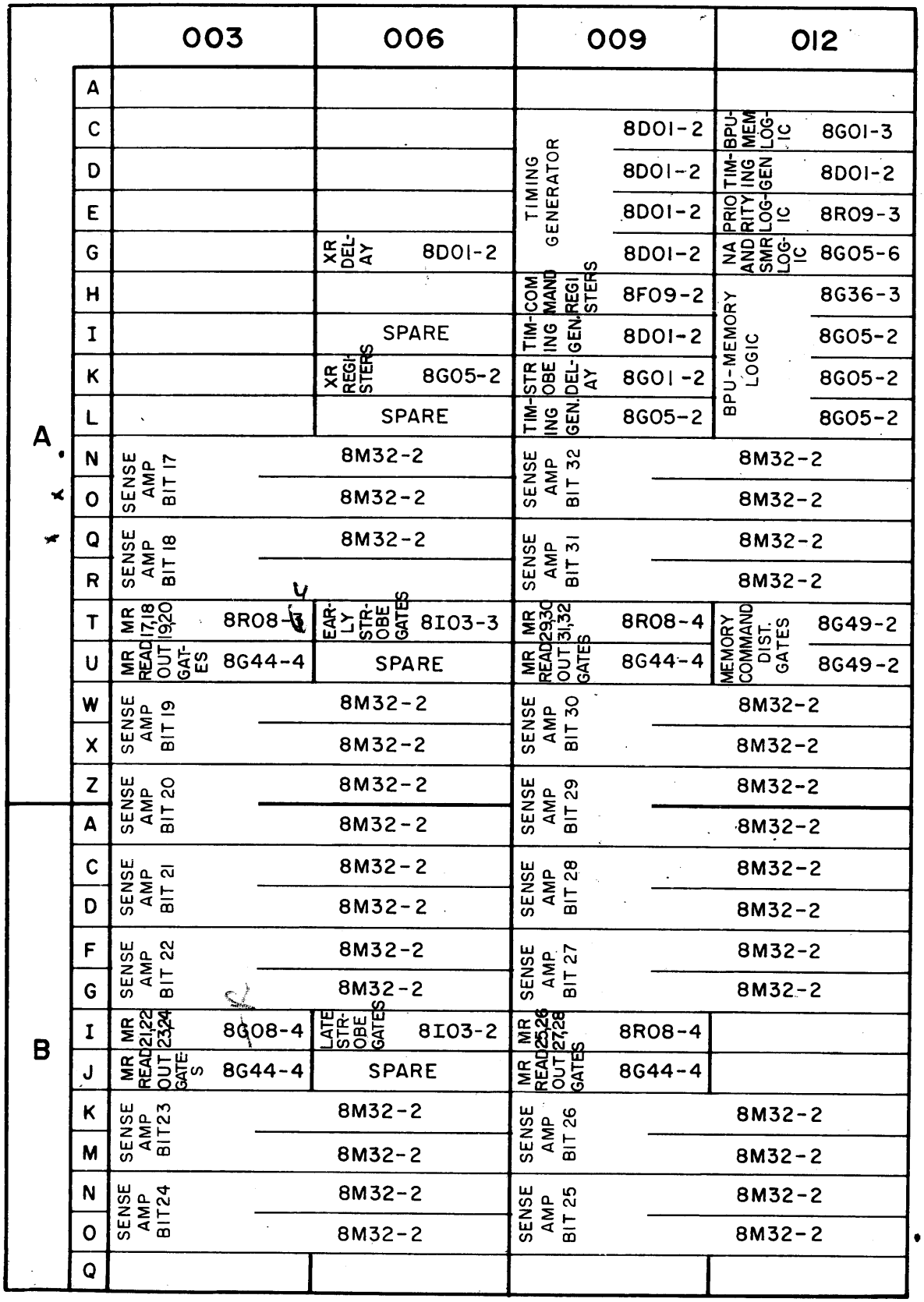

Figure 5-3. MM3CL, MM3CR Platter Plug-In Format

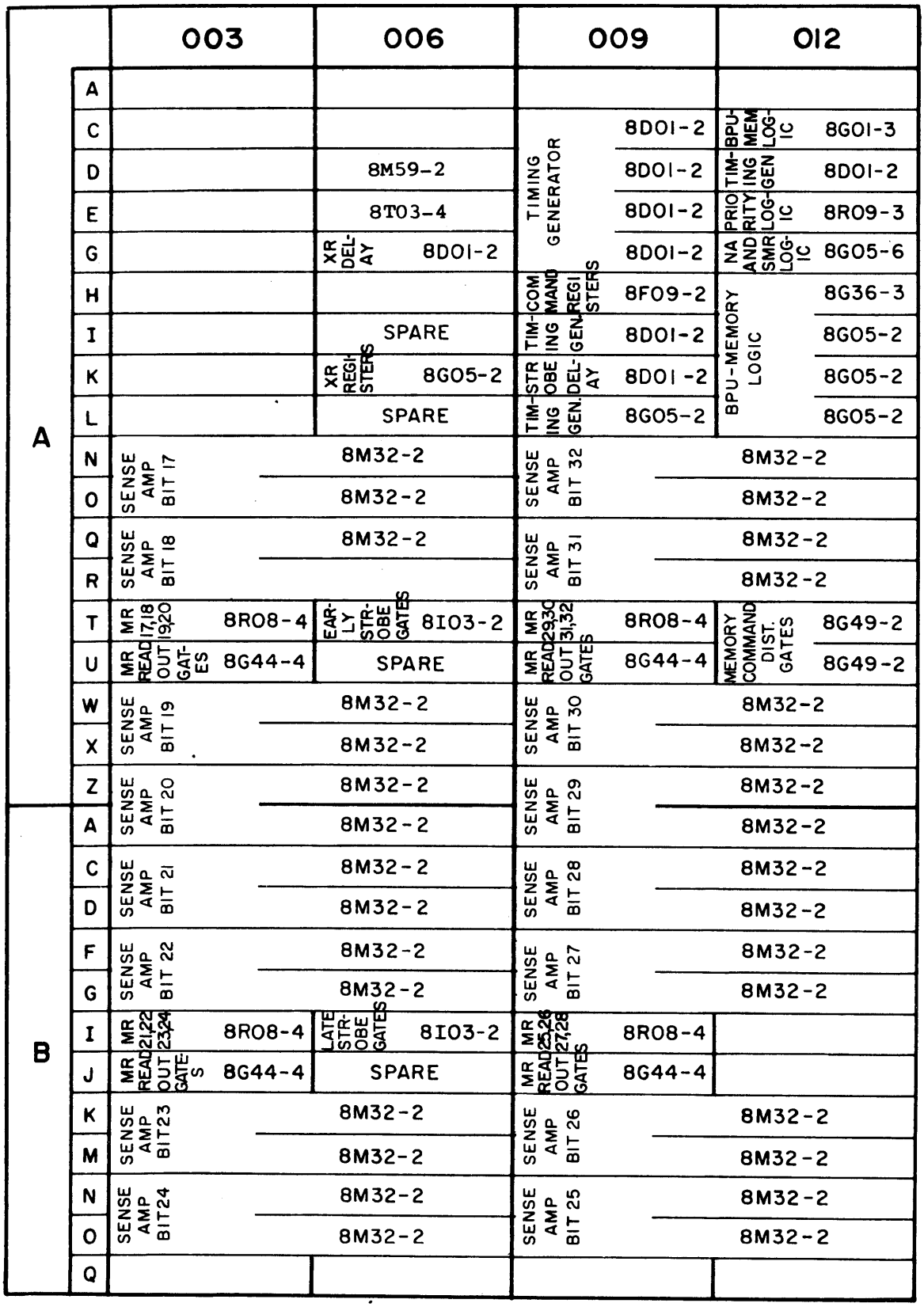

Figure 5-3. MM3CL, MM3CR Platter Plug-In Format

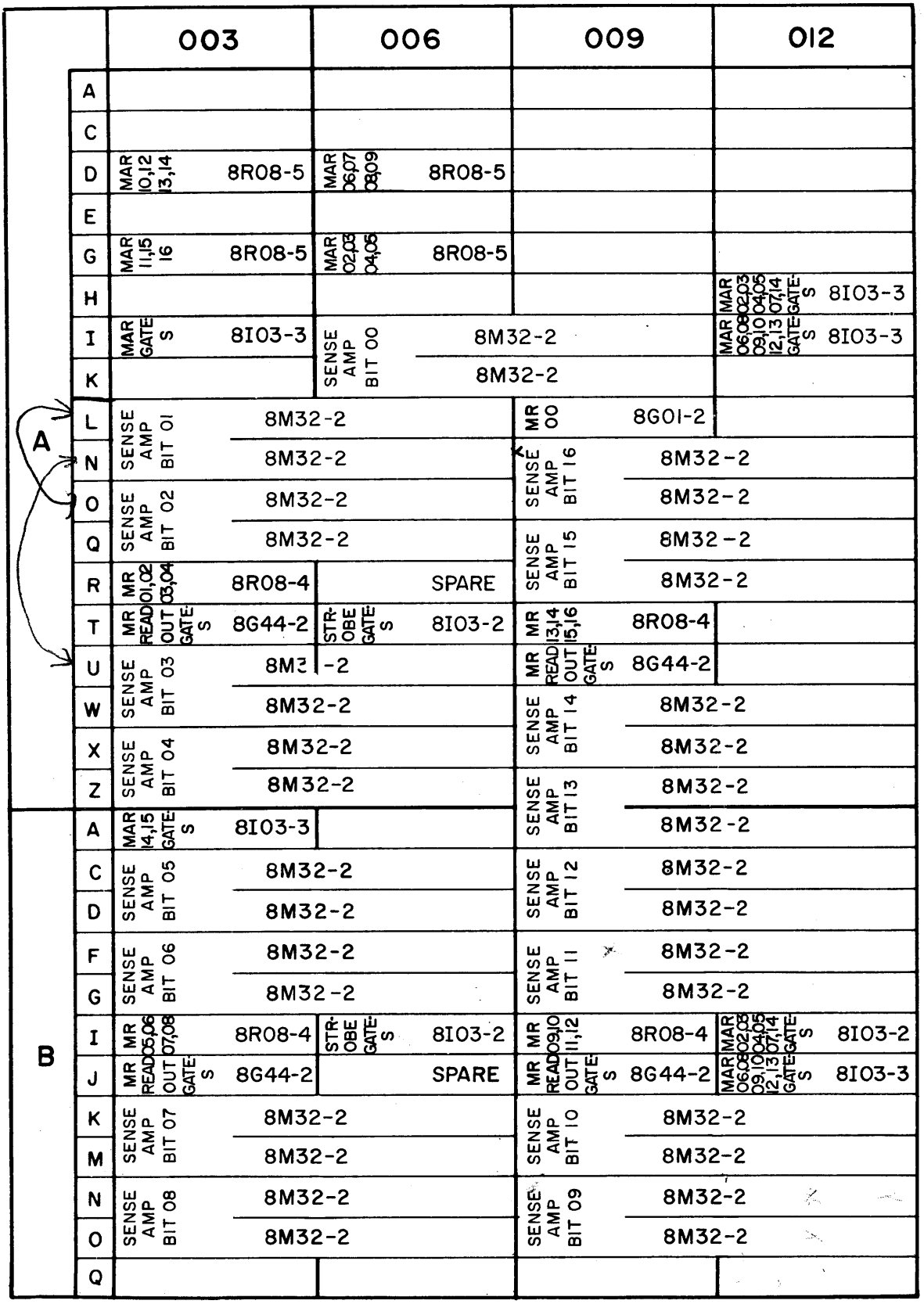

Figure 5-4. MM4CL, MM4CR Platter Plug-In Format

		003	006	009	012
A	A				
	C			INHIBIT BIT(23) 8M21-3	INHIBIT BIT(17) 8M21-3
	D			8M21-3	8M21-3
	E		INHIBIT BIT(29) 8M21-3	INHIBIT BIT(24) 8M21-3	INHIBIT BIT(18) 8M21-3
	G		8M21-3	8M21-3	8M21-3
	H		INHIBIT BIT(30) 8M21-3	INHIBIT BIT(25) 8M21-3	INHIBIT BIT(19) 8M21-3
	I		8M21-3	8M21-3	8M21-3
	K		INB DECODING (17,32) 8M20-6	SPARE	INB DECODING (17,32) 8M20-5
	L		INE (29,32) 8M22-3	INE (23,28) 8M22-3	INE (17,22) 8M22-3
	N		INHIBIT BIT(31) 8M21-3	INHIBIT BIT(26) 8M21-3	INHIBIT BIT(20) 8M21-3
	O		8M21-3	8M21-3	8M21-3
	Q		INHIBIT BIT(32) 8M21-3	INHIBIT BIT(27) 8M21-3	INHIBIT BIT(21) 8M21-3
	R		8M21-3	8M21-3	8M21-3
	T		SPARE	INHIBIT BIT(28) 8M21-3	INHIBIT BIT(22) 8M21-3
	U		SPARE	8M21-3	8M21-3
	W		SPARE	INHIBIT BIT(06) 8M21-3	INHIBIT BIT(00) 8M21-3
	X		SPARE	8M21-3	8M21-3
	Z		INHIBIT BIT(12) 8M21-3	INHIBIT BIT(07) 8M21-3	INHIBIT BIT(01) 8M21-3
B	A		8M21-3	8M21-3	8M21-3
	C		INHIBIT BIT(13) 8M21-3	INHIBIT BIT(08) 8M21-3	INHIBIT BIT(02) 8M21-3
	D		8M21-3	8M21-3	8M21-3
	F		INE (02,16) 8M22-3	INE (06,11) 8M22-3	INE (00,08) 8M22-3
	G		INB DECODING (00,16) 8M20-6	SPARE	INB DECODING 8M20-5
	I		INHIBIT BIT(14) 8M21-3	INHIBIT BIT(09) 8M21-3	INHIBIT BIT(03) 8M21-3
	J		8M21-3	8M21-3	8M21-3
	K		INHIBIT BIT(15) 8M21-3	INHIBIT BIT(10) 8M21-3	INHIBIT BIT(04) 8M21-3
	M		8M21-3	8M21-3	8M21-3
	N		INHIBIT BIT(16) 8M21-3	INHIBIT BIT(11) 8M21-3	INHIBIT BIT(05) 8M21-3
	O		8M21-3	8M21-3	8M21-3
	Q				

Figure 5-5. MM5CR Platter (Inhibit) Plug-In Format

		003	006	009	012
A	A				
	C			INHIBIT BIT 06 8M21-3	INHIBIT BIT 00 8M21-3
	D			INHIBIT BIT 06 8M21-3	INHIBIT BIT 00 8M21-3
	E		INHIBIT BIT 12 8M21-3	INHIBIT BIT 07 8M21-3	INHIBIT BIT 01 8M21-3
	G		INHIBIT BIT 12 8M21-3	INHIBIT BIT 07 8M21-3	INHIBIT BIT 01 8M21-3
	H		INHIBIT BIT 13 8M21-3	INHIBIT BIT 08 8M21-3	INHIBIT BIT 02 8M21-3
	I		INHIBIT BIT 13 8M21-3	INHIBIT BIT 08 8M21-3	INHIBIT BIT 02 8M21-3
	K		INB DEC. (00-16) 8M20-6	SPARE	INB DEC. (00-16) 8M20-5
	L		INE (12-16) 8M22-3	INE (06-11) 8M22-3	INE (00-05) 8M22-3
	N		INHIBIT BIT 14 8M21-3	INHIBIT BIT 09 8M21-3	INHIBIT BIT 03 8M21-3
	O		INHIBIT BIT 14 8M21-3	INHIBIT BIT 09 8M21-3	INHIBIT BIT 03 8M21-3
	Q		INHIBIT BIT 15 8M21-3	INHIBIT BIT 10 8M21-3	INHIBIT BIT 04 8M21-3
	R		INHIBIT BIT 15 8M21-3	INHIBIT BIT 10 8M21-3	INHIBIT BIT 04 8M21-3
	T		INHIBIT BIT 16 8M21-3	INHIBIT BIT 11 8M21-3	INHIBIT BIT 05 8M21-3
	U		INHIBIT BIT 16 8M21-3	INHIBIT BIT 11 8M21-3	INHIBIT BIT 05 8M21-3
	W		SPARE	INHIBIT BIT 23 8M21-3	INHIBIT BIT 17 8M21-3
	X		SPARE	INHIBIT BIT 23 8M21-3	INHIBIT BIT 17 8M21-3
	Z		INHIBIT BIT 29 8M21-3	INHIBIT BIT 24 8M21-3	INHIBIT BIT 18 8M21-3
B	A		INHIBIT BIT 29 8M21-3	INHIBIT BIT 24 8M21-3	INHIBIT BIT 18 8M21-3
	C		INHIBIT BIT 30 8M21-3	INHIBIT BIT 25 8M21-3	INH.BIT BIT 19 8M21-3
	D		INHIBIT BIT 30 8M21-3	INHIBIT BIT 25 8M21-3	INH.BIT BIT 19 8M21-3
	F		INE (29-32) 8M21-3	INE (23-28) 8M22-3	INE (17-22) 8M22-3
	G		INB DEC. (17-32) 8M20-6	SPARE	INB DEC. (17-32) 8M20-5
	I		INHIBIT BIT 31 8M21-3	INHIBIT BIT 26 8M21-3	INHIBIT BIT 20 8M21-3
	J		INHIBIT BIT 31 8M21-3	INHIBIT BIT 26 8M21-3	INHIBIT BIT 20 8M21-3
	K		INHIBIT BIT 32 8M21-3	INHIBIT BIT 27 8M21-3	INHIBIT BIT 21 8M21-3
	M		INHIBIT BIT 32 8M21-3	INHIBIT BIT 27 8M21-3	INHIBIT BIT 21 8M21-3
	N		SPARE	INHIBIT BIT 28 8M21-3	INHIBIT BIT 22 8M21-3
	O		SPARE	INHIBIT BIT 28 8M21-3	INHIBIT BIT 22 8M21-3
	Q				

Figure 5-6. MM5CL Platter (Inhibit) Plug-In Format

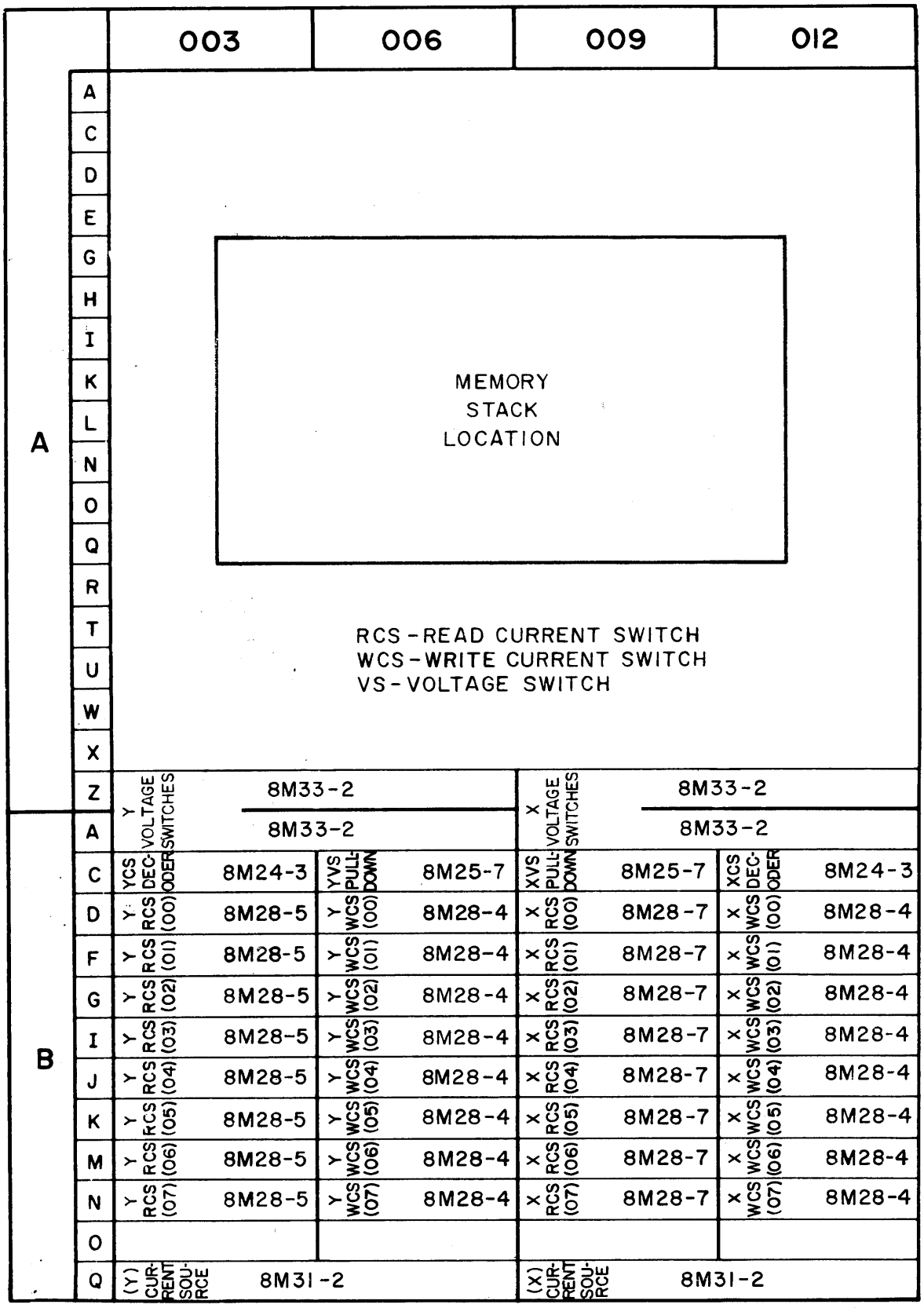

Figure 5-7. MM1SL Platter Plug-in Format

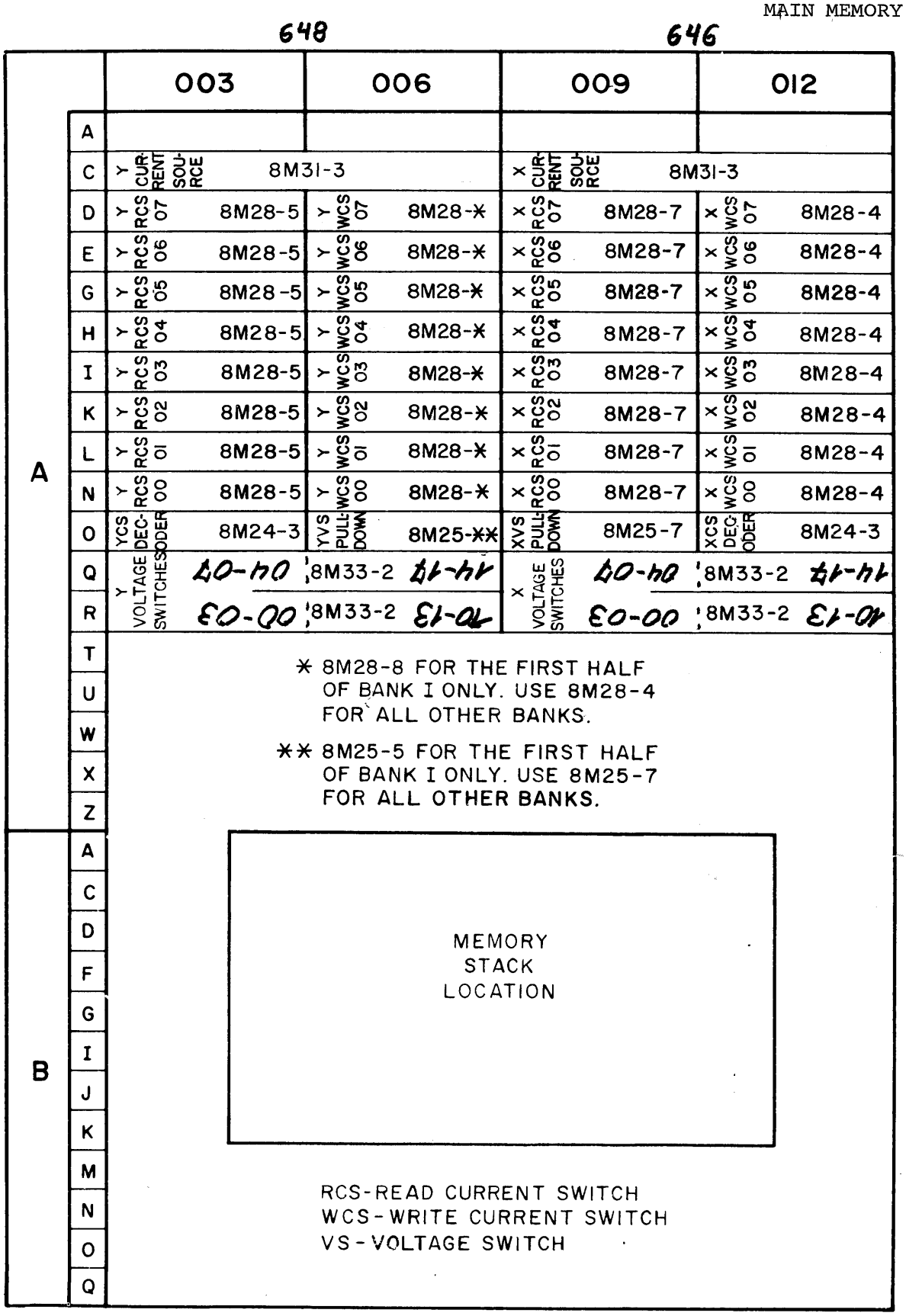

Figure 5-8. MM1SR Platter Plug-In Format

Table 5-4. Main Memory Platter Cable Drawings

From	To	Drawing No.
1-MM3CR	1-MM4CR	3682552
1-MM3CR & MM4CR	1-MM1SR-1 & MM1SR-2	3682553
1-MM3CR & MM4CR	1-MM5CR	3682554
1-MM4CR	1-MM5CL	3682555
1-MM3CR	1-MM5CL	3682556
1-MM3CR & MM4CR	1-MM1SL-1 & MM1SL-2	3682557
2-MM3CL	2-MM4CL	3682558
2-MM3CL & MM4CL	2-MM1SR-1 & MM1SR-2	3682559
2-MM3CL & MM4CL	2-MM5CR	3682560
2-MM4CL	2-MM5CL	3682561
2-MM3CL	2-MM5CL	3682562
2-MM3CL & MM4CL	2-MM1SL-1 & MM1SL-2	3682563
3-MM3CR	3-MM4CR	3682570
3-MM3CR & MM4CR	3-MM1SR-1 & MM1SR-2	3682571
3-MM3CR & MM4CR	3-MM5CR	3682572
3-MM4CR	3-MM5CL	3682573
3-MM3CR	3-MM5CL	3682574
3-MM3CR & MM4CR	3-MM1SL-1 & MM1SL-2	3682575
4-MM3CL	4-MM4CL	3682576
4-MM3CL & MM4CL	4-MM1SR-1 & MM1SR-2	3682577
4-MM3CL & MM4CL	4-MM5CR	3682578
4-MM4CL	4-MM5CL	3682579
4-MM3CL	4-MM5CL	3682580
4-MM3CL & MM4CL	4-MM1SL-1 & MM1SL-2	3682581

4. The sense cable connections are as follows:

1st Half Bank	MM3C P5	MM1SR-1 P5	Bits 17-32
	MM3C P6	MM1SR-1 P6	
	MM4C P55	MM1SR-2 P55	Bits 00-16
	MM4C P56	MM1SR-2 P56	
2nd Half Bank	MM3C P105	MM1SL-1 P105	Bits 17-32
	MM3C P106	MM1SL-1 P106	
	MM4C P155	MM1SL-2 P155	Bits 00-16
	MM4C P156	MM1SL-2 P156	

5. Inhibit cabling connections are specified in RCA Drawings 3630186 and 3630187.

5.1.4 MEMORY LOGIC

The logic functions of the memory are shown on 27 logic sheets; see Table 5-5 for details. The organization of the memory logics, as they relate to the memory stacks, is shown in Figure 5-9.

Table 5-5. 70/55 Main Memory Logic Drawings

RCA Drawing No.	Description
3661635	Timing Generator
3661636	Timing Generator
3661637	Command Distribution
3661638	Memory Address Register, (MAR02-05,11,16)
3661639	Memory Address Register, (MAR06-10,12-14)
3661640	Memory Register, (MR00-04,13-16)
3661641	Memory Register, (MR05-12)
3661642	Memory Register, (MR17-20,29-32)
3661643	Memory Register, (MR21-28)
3661644	Sense Amplifiers (SA00-16)
3661645	Sense Amplifiers (SA17-32)
3661646, 654	X Decoders, X Current and Voltage Switches
3661647, 655	X Drive Line Selection Matrix
3661648, 656	Y Decoders, Y Current and Voltage Switches
3661649, 657	Y Drive Line Selection Matrix
3661650, 658	Inhibit Driver Selection, (00-16)
3661652, 660	Inhibit Driver Selection, (17-32)
3661651, 659	Inhibit Drivers, (00-16)
3661653, 661	Inhibit Drivers, (17-32)

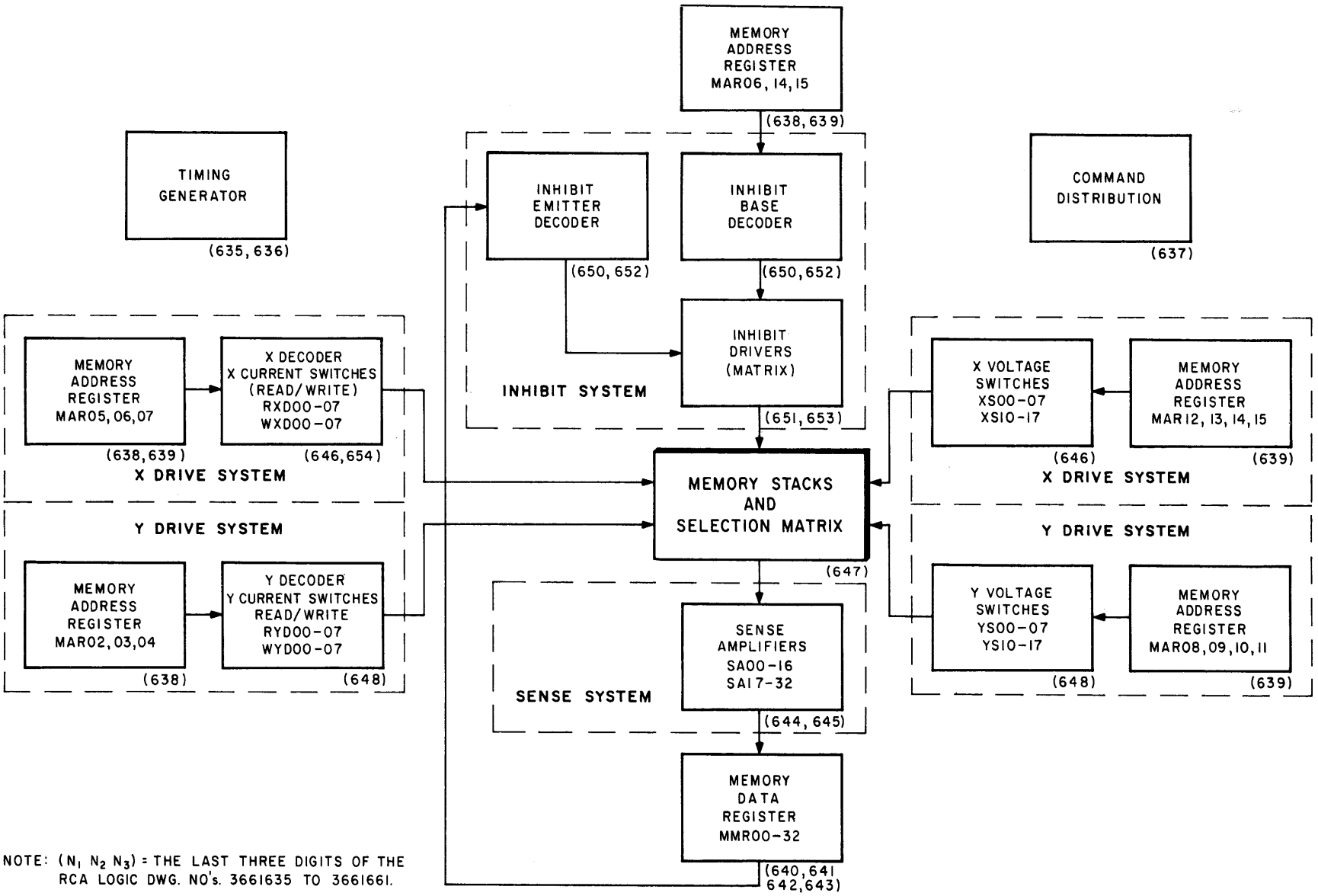

Figure 5-9. 70/55 Main Memory Logic Block Diagram

5.2 FUNCTIONAL CHARACTERISTICS

5.2.1 GENERAL

The 70/55 Main Memory is an asynchronous, random access memory. It has a unique feature of preventing a double start; that is, once the start or execute pulse begins the memory cycle, the execute signal has no affect on the memory until the cycle that was initiated is completed. The memory requires two timing pulses to complete one memory cycle: EXECUTE, which initiates a sequence of pulses that reads information from the memory (read sequence); and REGENERATE, which initiates a sequence of pulses that writes information into the memory (write sequence).

Information can be read out of the memory address registers at any time; however, information can only be transferred into the address registers with the initiation of a memory cycle.

The memory stack is used as a storage device for data information. Cores in the stack are switched by coincident X and Y currents.

A "split" cycle operation of the memory can be accomplished at the expense of increasing the memory cycle from the basic cycle time of 840 nanoseconds. An execute command initiates a read sequence which is completed approximately 420 nanoseconds later. Upon completion of the read sequence, the memory is inhibited from starting a write sequence until an external regenerate command is received. At this time data information can be changed but not addressing information. After the regenerate command is received by the memory, the write sequence is initiated and the memory cycle is completed with the termination of the write sequence.

5.2.2 DATA AND ADDRESS INFORMATION

Data and address information are sent from the basic processor unit (BPU) to the memory on the same signal lines but the information is controlled by time-differentiation of the strobe signals. Address information is strobed into the address registers several hundred nanoseconds before data information is strobed into the data registers.

5.2.3 ELECTRICAL REQUIREMENTS

5.2.3.1 Drive Currents

1. X Read Current - 460 ma $\pm$ 5%.
   Tr = 70 ns (10-90%), rise
   Tf = 70 ns (10-90%), fall
   Tw = 210 ns (50-50%), width

2. Y Read Current - 460 ma $\pm$ 5%. This current should begin 70 ns before the X Read Current.
   Tr = 70 ns (10-90%)
   Tf = 70 ns (10-90%)
   Tw = 285 ns (50-50%)

5.2 FUNCTIONAL CHARACTERISTICS

5.2.1 GENERAL

The 70/55 Main Memory is an asynchronous, random access memory. It has a unique feature of preventing a double start; that is, once the start or execute pulse begins the memory cycle, the execute signal has no affect on the memory until the cycle that was initiated is completed. The memory requires two timing pulses to complete one memory cycle: EXECUTE, which initiates a sequence of pulses that reads information from the memory (read sequence); and REGENERATE, which initiates a sequence of pulses that writes information into the memory (write sequence).

Information can be read out of the memory address registers at any time; however, information can only be transferred into the address registers with the initiation of a memory cycle.

The memory stack is used as a storage device for data information. Cores in the stack are switched by coincident X and Y currents.

A "split" cycle operation of the memory can be accomplished at the expense of increasing the memory cycle from the basic cycle time of 980 nanoseconds. An execute command initiates a read sequence which is completed approximately 490 nanoseconds later. Upon completion of the read sequence, the memory is inhibited from starting a write sequence until an external regenerate command is received. At this time data information can be changed but not addressing information. After the regenerate command is received by the memory, the write sequence is initiated and the memory cycle is completed with the termination of the write sequence. e

5.2.2 DATA AND ADDRESS INFORMATION

Data and address information are sent from the basic processor unit (BPU) to the memory on the same signal lines but the information is controlled by time-differentiation of the strobe signals. Address information is strobed into the address registers several hundred nanoseconds before data information is strobed into the data registers.

5.2.3 ELECTRICAL REQUIREMENTS

The following times are approximate (see DWG. 3685550 for Memory Timing). ■

5.2.3.1 Drive Currents

1. X Read Current - 460 ma ± 5%.
   Tr = 70 ns (10-90%), rise
   Tf = 70 ns (10-90%), fall
   Tw = 210 ns (50-50%), width

2. Y Read Current - 460 ma ± 5%. This current should begin 70 ns before the X Read Current.
   Tr = 70 ns (10-90%)
   Tf = 70 ns (10-90%)
   Tw = 285 ns (50-50%)

3. X and Y Write Current - 460 ma ± 5%.

   Tr = 70 ns (10-90%)
   Tf = 70 ns (10-90%)
   Tw = 210 ns (50-50%)

5.2.3.2 Inhibit Current - 400 ma ± 5%. The flat top of this current must bracket the flat top of the write currents.

   Tr = 90 ns (10-90%)
   Tf = 110 ns (10-90%)
   Tw = 300 ns (50-50%)

5.2.3.3 Signal Output (Under worst case disturb and data patterns terminated in the characteristic impedance of the sense winding).

The minimum "one" is 20 mV at the sense winding output and the maximum "zero" is 10 mV at the sense winding output. The ratio of "one" to "zero" at the peak time of the "one" is 5, minimum.

5.3.1 INTERFACE

The memory has interface connections with the power supply and with the basic processor unit. Figure 5-10 illustrates the signal and voltage flow to and from the memory. A more detailed interface chart is contained in Table 5-6. Table 5-6A shows the interface commands between the basic processor unit and the main memory. Table 5-6B shows the interface commands between the power supply and the main memory.

5.3.2 MEMORY TIMING CYCLE

5.3.2.1 Read Cycle

The memory timing cycle is shown in Figures 5-11 and 5-12. An execute signal (EX1-P) starts the memory cycle by initiating the following operations in the order listed below:

1. A memory present (MP1-P not shown in either figure, see logic 3661636) signal is sent to the basic processor if the memory bank is present.

2. A signal is generated to strobe in the address data which should be present on the data bus prior to the execute command.

3. The memory data registers (MRRES-P, Figure 5-12) are reset if an inhibit memory register reset (IMRRES1-P not shown in either figure, see logic 3661635) signal is not present.

4. A clock pulse for the voltage switch selection (VS-1N) is initiated.

5. If second half bank is addressed, an accept signal (AC1-P) is sent to the basic processor (provided that the memory capacity is greater than a half-bank). If the memory contains only the first half of the first bank, the accept command will not be sent when the second half bank is selected.

3. X and Y Write Current - 460 ma ± 5%.
   Tr = 70 ns (10-90%)
   Tf = 70 ns (10-90%)
   Tw = 210 ns (50-50%)

5.2.3.2 Inhibit Current - 400 ma ± 5%. The flat top of this current must bracket the flat top of the write currents.
   Tr = 90 ns (10-90%)
   Tf = 110 ns (10-90%)
   Tw = 300 ns (50-50%)

5.2.3.3 Signal Output (Under worst case disturb and data patterns terminated in the characteristic impedance of the sense winding).

The minimum "one" is 20 mV at the sense winding output and the maximum "zero" is 10 mV at the sense winding output. The ratio of "one" to "zero" at the peak time of the "one" is 5, minimum.

5.3.1 INTERFACE

The memory has interface connections with the power supply and with the basic processor unit. Figure 5-10 illustrates the signal and voltage flow to and from the memory. A more detailed interface chart is contained in Table 5-6A. Table 5-6A shows the interface commands between the basic processor unit and the main memory. Table 5-6B shows the interface commands between the power supply and the main memory.

5.3.2 MEMORY TIMING CYCLE

5.3.2.1 Read Cycle

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4. A clock pulse for the voltage switch selection (VS-1N) is initiated.

5. If second half bank is addressed, an accept signal (AC1-P) is sent to the basic processor (provided that the memory capacity is greater than a half-bank). If the memory contains only the first half of the first bank, the accept command will not be sent when the second half bank is selected.

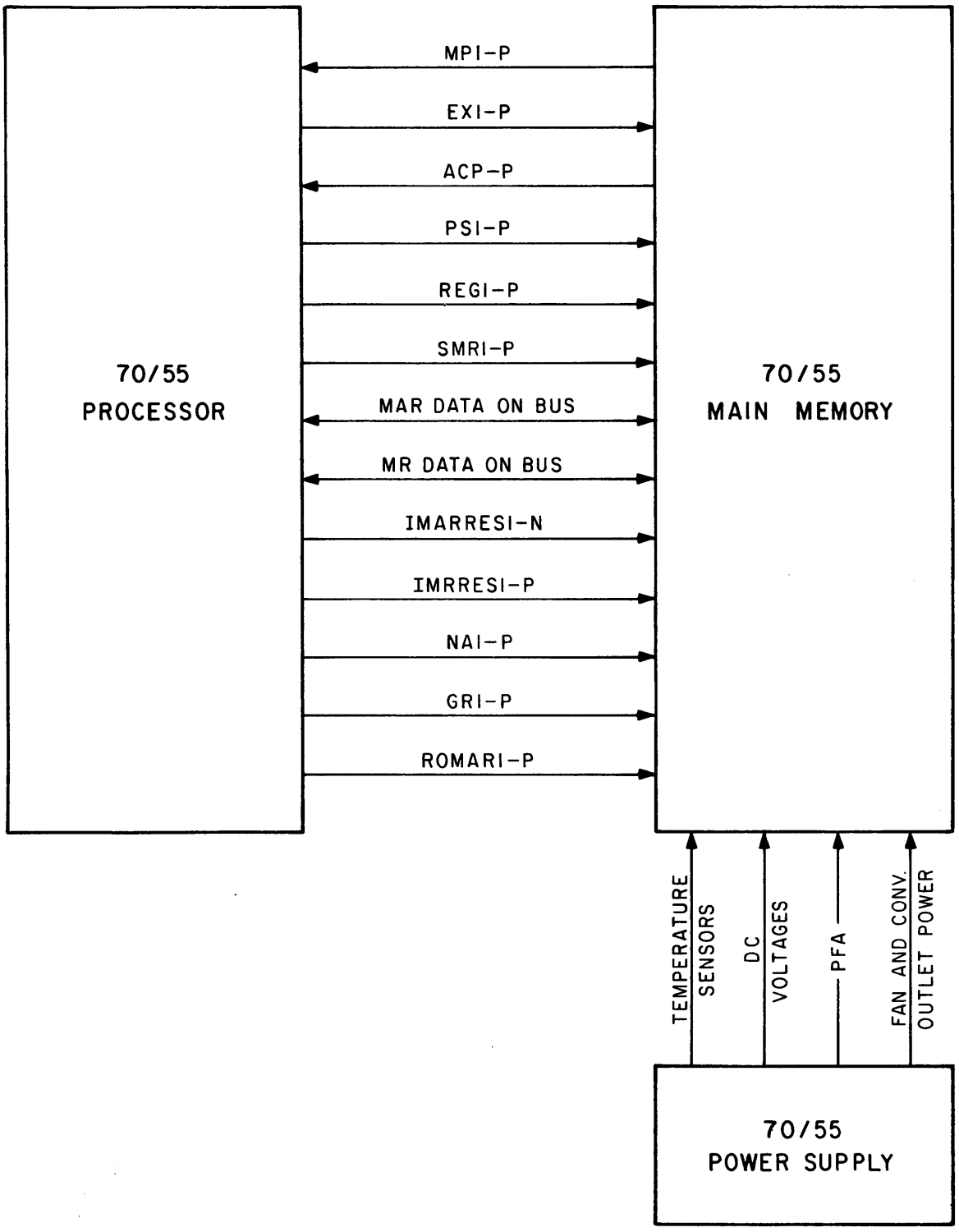

Figure 5-10. Interface Block Diagram

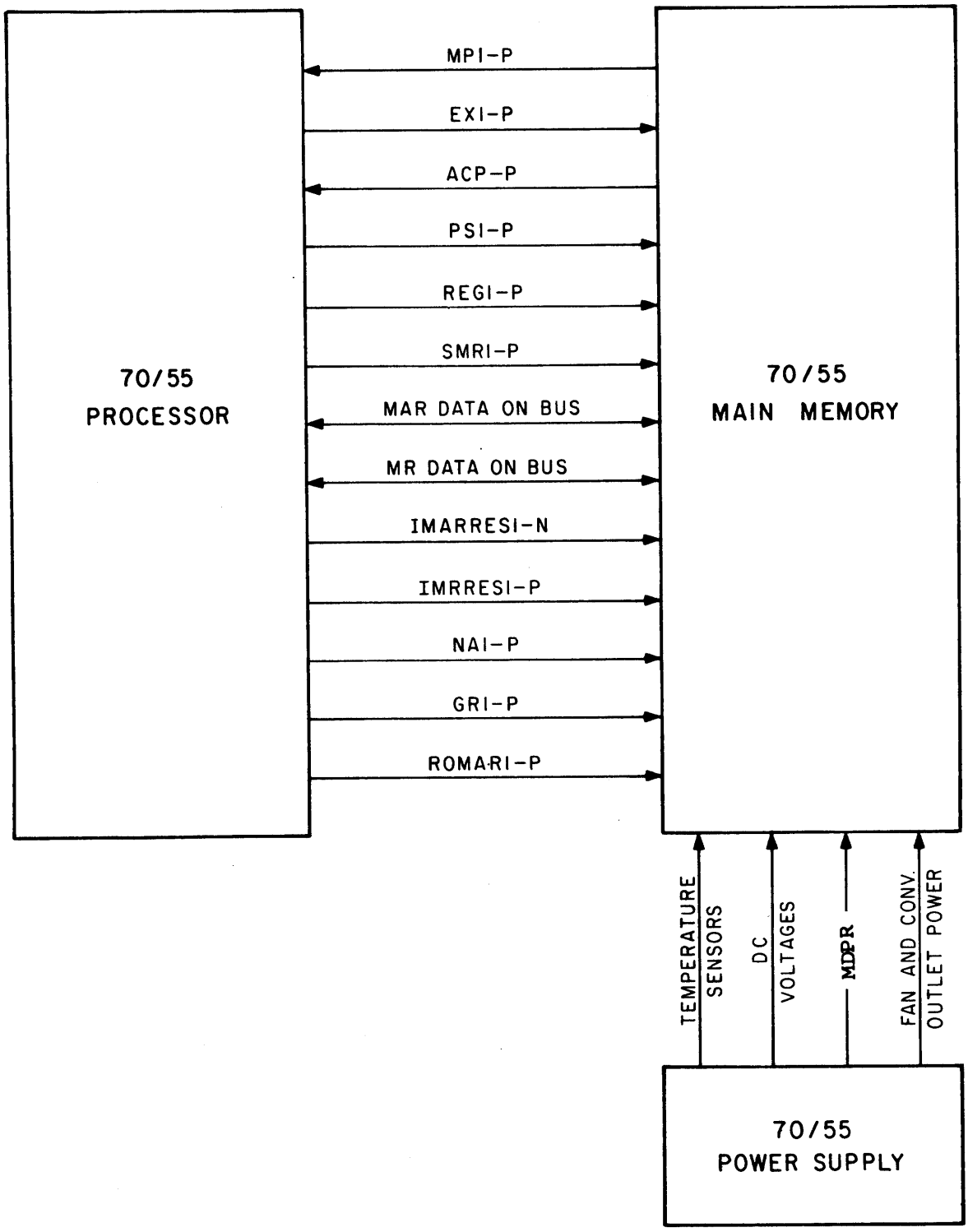

Figure 5-10. Interface Block Diagram

Table 5-6A. Interface Commands

BPU Command Name	MM Command Name	Functional Name	Function
MMCEX(A/B/C/D)-P 4 signals, 1 to each Bank; proper signal selected as follows: MA18 MA17 MMCEX 0 0 A 0 1 B 1 0 C 1 1 D	EX1-P	Execute	Request a memory cycle be performed by the selected Bank.
MIP (A/B/C/D)-P 4 signals, 1 from each Bank; only 1 Bank selected by EX1-P, so that only the selected Bank returns MIP: MIPA for MMCEXA MIPB for MMCEXB MIPC for MMCEXC MIPD for MMCEXD	MP1-P	Memory Present	Informs the BPU that the Half Bank selected exists on the system; if entire bank is absent, there is nothing to generate "MP"; if only one-half of this bank is present, MAR16 = 1 and inhibits MP. (See ACP)
ACP(A/B/C/D)-P 4 signals, 1 from each Bank; only one Bank selected by EX1-P, so only one Bank returns an ACP: ACPA for MMCEXA ACPB for MMCEXB ACPC for MMCEXC ACPD for MMCEXD	ACP1-P	Accept	Informs the BPU when the Execute command is going to be honored; BPU stops at CP and does not go to the next CP until Accept is received. As long as CP's are stopped, the Execute Command and the address are held on the interface. If the BPU does not receive MP1-P, the BPU does not wait for ACP1-P and generates ADEX (INT 223).
MMCNA-P One signal is sent to Bank A, since only Bank A contains a shaded memory.	NA1P One signal only since the Bank containing shaded memory cannot be shared.	Non-Addressable	The NA1-P is an address modifier that informs the Main Memory that the address wants to access the Shaded (non-addressable) Memory.
(1/2/3/4) Bus XX-N 132 signals, 33 to each bank; same bits appear on all four busses; only bus that is connected to the active bank will be used.	BUS XX-N1	BPU-Memory Data Bus	This bus is used to transfer 15 address bits and 33 data bits to a memory bank. Data XX = 00-32 (33 bits) Address XX = 02-16 (15 bits)
(1/2/3/4) DXXB-P 132 signals, 33 from each bank; only the bus from the active bank will contain bits: MMCEXA; data from 1DXXB MMCEXB; data from 2DXXB MMCEXC; data from 3DXXB MMCEXD; data from 4DXXB	DXX-P1	Memory-BPU Data Bus	This bus is used to transfer 15 address bits and 33 data bits from a memory bank to the BPU. Data XX = (00-32), (33 bits) Address XX = 02-16, (15 bits)
MMCPS(A/B/C/D)-P Four signals, 1 to each bank; only bank that received EX1-P will respond.	PS1-P	Permit Strobe	Informs the memory that information in the stack should be loaded into MMR during the Read cycle.
MMCSMR(A/B/C/D)-P Four signals, 1 to each bank; only the bank that received EX1-P will respond.	SMR1-P	Set Memory Register	Informs memory to reset MMR and read data on the BPU-Memory Data Bus into the MMR.
MMCREG(A/B/C/D)-P Four signals, 1 to each bank; only bank that has previously received EX1-P will respond.	REG1-P	Regenerate	Informs memory to write the present contents of the MMR into the stack.
MCROMAR-(A/B/C/D)-P Four signals, 1 to each bank; only the bank that last received EX1-P will respond.	ROMAR1-P	Read Out MAR	Informs memory to send the present contents of MAR to DXXB. Allows the Console display of MAR or snapshot of MAR.
IMARRES(A/B/C/D)-N Four signals, 1 to each bank; applicable only to the bank now cycling.	IMARRES1-N	Inhibit MAR Reset	Informs the memory Timing Generator not to reset MAR. Normally MAR is automatically reset following the Regenerate cycle, but IMARRES will preserve MAR for Console display, or snapshot
	IMRRES1-P	Inhibit Reset	Informs the Memory Timing Generator not to reset the MMR at the beginning of a Memory cycle. Normally the MMR is reset shortly after the Execute command is received but before information is read from the memory stack.
	GR1-P	General Reset	Resets all registers in the Memory.

Table 5-6B. Interface Commands

From Power Supply	MM Command Name	Functional Name	Function
One Cable Per Memory Rack	**MDPR**	**Memory Delay Power Reset**	**Unlocks the memory by resetting error control flip-flops**
	115V 60CPS Fans	Same	Cooling fan power
	High Temp n n=1 thru 6	High temperature sensing	Rack sensing for 131°F in the rack
	High Temp Comm	High temperature sensing common	Same as functional name
	Low Temp n n=1 thru 6	Low temperature sensing	Rack sensing for 122°F in the rack
	Low Temp Comm	Low temperature sensing common	Same as functional name
	115V 60CPS	Same	Convenience outlet power
	MARCHK n n=1, 2	Marginal Check Voltage	Provide marginal check voltage for individual Memory banks--one line per Memory bank
One Line Per DC Voltage Per Memory Rack	DC Voltages +50V,+30V,+10V, -5V, Ground	Same	DC power for memory operation

6. A Y read current (YR-1N) strobe pulse is initiated.

7. An X read current (XR-n_1n_2-N)* strobe pulse is initiated.

8. A strobe signal (STIX-P, see Figure 5-11) is generated if a permit strobe (PS1-P), signal is received from the basic processor. If a permit strobe signal is not received (see Figure 5-12), then the information at the memory location being addressed at that time will be destroyed.

9. Data will be automatically transferred from the sense amplifiers to the memory data registers and then to the memory-to-basic processor bus if the read-out-memory-address register (ROMARI-P not shown in either figure, see logic 3661635) is not present. The ROMARI-P signal will prevent the memory data from being transferred from the memory data register to the data bus.

The read cycle of the memory will be completed after the read drive currents decay.

* n_1n_2 = 1 or 2

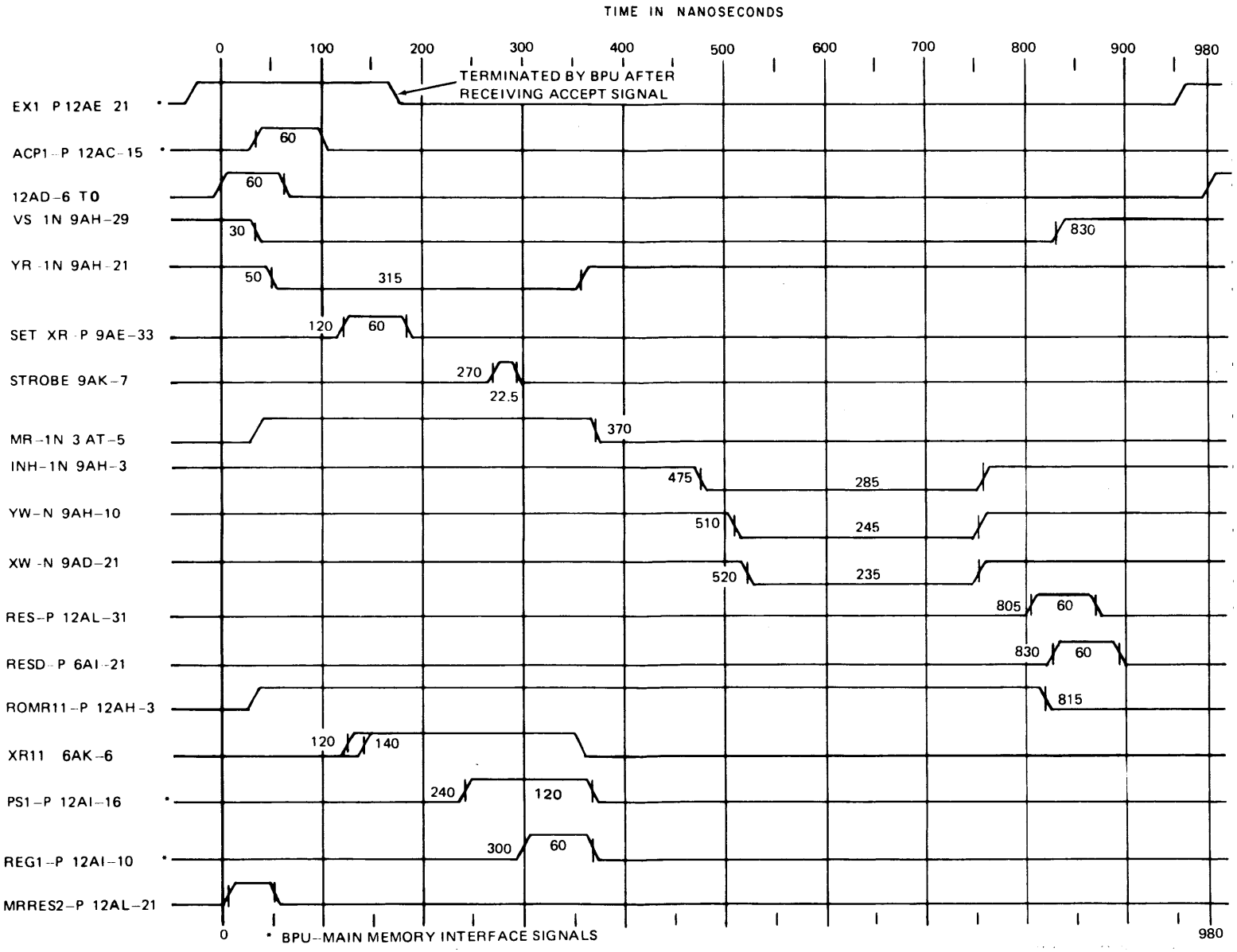

Figure 5-11. Timing Chart (Basic Read Cycle)

5.3.2.2 Write Cycle

The memory will not perform a write-data-into-memory function until a regenerate (REG1-P, see Figure 5-12) command is received from the basic processor. If the regenerate command is received before the read cycle is completed, then the write cycle will automatically begin upon completion of the read cycle. If, however, the regenerate signal is not received after completion of the read cycle, the memory will be "locked"; that is, a single address is decoded and the memory will not respond to any commands but a regenerate or a general reset (GR1-P, see logic 3661635) command. Even the execute command will not affect the memory when it is "locked". The general reset command will reset all memory registers and destroy all data present without a ready cycle but a regenerate command will store whatever data is in the data registers into the memory stack. After completion of a read cycle, new data can be sent to the memory and then transferred into the memory data register with the set memory register (SMR1-P) command. The SMR1-P command also initiates a memory data register reset to ensure correct data transfer from the data bus into the register. Data information remains at the set side of the data flip-flops approximately 50 nanoseconds longer than the reset pulse remains at the reset side of the flip-flop. In a split or read-write cycle, SMR1-P should not be present until completion of the read cycle. In split cycle operation, data is changed in the memory register after completion of the read cycle.

A regenerate command will initiate the following operations in the order listed below (see Figure 5-12):

1. An inhibit current (INH-1N) strobe pulse is initiated for those data bits that have "zeros" (or no information) stored in their data registers.

2. A Y write current (YW-1N) strobe pulse is initiated.

3. An X write current (XW-1N) strobe pulse is initiated.

4. After the drive and inhibit currents decay, all memory registers will be reset, completing the memory cycle unless the inhibit memory address register (IMMARRES1-N, not shown on any figure, see logic 3661636) command is sent from the basic processor. Presence of the IMMARRES1-N signal prevents generation of the reset signal which resets the memory data register, memory address registers, and all the memory control registers. When the IMMARRES1-N signal reverses polarity, from (N) to (P), then all registers in the memory will reset.

The memory is now ready for another execute command to initiate another memory cycle.

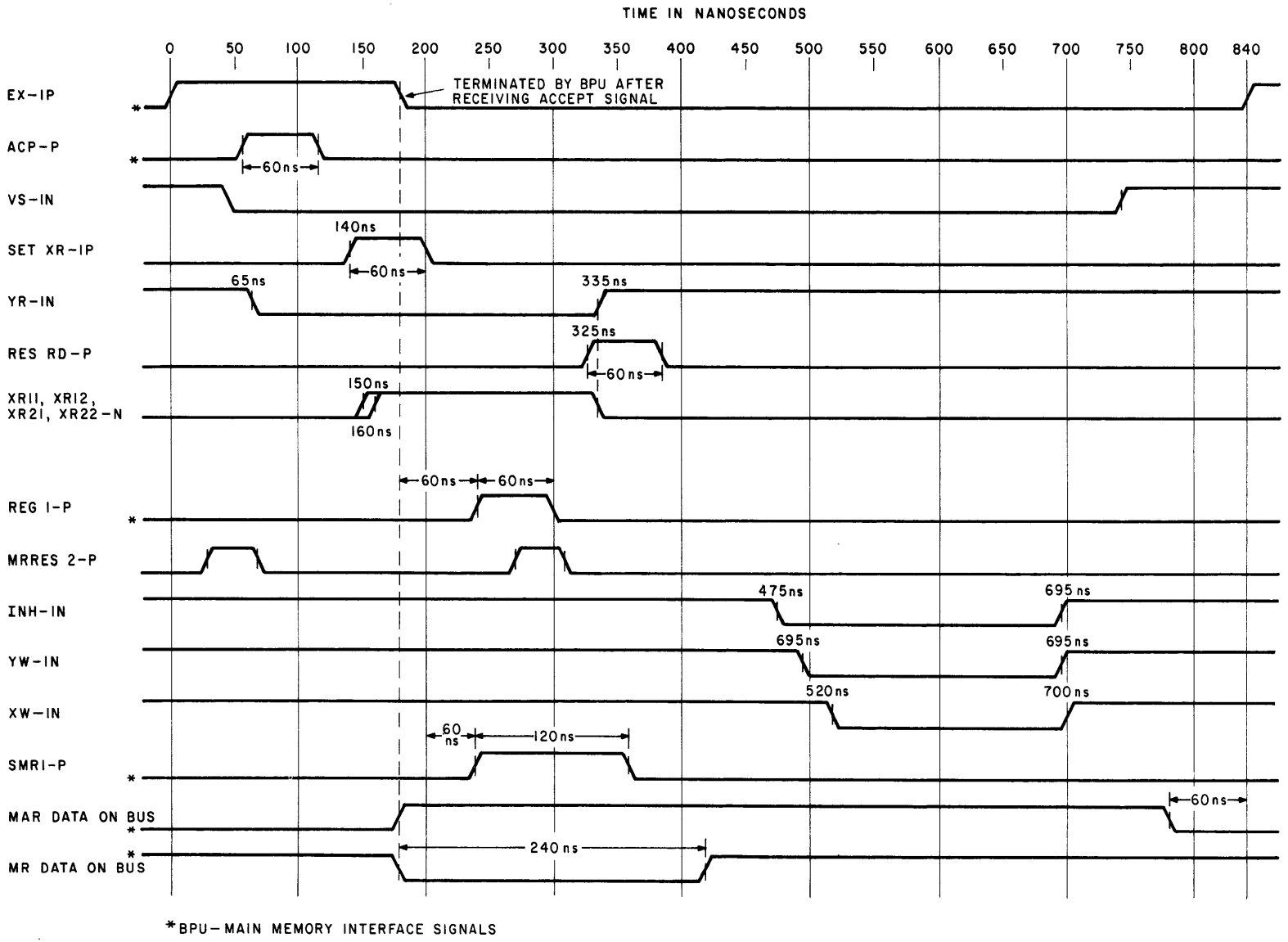

Figure 5-12. Timing Chart (Basic Write Cycle)

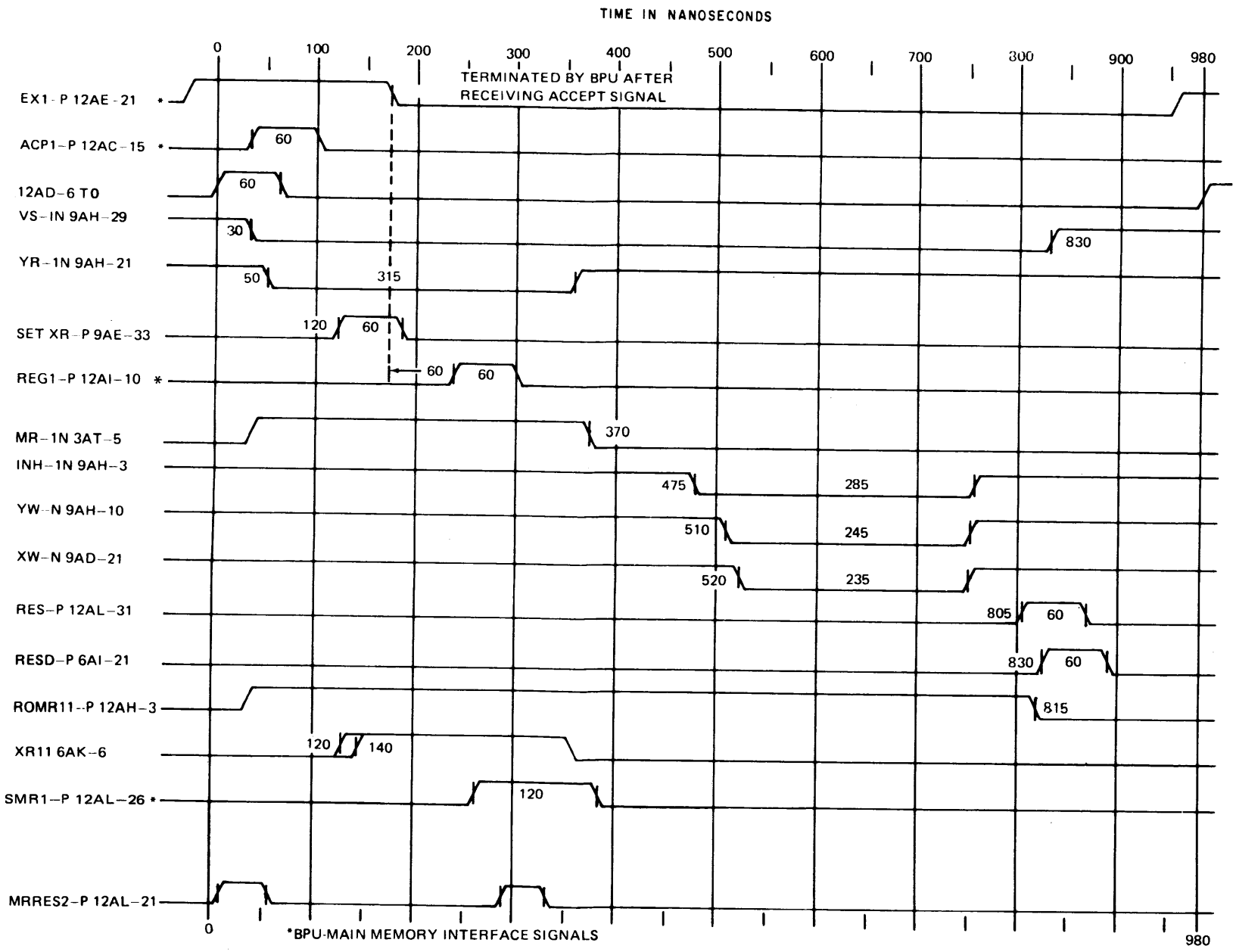

Figure 5-12. Timing Chart (Basic Write Cycle)

5.4 THEORY OF OPERATION

5.4.1 MEMORY OPERATION

Figure 5-13 shows a block diagram of the signal flow from the basic processor unit (BPU) through the memory and back again. Figure 5-14 shows a more detailed block diagram of the stack driver and sensing systems.

The execute (EX1-P) command initiates the memory cycle by activating the timing generator which generates synchronous pulses to select X and Y voltage switches, to select X and Y current switches, and to enable the sense amplifier if information is to be read from the memory.

The memory address register distributes addressing information to the drive system (X and Y) and the inhibit drive system. See Tables 5-7 through 5-13 for detailed decoding of the memory.

The Y read current is turned on first and 75 nanoseconds later the X read current is turned on. Both currents fall to zero at the same time. If the regenerate command is present, the Y write current will start approximately thirty nanoseconds after the read current falls to zero. Five nanoseconds later the X write current will start. The currents terminate in the reverse order from which they started the write sequence. Selected addresses must have X and Y coincident current throughout the 33 bits of the memory word line.

Signals from the core (nominally 28 millivolts peak) will appear at the sense amplifier approximately 140 nanoseconds after the X read current reaches 10% of its full amplitude. The core signal is amplified by the sense preamplifier, then by the sense amplifier (see Figures 5-13 and 5-20), and then passes through the discriminator. If the amplitude of the core signal is at least a minimum "one" amplitude when the strobe signal is present, then the output of the sense amplifier will set the memory data register.

Inhibit currents are activated during the write sequence if a "zero" or no information is to be written into the memory. The inhibit currents are turned on before the Y write current. When the inhibit currents reach approximately 80 to 90% of their final values, the Y and then the X currents are started. All currents are terminated in the reverse order from which they started the write sequence.

The inhibit currents cause a magnetizing flux which is in opposition to the X write currents. Neither the X nor the Y drive currents alone is sufficient to change the state of the core, therefore, cores which are not subjected to coincident X and Y currents remain in the unswitched or "zero" state.

5.4.2 MEMORY CONTROL LOGICS

There are three groups of logic which control the operation of the memory, namely the timing generator, address and data registers.

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The memory address register distributes addressing information to the drive system (X and Y) and the inhibit drive system. See Tables 5-7 through 5-13 for detailed decoding of the memory.

The Y read current is turned on first and 70 to 90 nanoseconds later the X read current is turned on. Both currents fall to zero at the same time. If the regenerate command is present, the Y write current will start approximately 50 nanoseconds after the read current falls to zero. From zero to 10 nanoseconds later the X write current will start. The currents terminate at the same time. Selected addresses must have X and Y coincident current throughout the 33 bits of the memory word line.

Signals from the core (nominally 28 millivolts peak) will appear at the sense amplifier approximately 160 nanoseconds after the X read current reaches 10% of its full amplitude. The core signal is amplified by the sense pre-amplifier, then by the sense amplifier (see Figures 5-13 and 5-20), and then passes through the discriminator. If the amplitude of the core signal is at least a minimum "one" amplitude when the strobe signal is present, then the output of the sense amplifier will set the memory data register.

Inhibit currents are activated during the write sequence if a "zero" or no information is to be written into the memory. The inhibit currents are turned on before the Y write current. When the inhibit currents reach approximately 80 to 90% of their final values, the Y and then the X currents are started. The Y and X currents terminate at the same time and the inhibit current termination follows.

The inhibit currents cause a magnetizing flux which is in opposition to the X write currents. Neither the X nor the Y drive currents alone is sufficient to change the state of the core, therefore, cores which are not subjected to coincident X and Y currents remain in the unswitched or "zero" state.

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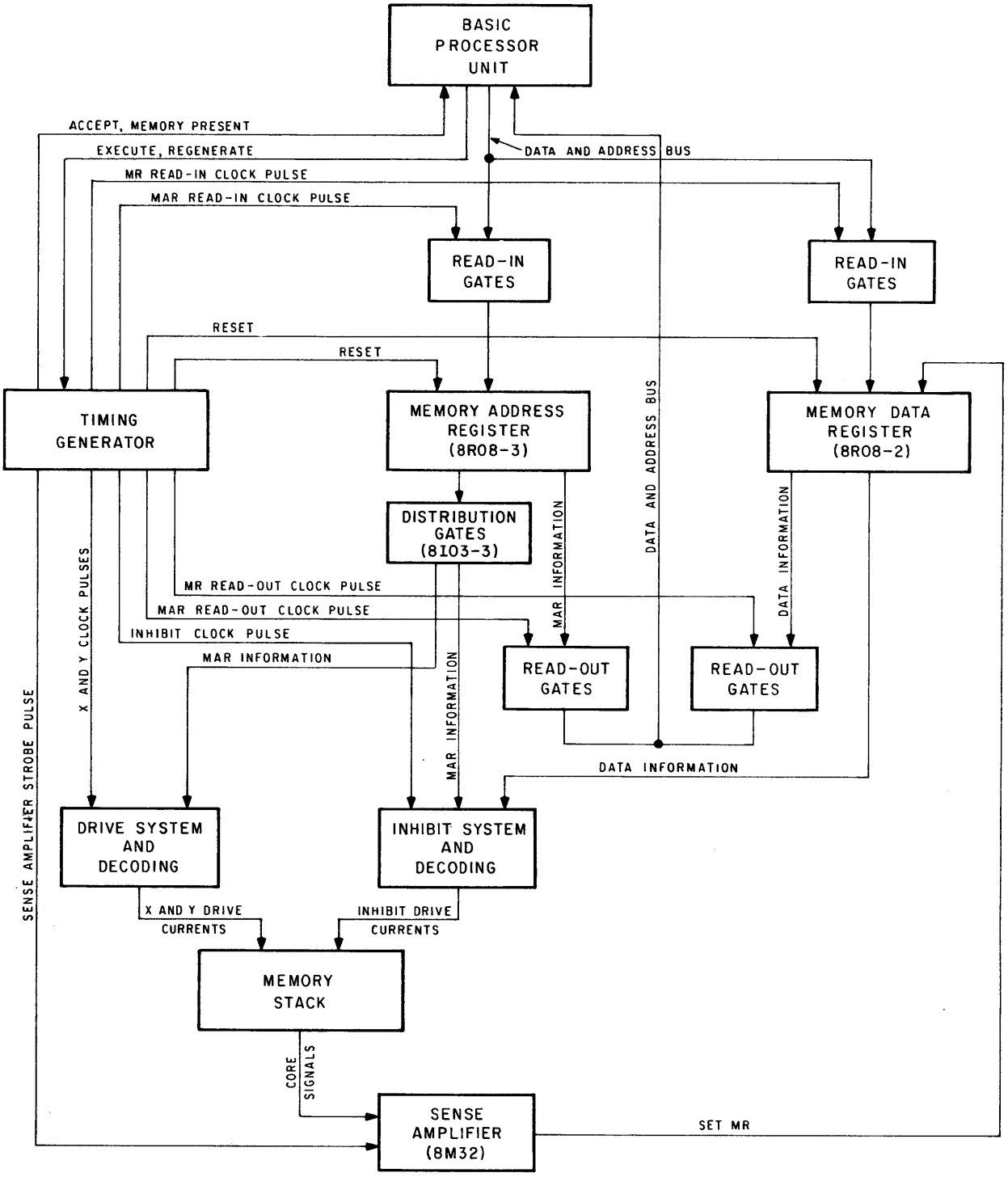

Figure 5-13. Main Memory Signal Distribution, Simplified Block Diagram

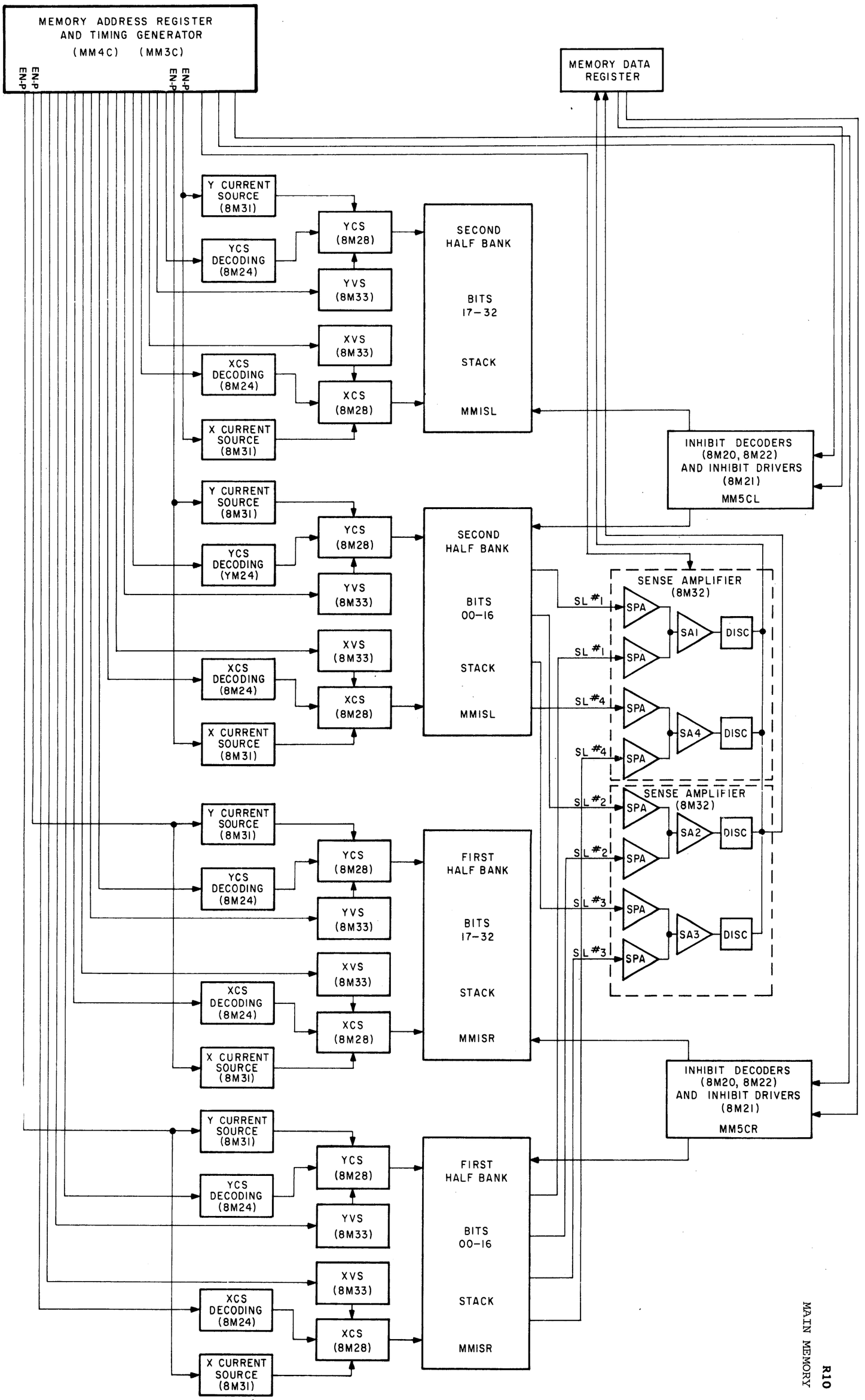

Figure 5-14. Main Memory, Detailed Block Diagram

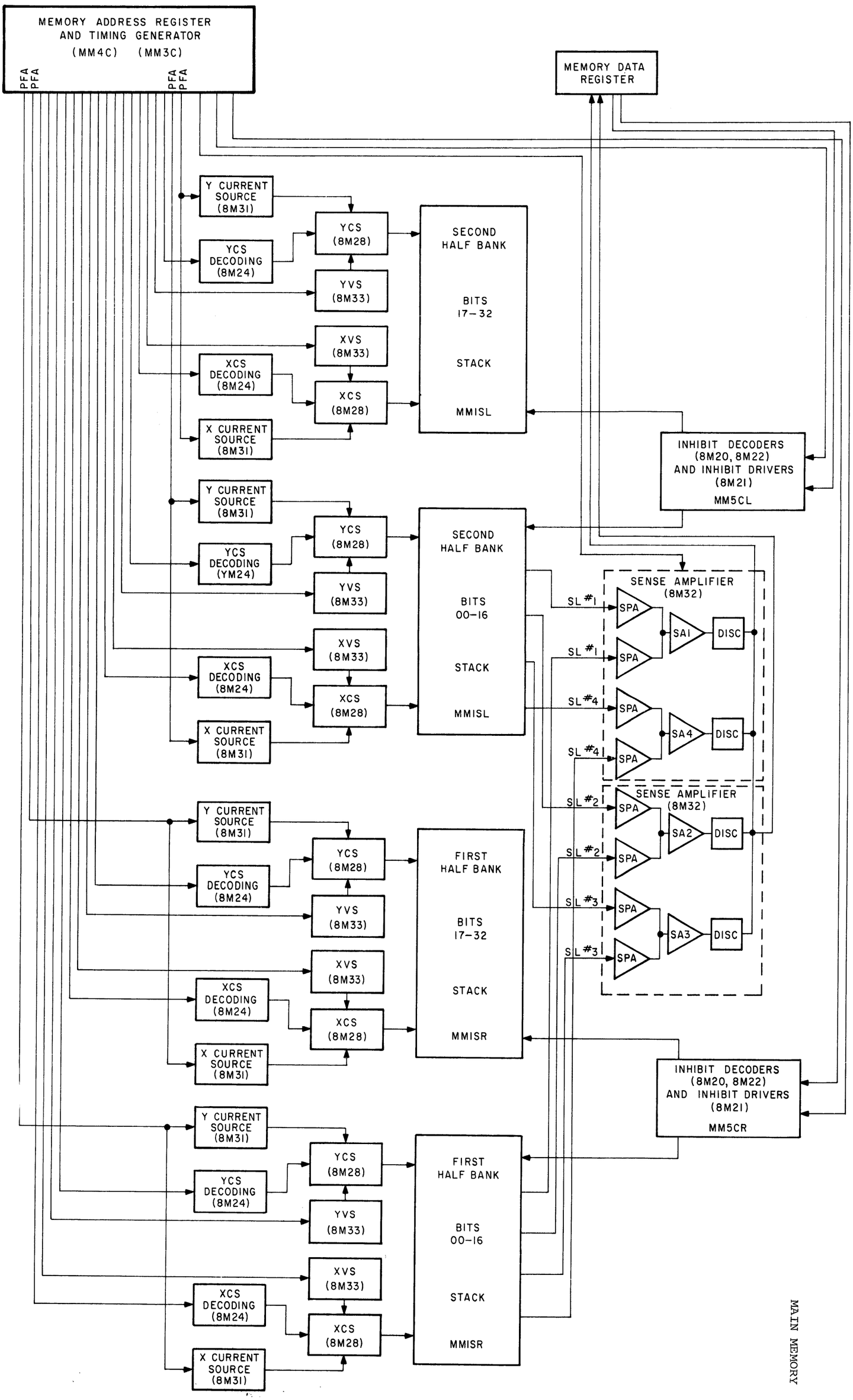

Figure 5-14. Main Memory, Detailed Block Diagram

5.4.2.1 Timing Generator

The timing generator consists of fixed delay lines, pulse shapers and timing gates which generate the clock pulses for the memory logics of a full bank. The initial setting of the timing circuits is dependent on the performance of the logics for a full bank of memory. The performance criteria of a full bank of memory is measured by the Marginal Range Check. Therefore, if any adjustments are made in the field on these timing circuits, they will affect the performance of a full bank of memory.

The timing generator, upon command from the Basic Processor Unit, provides the timing pulses which control the sequence of operating the memory. The timing pulses are derived from a chain of fixed delay lines and pulse shapers. The delay plug boards (8D01) are provided with tapped delay lines which allow setting of the timing pulses for optimum memory operation.

5.4.2.2 Memory Address Register

The Memory Address Register (MAR) consists of 15 (bits) flip-flops which receive address data from the BPU, provides temporary storage for the address data during the memory cycle, and distributes the data to the drive and inhibit systems for decoding purposes.

The MAR is common to both halves of a full bank.

5.4.2.3 Main Memory Register

The Main Memory Register (MMR) consists of 33 (bits) flip-flops which receives data information from the BPU or from the sense amplifiers, provides temporary storage during part or during the whole memory cycle, and supplies write information to the inhibit system decoders.

Data received from the BPU is temporarily stored in the MMR prior to being stored in the stack. Whereas data from the sense amplifiers is temporarily stored in the MMR prior to being sent to the BPU. Data information supplied to the inhibit system controls the information to be written into the stack ("one" or "zero") on a bit basis.

The (MMR) is common to both halves of a full bank.

5.4.3 MEMORY SUB-SYSTEMS

The main memory, Figure 5-13 is composed of three sub-systems: the drive system, inhibit system and sense system. Each bank of memory is, in turn, composed of two half-banks, Figure 5-14. Breaking down the memory still further, the memory word (33 bits) is divided into two half-words of which the first half contains bits 00-16 and the second half contains bits 17-32. Figure 5-15 shows the bit-stack relationship in the memory; each stack stores a half-word.

Every stack has its own inhibit and drive system but the sensing system is common to two stacks. Figure 5-14 shows the bit breakdown of the sensing system.

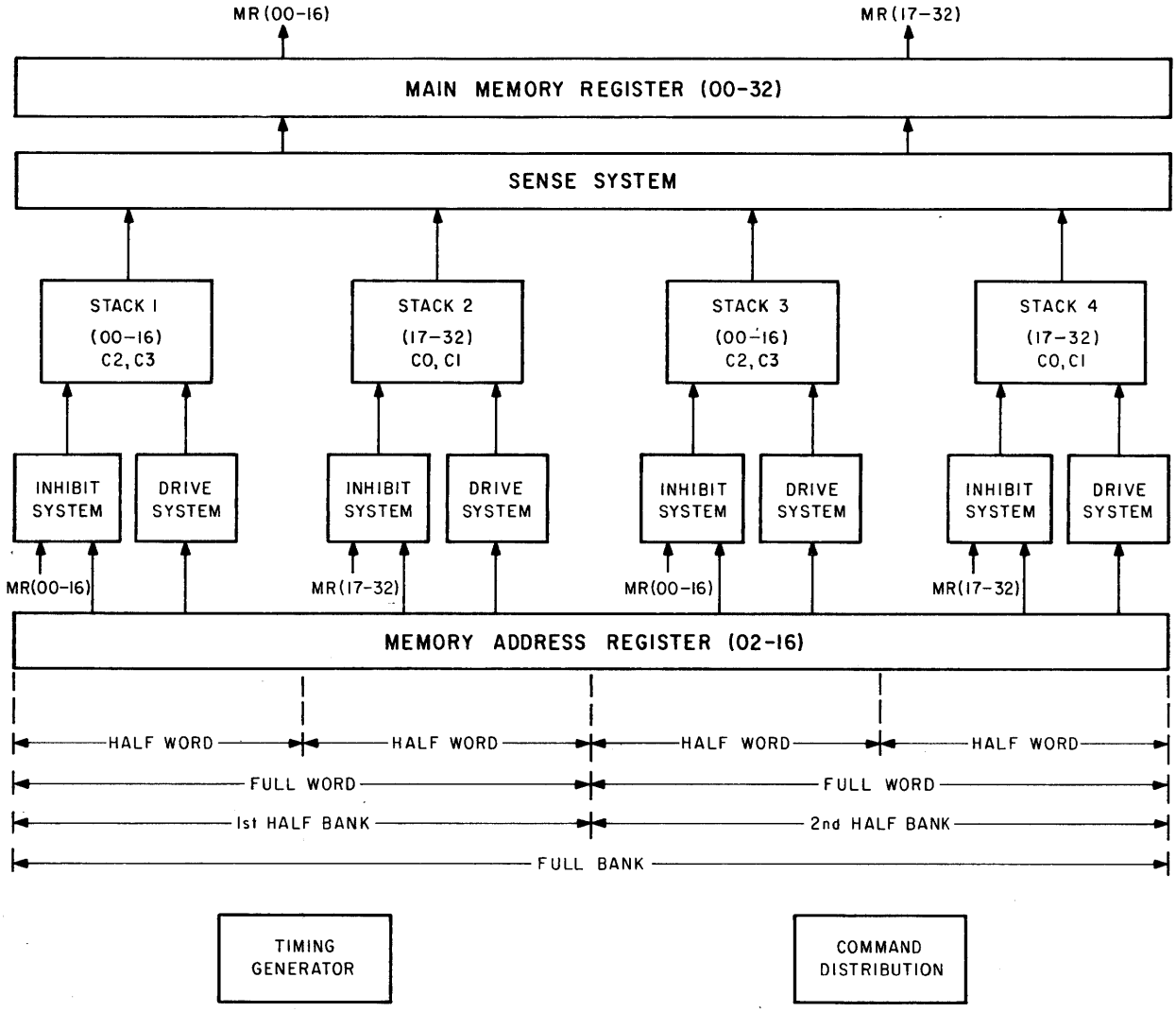

Figure 5-15. Main Memory, Systems Block Diagram

5.4.3.1 Drive System

The drive system consists of the X and Y current switches, voltage switches, decoders, and current sources which generate and control the drive currents for the separate stacks. The drive system accepts commands and address data, decodes this information, and provides the required drive currents on the selected drive lines. Each stack is separately accessed by the coincident X and Y drive currents. The area of the memory where coincidence occurs represents the address which is selected.

The drive system for each stack is composed of two completely separate sub-systems, the X and Y drive systems. These sub-systems are identical, except in the first half of the first bank. The Y drive sub-system has an additional voltage switch and eight additional output transformers. The total addresses available because of the additional circuits in the Y drive system are 1 x 8 x 128 (number of X lines) = 1024. The 1024 additional

addresses are called the Non-addressable area of the memory. A typical cross-section of a drive sub-system which selects and drives one drive line, is shown in Figure 5-16. A drive line is selected and energized by first turning on one of the sixteen voltage switches and then one of the eight read/write current switches. The output potential of the voltage switch is changed from its quiescent level of +30V to ground; the read timing clock pulse then turns on the read current switch. Current flows from the current source through the switch to one half of the drive transformer primary, and through the saturated voltage switch to ground. After the read current turns off, the write timing clock pulse turns on the write current switch and current flows through the other half of the drive transformer.

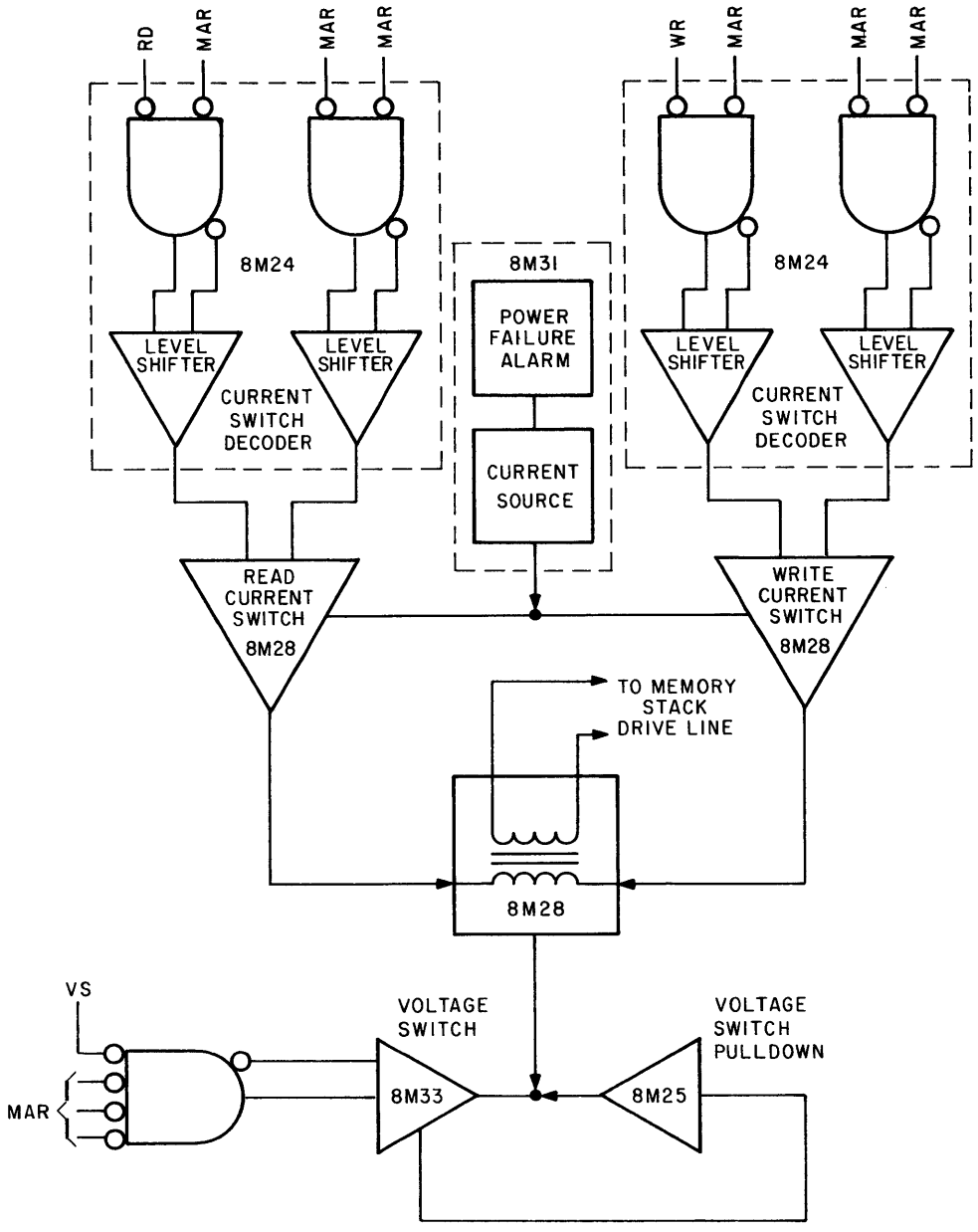

Figure 5-16. Drive System, Block Diagram

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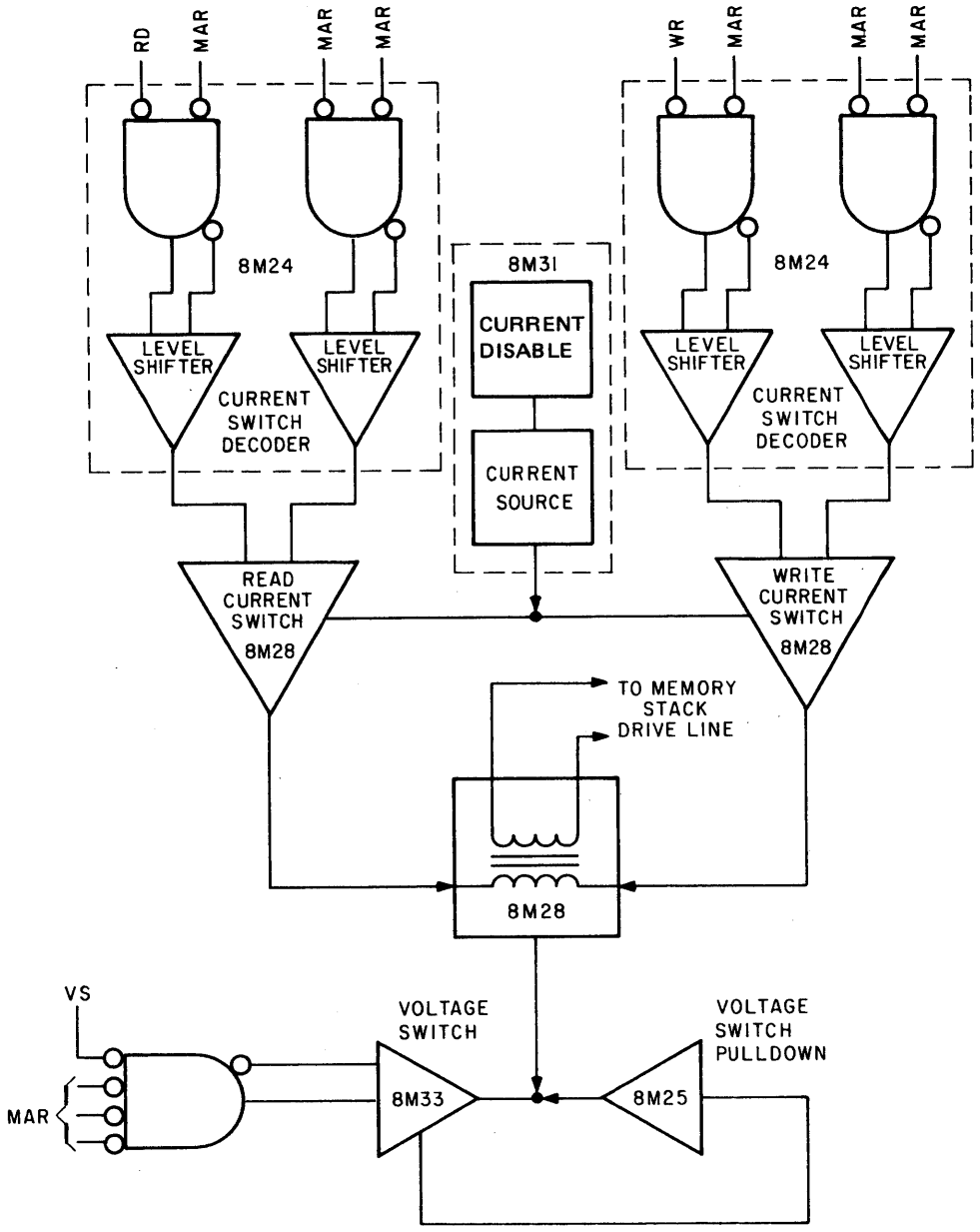


Figure 5-16. Drive System, Block Diagram

5.4.3.2 Drive System Matrix

The drive system consists of two matrices. The first matrix consists of the X and Y drive systems. The (128 x 128) matrix for the basic stack consists of the 128 X drive lines and 128 Y drive lines. (For the first half of the first bank there are 128 X drive lines and 136 Y drive lines.) Selection of the X and Y drive lines is obtained by the current switch and voltage switch matrix of each drive system. Figure 5-17 illustrates the X drive system matrix. The (16 x 8) matrix consists of the 16 voltage switches (VS00-VS07), (VS10-VS17) and the 8 read/write current switches, (CS00-CS07). To select drive line (000), requires the selection of VS00 and CS00. To determine the location of these two plug boards, refer to Tables 5-9 and 5-11.

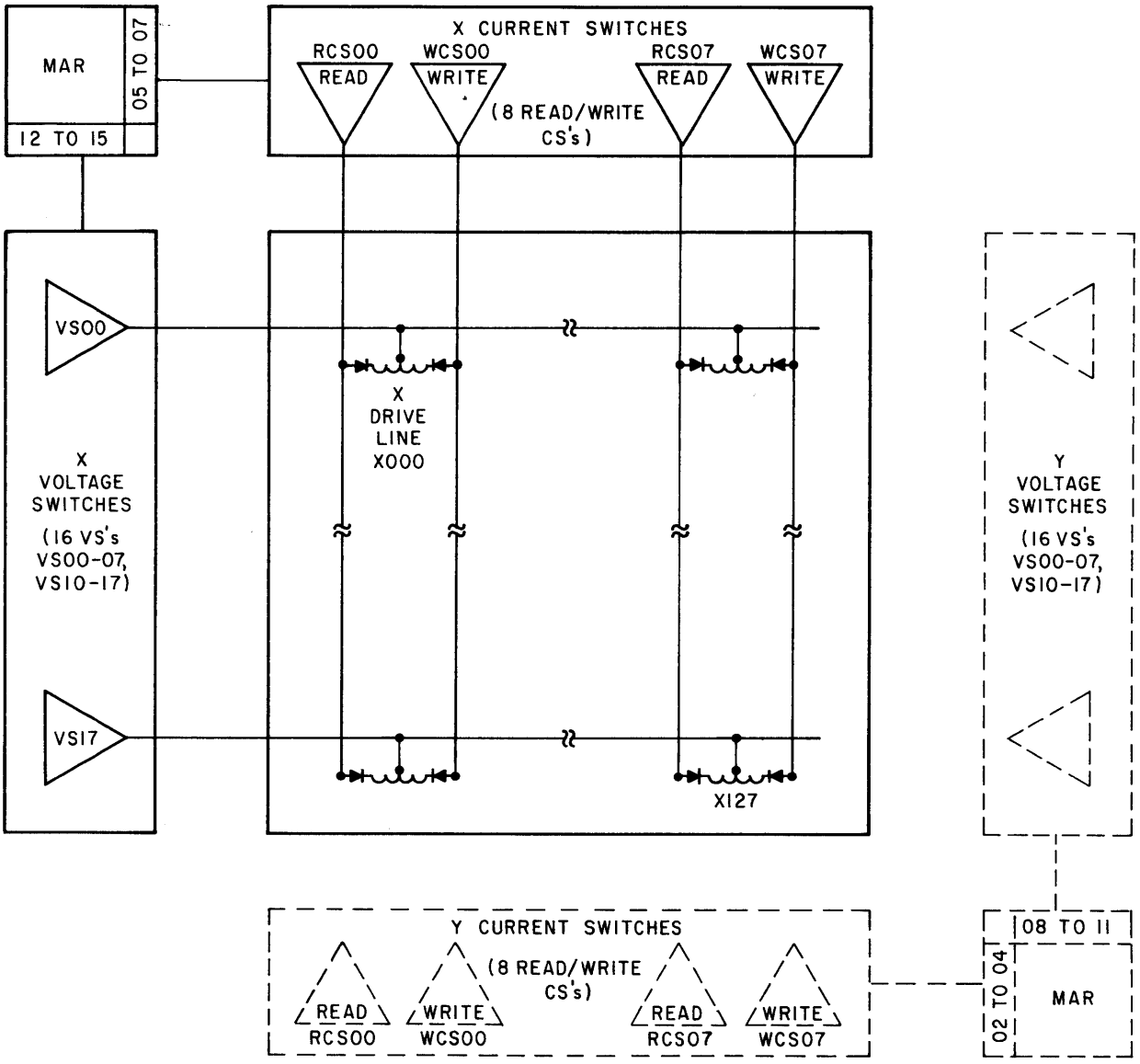


Figure 5-17. Drive System Matrix Diagram

The Y drive system matrix is indicated by the dotted lines in the matrix diagram. To find the location of the Y plug boards selected by the address bits see Tables 5-8 and 5-10.

5.4.3.3 Inhibit System

The inhibit system consists of the inhibit windings in the memory stack, cabling from the stack to the inhibit drivers (8M21 plug-ins), inhibit drivers and the inhibit driver decoders which control and generate the inhibit currents in the memory stacks. The inhibit drivers are controlled by the information stored in the data and address registers, and by the inhibit clock pulse. Information in the data register determines which data bits in the full word are to be zeros, information in the address register determines the area of the bit-plane which is selected for the inhibit current, and the inhibit clock pulse determines the time at which the inhibit current is selected.

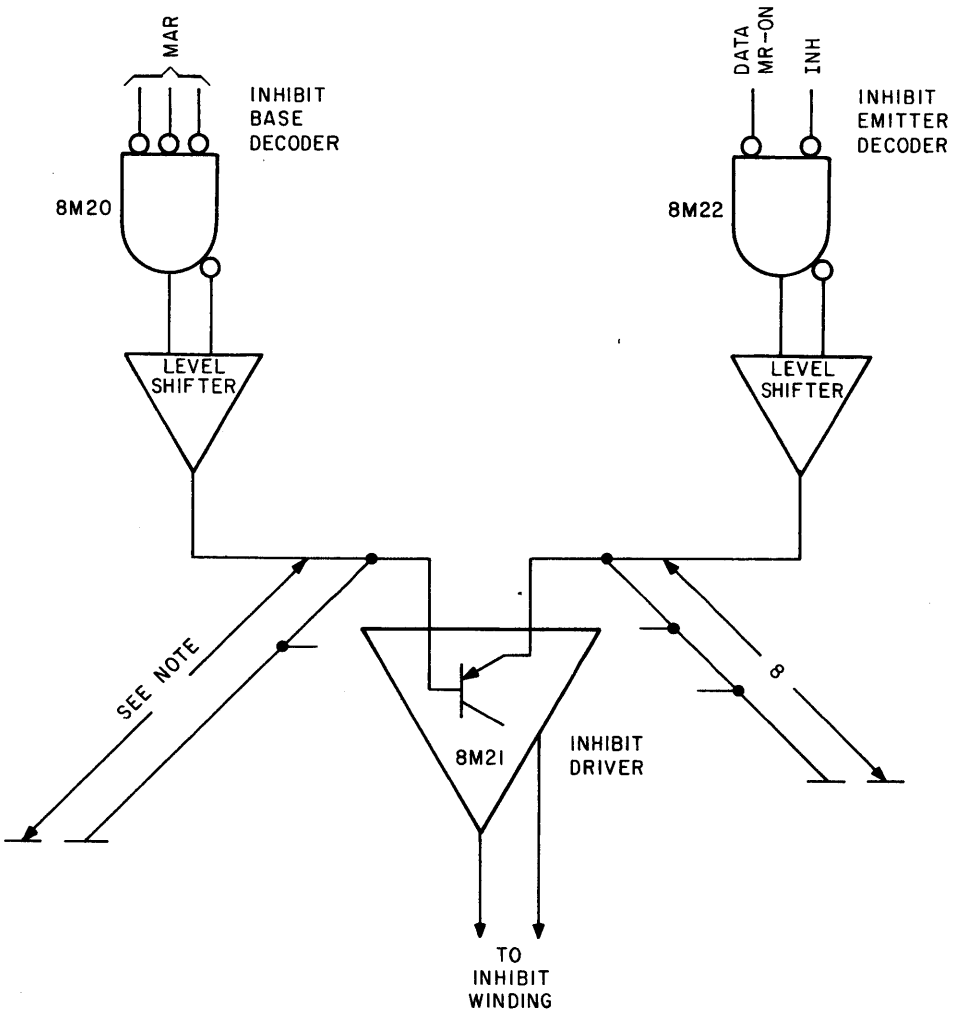
The inhibit system for a full word consists of two matrices: 8 x 17 and 8 x 16, see Figure 5-18. Both matrices are located on every inhibit platter. Each matrix has an independent inhibit clock pulse as shown in Figure 5-19. The inhibit base decoder drives 17 inhibit driver bases in the 8 x 17 matrix but only 16 inhibit driver bases in the 8 x 16 matrix. On the other hand, the inhibit emitter decoder drives eight inhibit driver emitters in both matrices. There are eight inhibit drivers per data bit and each data bit is contained in one bit-plane. A full word contains 17 + 16 or 33 bits for a total of 8 x 33 or 264 inhibit drivers (8 x 17 or 136 for one matrix and 8 x 16 or 128 for the other matrix).

See section 5.6 for a more detailed description and illustration of the inhibit windings in the stack and Tables 5-12 and 5-14 for decoding of the inhibit lines. Table 5-12 shows that each bit contains two 8M21 plug-ins; four inhibit circuits per 8M21.

5.4.3.4 Sense System

The sense system is comprised of the following: sense line windings in the memory stack, cabling from the stack to the sense preamplifier (8M32 plug-in), the sense preamplifier, sense amplifier, strobe gate and discriminator (which includes the marginal check voltage). Figure 5-14 shows how the sense preamplifiers are wired to reduce noise coupling into the sense system and to reduce the number of sense amplifiers required per system. There are four sense winding pairs per bit-plane making totals of four sense windings per half bank and eight sense windings per bank. See Section 5.6 for a more detailed description of the bit-plane and Tables 5-13 and 5-14 for decoding of the sense lines. Figure 5-20 shows a more detailed drawing of how the sense lines are connected to the sense preamplifiers (two 8M32 plug-ins per bit). A complete sensing system is contained in one memory bank.

A signal from the X-Y coincident core (per bit-plane) is present on one of the sense lines in the stack during both the read and the write sequences. The signal present during the read sequence represents information that had been stored in the core during a previous memory cycle. Whereas, the signal present during the write sequence represents information



NOTE: 17 FOR A "D" TYPE STACK INHIBIT DRIVE SYSTEM.
16 FOR A "C" TYPE STACK INHIBIT DRIVE SYSTEM.

Figure 5-18. Inhibit Drive System, Block Diagram

that is being stored into the core at the present write sequence. The strobe signal sent to the sense amplifiers enable a read-out to the memory data registers during a read sequence only.

5.4.3.5 Memory Address Decoding

Table 5-7 shows the complete decoding outline scheme of the main memory. A more detailed decoding breakdown is shown in the following tables:

Table 5-8. Y Current Switch Decoding
Table 5-9. X Current Switch Decoding
Table 5-10. Y Voltage Switch Decoding
Table 5-11. X Voltage Switch Decoding
Table 5-12. Inhibit Selection

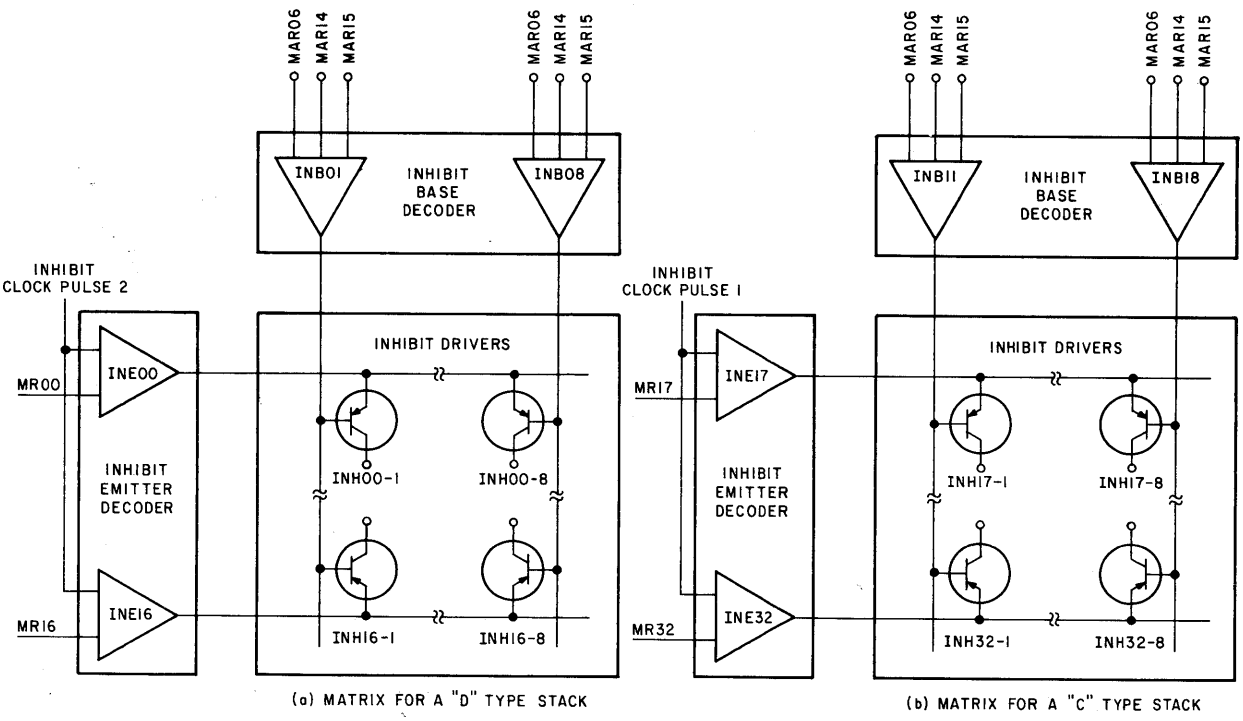


Figure 5-19. Inhibit System Matrix Diagram

Table 5-7. Memory Address Decoding

MAR Bits	Function
04, 03, 02	Y Current Switch Selection
05, 06, 07	X Current Switch Selection
11, 10, 09, 08	Y Voltage Switch Selection
15, 14, 13, 12	X Voltage Switch Selection
16	Half Bank Select
15, 14, 06	Inhibit Winding Selection
15, 14, 02, 04	Sense Winding Selection

The sense lines that are addressed can be determined by examining Table 5-13A. The location of the sense line pin numbers on a pair of sense amplifier plug-ins associated with a single data bit is shown in Table 5-13B.

R: 648 L: 656

Table 5-8. Y Current Switch Decoding

MAR Bits				Read/Write Plug-In Location	
04	03	02	R/WYD	MM1SL	MM1SR
0	0	0	0	3/6 BD	3/6 AN
0	0	1	1	3/6 BF	3/6 AL
0	1	0	2	3/6 BG	3/6 AK
0	1	1	3	3/6 BI	3/6 AI
1	0	0	4	3/6 BJ	3/6 AH
1	0	1	5	3/6 BK	3/6 AG
1	1	0	6	3/6 BM	3/6 AE
1	1	1	7	3/6 BN	3/6 AD

R: 646 L: 654

Table 5-9. X Current Switch Decoding

MAR Bits				Read/Write Plug-In Location	
07	06	05	R/WXD	MM1SL	MM1SR
0	0	0	0	9/12 BD	9/12 AN
0	0	1	4	9/12 BJ	9/12 AH
0	1	0	2	9/12 BG	9/12 AK
0	1	1	6	9/12 BM	9/12 AE
1	0	0	1	9/12 BF	9/12 AL
1	0	1	5	9/12 BK	9/12 AG
1	1	0	3	9/12 BI	9/12 AI
1	1	1	7	9/12 BN	9/12 AD

Table 5-10. Y Voltage Switch Decoding R: 648 L: 656

MAR Bits				OKTAL	Plug-In Location (PIN)	
11	10	09	08	VS	MM1SL	MM1SR
0	0	0	0	00	3AZ-103	3AR-103
0	0	0	1	01	3AZ-104	3AR-104
0	0	1	0	02	3AZ-119	3AR-119
0	0	1	1	03	3AZ-123	3AR-123
0	1	0	0	04	3BA-122	3AQ-122
0	1	0	1	05	3BA-121	3AQ-121
0	1	1	0	06	3BA-130	3AQ-130
0	1	1	1	07	3BA-123	3AQ-123
1	0	0	0	10	3AZ-203	3AR-203
1	0	0	1	11	3AZ-204	3AR-204
1	0	1	0	12	3AZ-219	3AR-219
1	0	1	1	13	3AZ-223	3AR-223
1	1	0	0	14	3BA-222	3AQ-222
1	1	0	1	15	3BA-221	3AQ-221
1	1	1	0	16	3BA-230	3AQ-230
1	1	1	1	17	3BA-223	3AQ-223

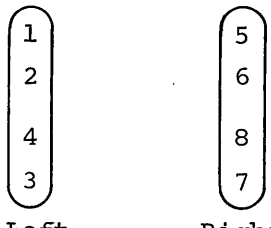
Table 5-11. X Voltage Switch Decoding R:646 L:654

MAR Bits				OKTAL	Plug-In Location (PIN)	
15	14	13	12	VS	MM1SL	MM1SR
0	0	0	0	00	9AZ-103	9AR-103
0	0	0	1	01	9AZ-104	9AR-104
0	0	1	0	02	9AZ-119	9AR-119
0	0	1	1	03	9AZ-123	9AR-123
0	1	0	0	04	9BA-122	9AQ-122
0	1	0	1	05	9BA-121	9AQ-121
0	1	1	0	06	9BA-130	9AQ-130
0	1	1	1	07	9BA-123	9AQ-123
1	0	0	0	10 8	9AZ-203	9AR-203
1	0	0	1	11 9	9AZ-204	9AR-204
1	0	1	0	12 A	9AZ-219	9AR-219
1	0	1	1	13 B	9AZ-223	9AR-223
1	1	0	0	14 C	9BA-222	9AQ-222
1	1	0	1	15 D	9BA-221	9AQ-221
1	1	1	0	16 E	9BA-230	9AQ-230
1	1	1	1	17 F	9BA-223	9AQ-223

Table 5-12. Inhibit Selection

MAR Bits			Inhibit Line	Pin No./PI Location
15	14	06		
0	0	0	1	5/Left
0	0	1	2	12/Left
0	1	0	3	36/Left
0	1	1	4	29/Left
1	0	0	5	5/Right
1	0	1	6	12/Right
1	1	0	7	36/Right
1	1	1	8	29/Right

Pair of 8M21's



The two blocks show the location of the pin numbers of the inhibit lines connected to a pair of inhibit drivers for a single bit, as viewed from the pin side of the platter.

Table 5-13A. Sense Line Decoding

MAR Bits 15	14	04	02	Sense Line
0	0	0	0	1
0	0	0	1	3
0	0	1	0	4
0	0	1	1	2
0	1	0	0	4
0	1	0	1	2
0	1	1	0	1
0	1	1	1	3
1	0	0	0	3
1	0	0	1	1
1	0	1	0	2
1	0	1	1	4
1	1	0	0	2
1	1	0	1	4
1	1	1	0	3
1	1	1	1	1

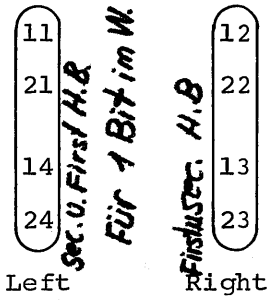
Durch Fädelung der Sense-Lines in einer Ebene bedingt

Table 5-13B. Sense Amplifier - Sense Line Designation

Half Bank No.	Sense Line No.	Pin No.	Plug-In
1	1	107,108	Left
1	2	107,108	Right
1	3	222,223	Right
1	4	222,223	Left
2	1	113,114	Left
2	2	113,114	Right
2	3	228,229	Right
2	4	228,229	Left

9BN 9BQ

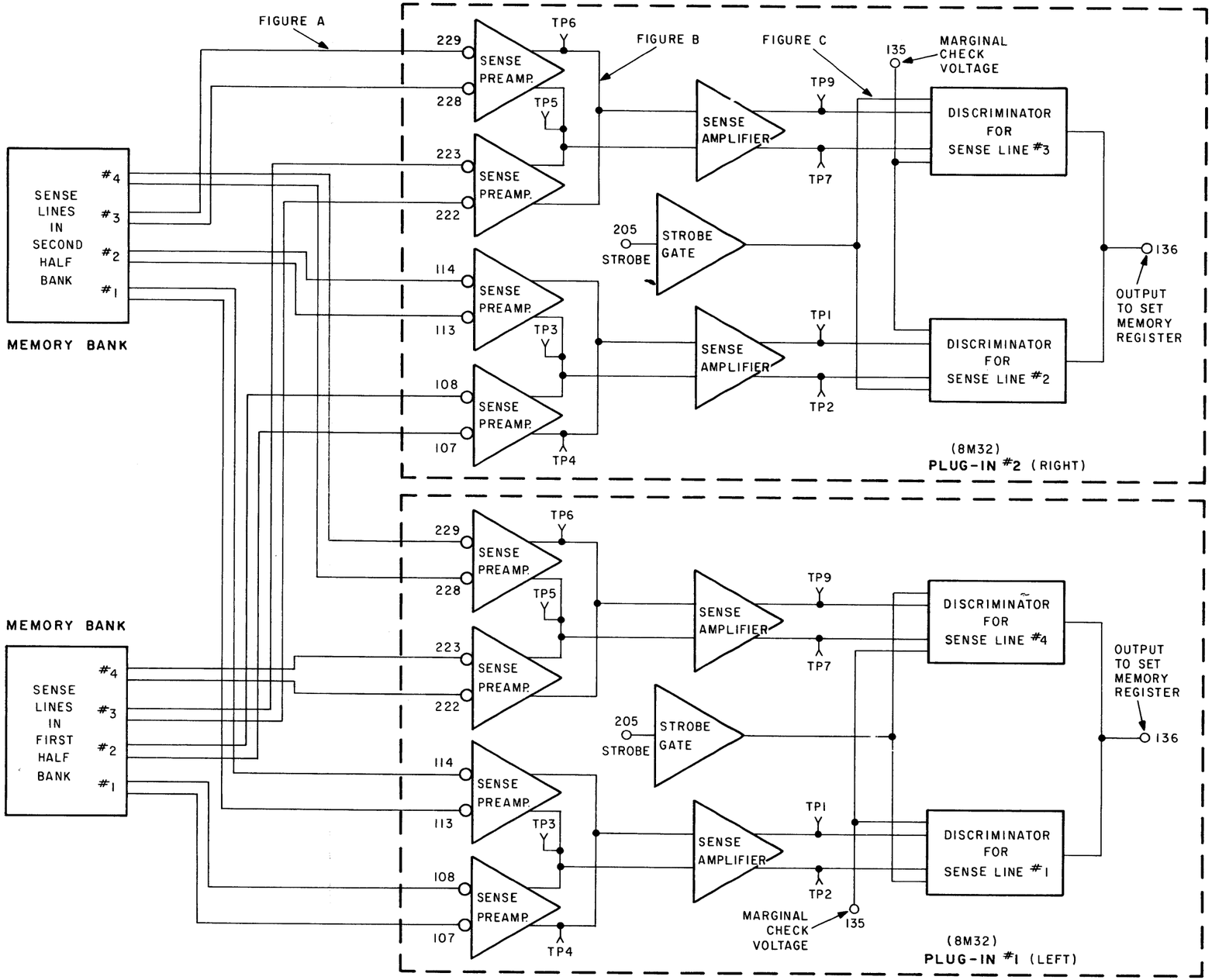
Pair of 8M32's

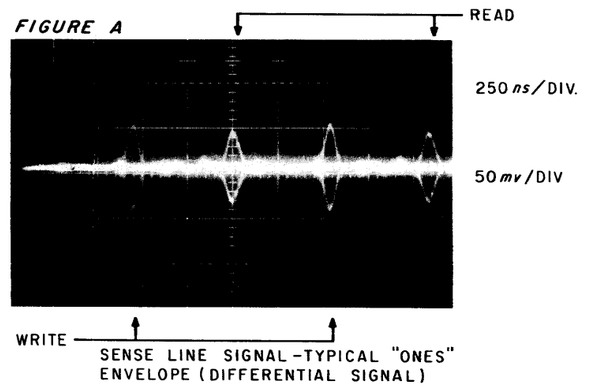


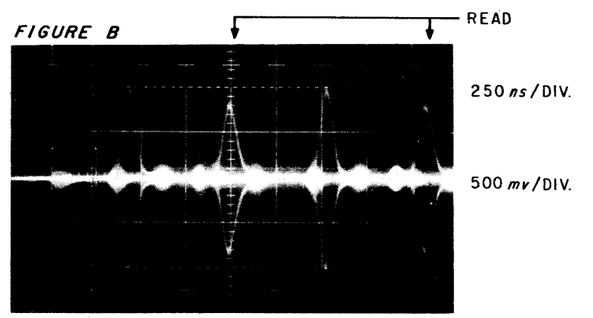
Sense Line Determination

Left
- 11 - First half-bank, sense line No. 1
- 12 - First half-bank, sense line No. 2
- 13 - First half-bank, sense line No. 3
- 14 - First half-bank, sense line No. 4
- 21 - Second half-bank, sense line No. 1
- 22 - Second half-bank, sense line No. 2
- 23 - Second half-bank, sense line No. 3
- 24 - Second half-bank, sense line No. 4

The two blocks show the locations of the pin numbers of the sense lines connected to a pair of sense amplifiers for a single bit, as viewed from the pin side of the platter.







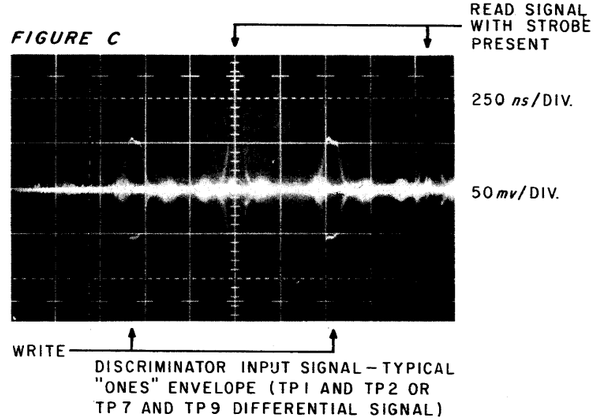


Figure 5-20. Sense Amplifier, Block Diagram

5.5 CIRCUIT DESCRIPTION

The main memory contains special circuits which are used in the following three memory sub-systems: Drive System, Inhibit System and the Sense System. The plug-in (circuit) breakdown of the three systems are listed below:

1. Drive System
    a. Current Switch Decoder, 8M24
    b. Current Switch, 8M28
    c. Voltage Switch, 8M33
    d. Voltage Switch Pull Down, 8M25
    e. Current Source, 8M31
2. Inhibit System
    a. Inhibit Base Decoder, 8M20
    b. Inhibit Emitter Decoder, 8M22
    c. Inhibit Driver, 8M21
3. Sense System
    a. Sense Amplifier, 8M32 (see Section 5.5.3)

5.5.1 DRIVE CIRCUITS

The Drive Circuits shown in Figures 5-21 and 5-22 are sub-divided into five board types.

5.5.1.1 Current Switch Decoder (8M24)

The Current Switch Decoder for the X or Y drive system is contained on one 8M24 plug-in. It consists of two sections which drive a matrix of transformer inputs to the current switches. Each section provides a one-of-four decode. Three address bits and the Read or Write command are decoded to yield a one-of-eight address decode for both Read and Write. The Read section consists of two ICP's (No. 1 on Figure 5-21) driving two level shifters. The level shifter (Q1 and Q2) converts the -.8V and -1.5V logic levels to -.3V and +10V respectively. In operation Q2 is normally conducting and Q1 is cut-off. When a gate "1" is selected, Q2 turns off and Q1 turns on. Q2's collector rises from -.3V to a level (less than +10V) determined by the current flowing through the collector resistor. This current is controlled by the impedance seen at the primary of the current switch transformer and the series resistance of the other side of the matrix. The voltage at the collector of Q2 rises to approximately +7 volts. The Write section of the decoder is identical to the Read section. The second section of the decoder consists of gates (No. 3 in Figure 5-21) and the associated

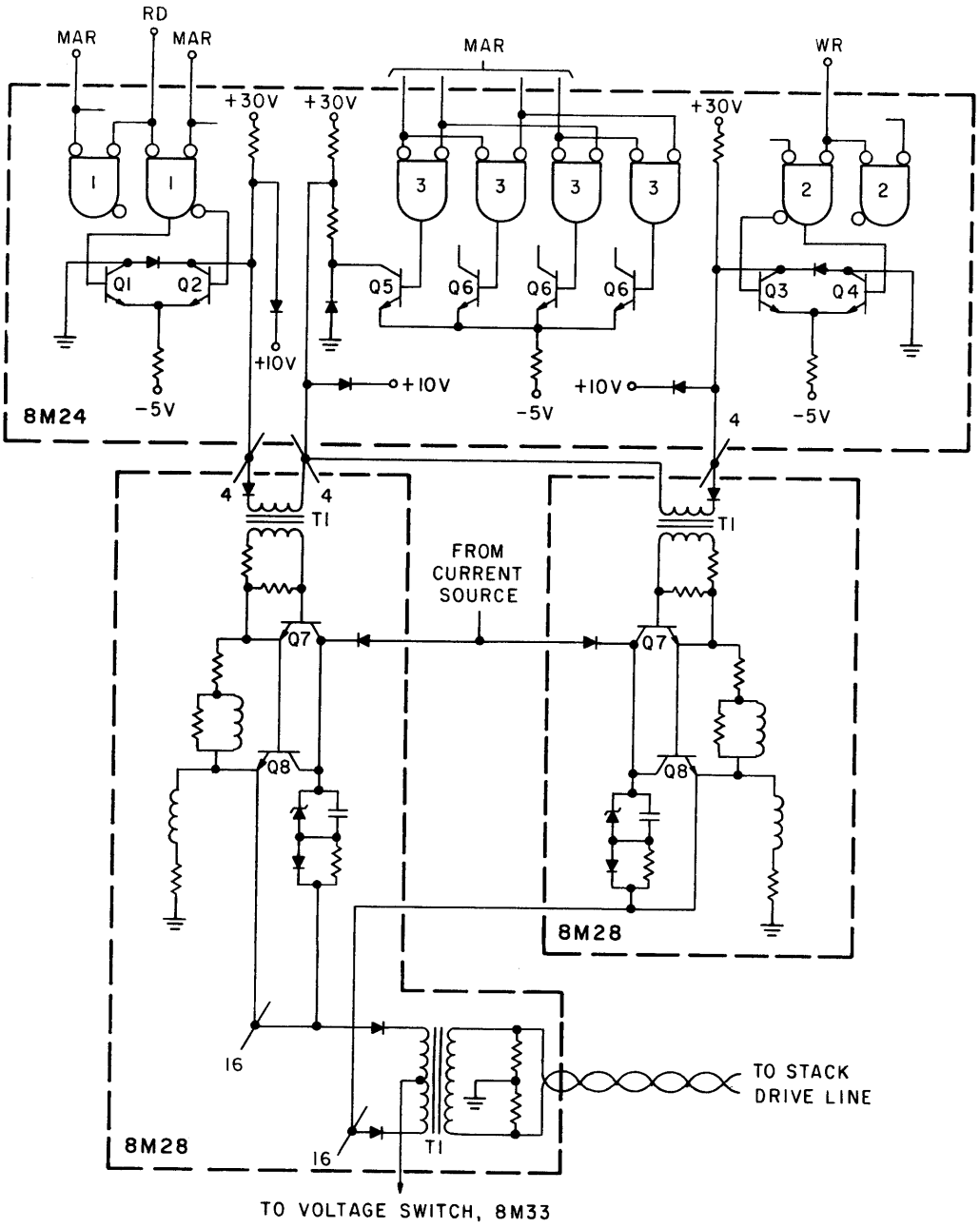


Figure 5-21. Current Switch and Current Switch Decoder, Simplified Schematic Diagram

level shifters (Q5, Q6). Single transistors are used in this level shifter because only one may be on at any given time. The output of Q5 is clamped to +10V, when not selected, to permit use of a low breakdown voltage transistor. The series resistor at the collector of Q5 is required to improve the recovery time of the switch input transformer.

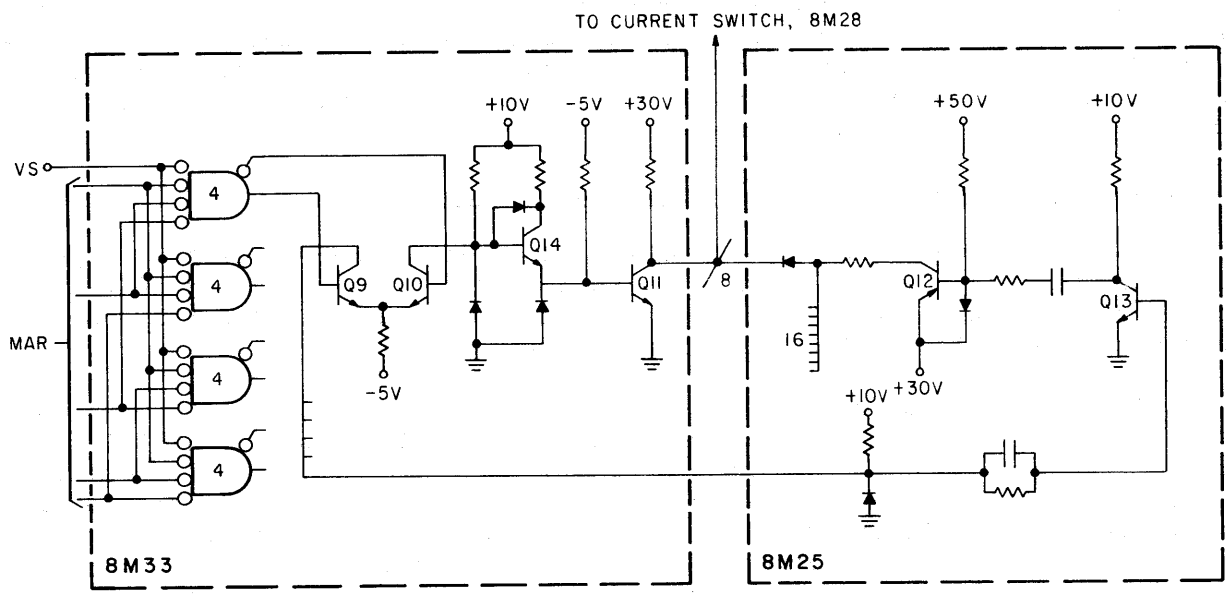


Figure 5-22. Voltage Switch and Voltage Pull-down, Simplified Schematic Diagram

5.5.1.2 Current Switch (8M28)

The Current Switch is composed of two transistors connected in a Darlington configuration with a transformer coupled input and output. One current switch and eight output transformers, with the required diodes and terminators, are mounted on an 8M28 plug-in. The collectors of the transistors (Q7, Q8 of Figure 5-21) are isolated from the current source by a series diode. The emitter of Q8 has an RL network to ground to increase the output current rise time. The network also provides a ground reference to back bias the output diode when the switch is not selected. The center tap of the primary of the output transformer is returned to one of the sixteen voltage switch outputs. The secondary of the output transformer is terminated in a line matching resistance, center-tapped to ground. Each Q8 emitter is diode coupled to sixteen output transformers. The drive system uses eight read current switches (and eight write current switches) to form an eight by sixteen output transformer matrix to select one of 128 drive lines. The output transformer is a 2:1 current reduction transformer.

5.5.1.3 Voltage Switch (8M33)

The Voltage Switch is used as a saturated switch. The output is normally at +30 volts and is at ground level when selected. The sixteen voltage switches of a drive system are contained on two 8M33 plug-ins. Sixteen gates of which only four are shown (No. 4 in Figure 5-22), decode three address bits and an address-gated Voltage Switch command. The level shifters (Q9, Q10) convert the logic level at the output of the selected decoder gate to the level and current required to saturate the output stage (Q11). The

collectors of all of the Q9's are connected to a common collector resistor. The signal generated at this common collector point is connected to the input of the Voltage Switch pull-down circuit. The voltage switch conducts read and write currents while in the saturated state. After the write current decays to zero milliamperes, the voltage switch is turned off; the collector of the voltage switch returns to +30 volts with the aid of the pull-down circuit.

5.5.1.4 Voltage Switch Pull-down/Voltage Switch (8M25)

The 8M25 plug-in contains a pull-down circuit (8M25-7) or both a pull-down circuit and a voltage switch circuit (8M25-5). The voltage switch circuit is identical to the circuits on the 8M33 plug-in. The pull-down circuit is described below. See Figure 5-22.

The Pull-down circuit returns the voltage switch bus to +30V when the selected switch is turned off. The output of the first stage (Q13) is capacitively coupled to the input of the second stage (Q12). The coupling time constant has been selected so that the voltage at the collector of Q11 is returned to at least +28.0 volts approximately 53 ns after the voltage at the collector of Q9 reaches +3.0 volts. The voltage bus capacitance is recharged to +30V, before the next voltage switch is turned on so that all the drive current is directed to a single drive line. The output of Q12 is diode coupled to all sixteen voltage switch buses. This circuit is mounted on an 8M25 plug-in.

5.5.1.5 Current Source (8M31)

The current source provides both read and write currents. Two current sources are used to drive one memory stack, one for the X drive system and one for the Y drive system. See the schematic diagram, Figure 5-23.

There are three sections to the current source: a current disable section, a voltage regulator section and a current control section. The current disable section consists of Q14 and K1. Whenever the PFA (power failure alarm) signal is five volts or higher, Q14 turns on and energizes K1. A forward bias is then transferred to the bases of transistors Q1 through Q10, enabling the current source. Precision resistors in the emitters of the ten output transistors provide controlled sharing of the output current among the transistors. The voltage regulator section consists primarily of the Zener diodes CR1, CR2, and CR3 and the resistor R13. A predetermined voltage is impressed on the base of Q11, thereby fixing the emitter potential which is used as the bias for the current source transistors Q1 through Q10. The current control section consists of resistors R14, R25, R27 and R30. There is a possibility that not all resistors will be used, depending on the resistor tolerances.

During the quiescent state of the memory (no current switches are turned on), the total output current of the current source is directed through the two parallel one ohm resistors to +30V. None of the transistors supplying current to the output terminal is saturated; therefore, the current through the two parallel one ohm resistors (0.5 ohms) is the total current that the current source will supply. An accurate voltage measurement

collectors of all of the Q9's are connected to a common collector resistor. The signal generated at this common collector point is connected to the input of the Voltage Switch pull-down circuit. The voltage switch conducts read and write currents while in the saturated state. After the write current decays to zero milliamperes, the voltage switch is turned off; the collector of the voltage switch returns to +30 volts with the aid of the pull-down circuit.

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5.5.1.5 Current Source (8M31)

The current source provides both read and write currents. Two current sources are used to drive one memory stack, one for the X drive system and one for the Y drive system. See the schematic diagram, Figure 5-23.

There are three sections to the current source: a current disable section, a voltage regulator section and a current control section. The current disable section consists of Q14 and the MAD1 circuit assembly. Whenever the EN-P signal is five volts or higher, Q14 turns on and grounds R13. A forward bias is then transferred to the bases of transistors Q1 through Q10, enabling the current source. Precision resistors in the emitters of the ten output transistors provide controlled sharing of the output current among the transistors. The voltage regulator section consists primarily of the Zener diodes CR1, CR2, and CR3 and the resistor R13. A predetermined voltage is impressed on the base of Q11, thereby fixing the emitter potential which is used as the bias for the current source transistors Q1 through Q10. The current control section consists of resistors R14, R25, and R27. There is a possibility that not all resistors will be used, depending on the resistor tolerances.

During the quiescent state of the memory (no current switches are turned on), the total output current of the current source is directed through the two parallel one ohm resistors to +30V. None of the transistors supplying current to the output terminal is saturated; therefore, the current through the two parallel one ohm resistors (0.5 ohms) is the total current that the current source will supply. An accurate voltage measurement

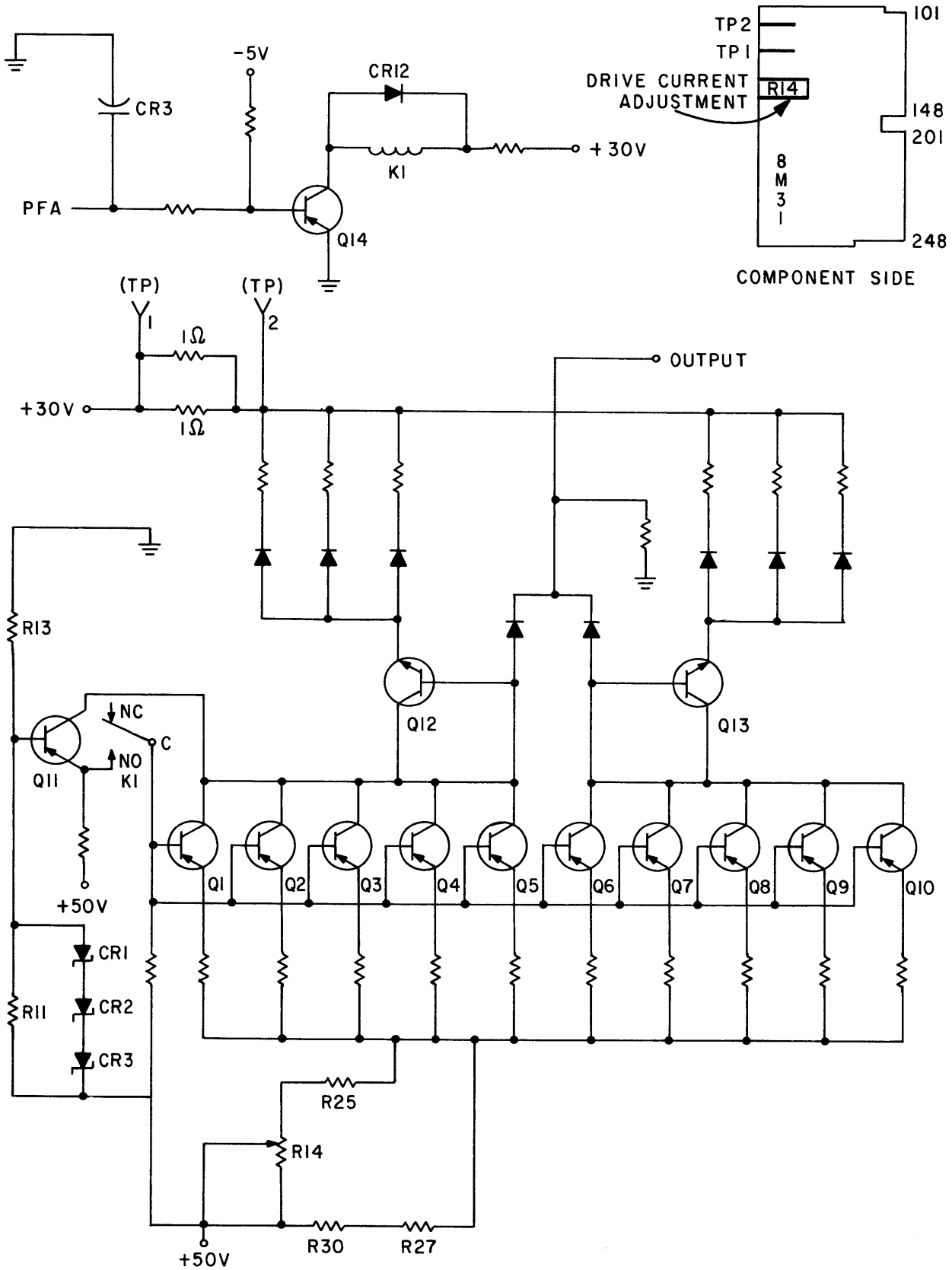


Figure 5-23. Current Source, Simplified Schematic Diagram

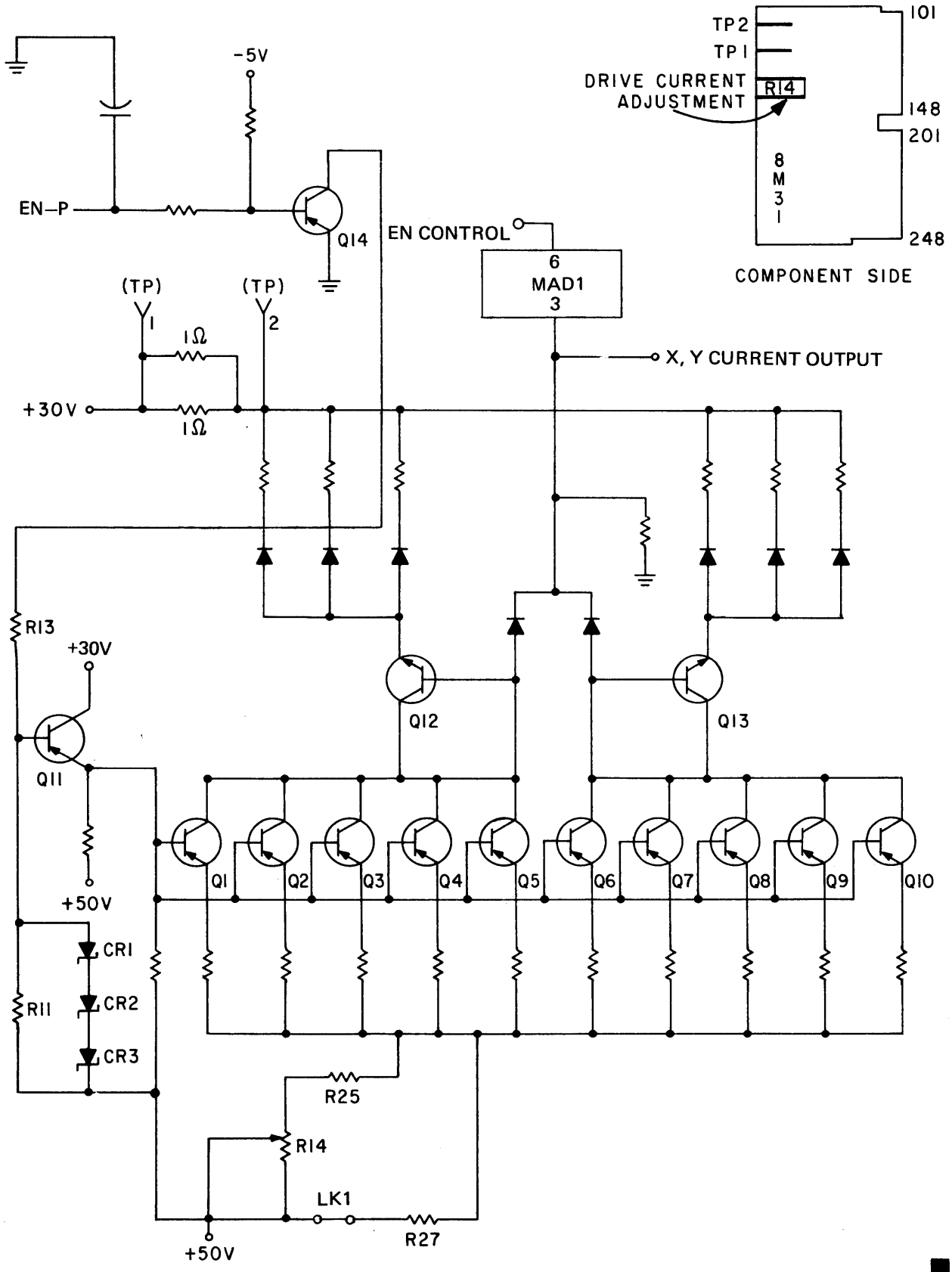


Figure 5-23. Current Source, Simplified Schematic Diagram

of the potential across the one ohm resistors during the quiescent state of the current source provides a good current measurement -- i.e., a 0.560 volt measurement is actually a (.560/0.5) = 1.120 amp. current measurement.

5.5.2 INHIBIT CIRCUITS

There are three basic circuits used in the Inhibit system: the Inhibit Base Decoders, the Inhibit Emitter Decoders and the Inhibit Drivers. There are eight inhibit drivers for each bit-plane in the core stack. The Inhibit Base Decoder selects one of the eight drivers for each bit while the Inhibit Emitter Decoder provides data control and timing. (Figure 5-24.)

5.5.2.1 Inhibit Base Decoder (8M20)

The Inhibit Base Decoders are located on the 8M20 plug-ins. The outputs of the gates (designated as "1" in Figure 5-24) control the level shifting differential stage (Q1, Q2). When the NOR output of the selected gate goes positive, Q1 turns on and Q2 turns off. The collector voltage of Q1 falls from a quiescent level of +2.5V to -.3V. (the drop across the clamp diode). The +2.5V level is established by the voltage divider in the collector circuit of Q1. The emitter follower (Q3) provides the power to drive the 16 or 17 output stages connected to it. (See Notes of Figure 5-24.) The output of Q3 is +3.5V when quiescent, and +1.25V when selected.

5.5.2.2 Inhibit Emitter Decoder (8M22)

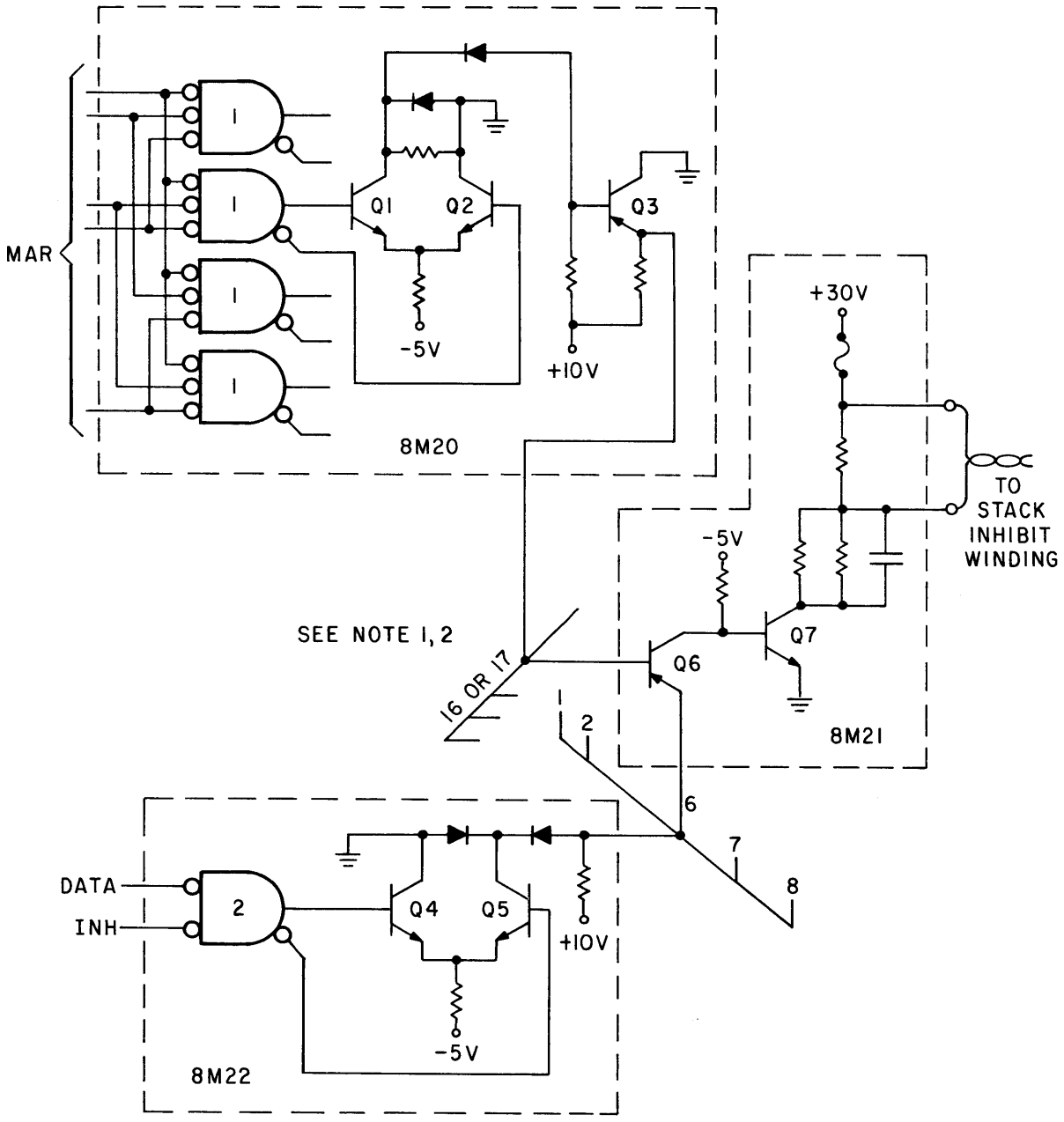
The Inhibit Emitter Decoder consists of a logic gate followed by a level shifter. Six of these circuits are mounted on one 8M22 plug-in. The gate designated as "2" (Figure 5-24) is enabled by a zero in the MR and is turned on by the INH command. The INH command previously gated with the Half-Bank control bit (MAR 16), provides the timing for the Inhibit current. Q5, which is normally on, is turned off by the OR output of gate "2". This permits the voltage at the collector of Q5 to rise toward +10V. The collector resistor then provides the emitter current for the selected driver input transistor. The emitter current limits the excursion at the collector of Q5 to +2.5V (controlled by the level set by the selected inhibit base decoder output). When Q5 is ON the output voltage is +.5V (more negative than the lowest inhibit base decoder output level) to ensure that the output stage does not turn on.

5.5.2.3 Inhibit Driver (8M21)

The Inhibit Driver consists of an input transistor and the output stage. Four drivers are mounted on one 8M21 plug-in. The input transistor (Q6) is operated in an unsaturated mode to reduce turn off time. The output stage (Q7) is saturated when Q6 turns on. The collector circuit of Q7 includes a line terminating resistor, current limiter, and a matching capacitor.

5.5.3 SENSE AMPLIFIER CIRCUIT (8M32)

The sense amplifier circuits consist of a pre-amplifier, a second stage, a threshold stage, a strobe, and an output stage. The 8M32-2 contains the circuitry for four sense amplifiers. Figure 5-25 is a simplified schematic illustrating all the essential circuits of one sense amplifier.



NOTE: (1) 16 LINES FOR INHIBIT SELECTION WHERE A "C" TYPE OR 16 PLANE MEMORY STACK IS BEING DECODED.

(2) 17 LINES FOR INHIBIT SELECTION WHERE A "D" TYPE OR 17 PLANE MEMORY STACK IS BEING DECODED.

Figure 5-24. Inhibit System, Simplified Schematic Diagram

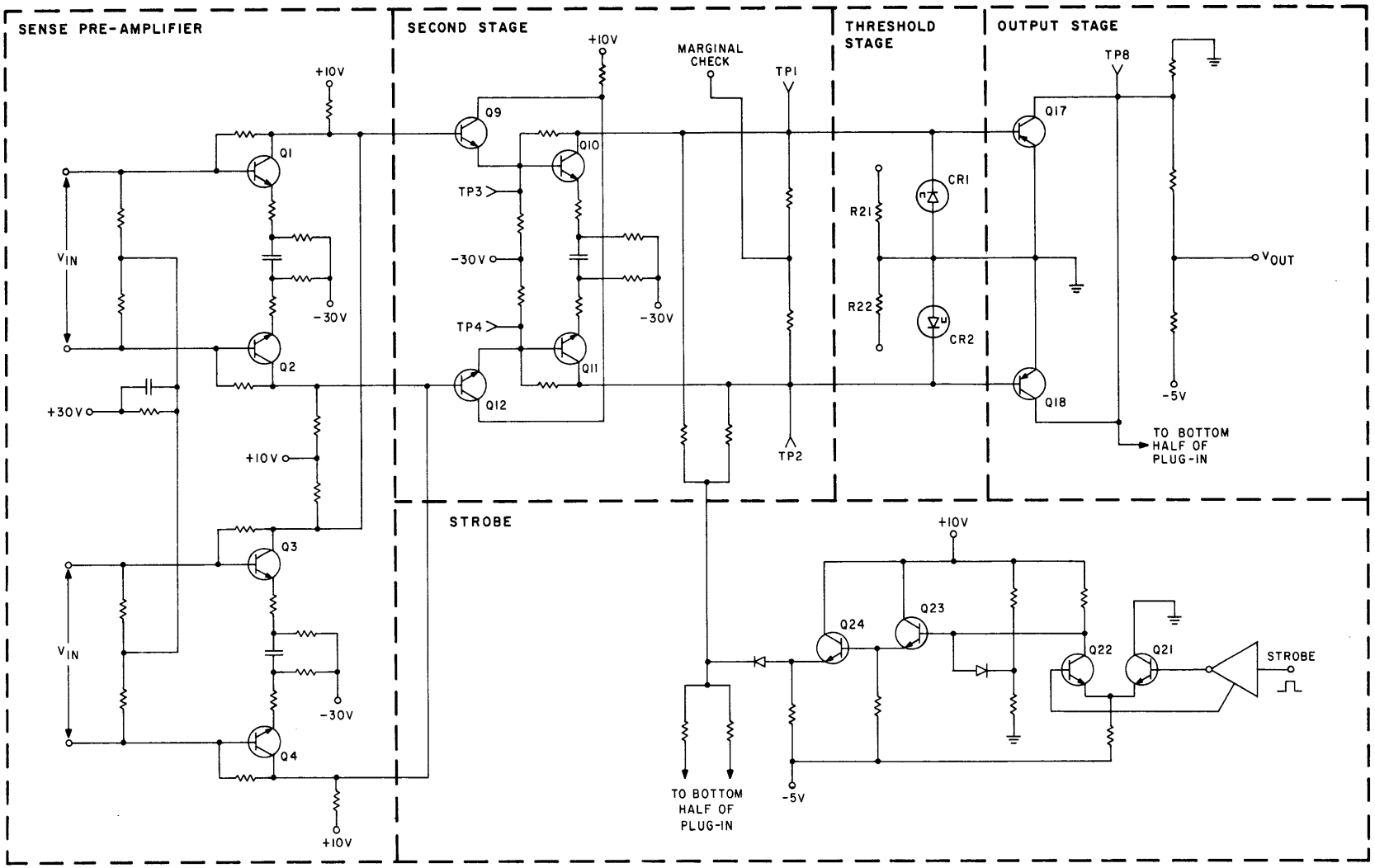


Figure 5-25. Sense Amplifier, Simplified Schematic Diagram

5.5.3.1 Sense Pre-Amplifier

The two transistors Q1 and Q2 are always ON. A difference voltage at the input produces two equal but opposite polarity signals at the two collector outputs. Both signals are transferred to the second stage. The signal at the collector of Q1 is transferred to the base of Q9; the signal from Q2 is transferred to the base of Q12.

5.5.3.2 Second Stage

The incoming signal is inverted and transferred to the threshold stage. The inverted signal at the collector of Q10 is transferred to the anode of the tunnel diode, CR1; the inverted signal at the collector of Q11 is transferred to the tunnel diode, CR2.

5.5.3.3 Threshold Stage

The threshold stage differentiates between input signals of 25mV and 12mV. The variable bias of the marginal check voltage allows the varying of the threshold level.

The threshold stage illustrated contains two separate circuits containing the two tunnel diodes, CR1 and CR2. Depending upon the polarity of the incoming signal, and the presence of a strobe, one of the two tunnel diodes is switched and transfers the signal to the output stage.

The internal resistance of a tunnel diode is very low when conducting a current of less than 2.2mA. However, the internal resistance increases tenfold, when the conducted current increases to more than 2.2mA. The transition from low to high resistance is practically instantaneous and causes the corresponding voltage across the diode to increase proportionately. The current through the tunnel diode depends on five variables:

1. the signal current
2. the fixed bias current
3. the variable bias current
4. the strobe current
5. the steady current to the second stage

The variable bias current is dependent on the marginal checking voltage. When the strobe and the two bias currents together equal the current drawn by the second stage, no current flows through the tunnel diode. Even if a signal current corresponding to a 25mV signal is present, current through the tunnel diode will be less than the 2.2mA required for switching. When a 25mV signal is present and when the strobe current falls to zero (during the strobing period), the second stage draws sufficient current through the tunnel diode to exceed the 2.2mA limit or threshold level. When the 2.2mA level is exceeded, the tunnel diode "switches".

5.5.3.4 Output Stage

Normally the output is at the low logic level (-1.6V). When there is an output, this level goes to the high logic level (-0.8V). The voltage at the base of transistors Q17 and Q18 is normally -0.05V. This voltage is not sufficient to make the transistors conduct; and as a result the output is low (-1.6V).

When either tunnel diode CR1 or CR2 switches, the base voltage increases to -0.5V because of the large and sudden voltage change across the tunnel diode. When CR1 or CR2 switches, the associated transistor Q17 or Q18 turns on and the output goes high (to -0.8V).

5.5.3.5 Strobe

Normally, transistor Q22 is OFF. The collector of Q22 is high and current flows via Q23, Q24, and CR6 to the tunnel diodes. This prevents switching of the tunnel diode. When a strobe timing pulse is present in pin 205, a positive signal is applied to the base of Q22. The emitter voltage of Q21 is lowered and reverse biases CR6. This action results in removing the strobe current and allowing the tunnel diode to switch if a sufficiently large signal is present.

5.5.3.6 Test Points

The following test points on the 8M32 plug-in are used to check the operation of the sense amplifier:

1. Test points TP3, TP4, TP5 and TP6 are connected to the outputs of the four preamplifiers. The signal measured at these points should be amplified approximately ten times.

2. Test points TP1, TP2, TP7 and TP9 are connected to the inputs of the four threshold stages. Both the signal and the strobe pulse can be observed at these points.

3. Test point TP8 is connected to the output of the sense amplifier. The output pulse observed at this point is before it is shifted to its nominal level.

5.6 MEMORY STACK

5.6.1 GENERAL

The stacks ("C" and "D" types) consist of 16 (type C) or 17 (type D) matted memory planes mounted on insulated boards for support. See Figure 5-26. Each mat consists of 16 sub-mats: eight sub-mats contain 1,024 cores (32 x 32) and eight sub-mats contain 1,152 cores (32 x 36). See Figure 5-27.

5.6.2 CORE WIRING

Each core of a plane is threaded by four wires: one X, one Y, one sense and one inhibit wire. See Figure 5-28. The cores are spaced on nominal 0.025 inch centers. The inhibit wires thread the cores in a parallel direction to the X-wires and in a perpendicular direction to the Y-wires.

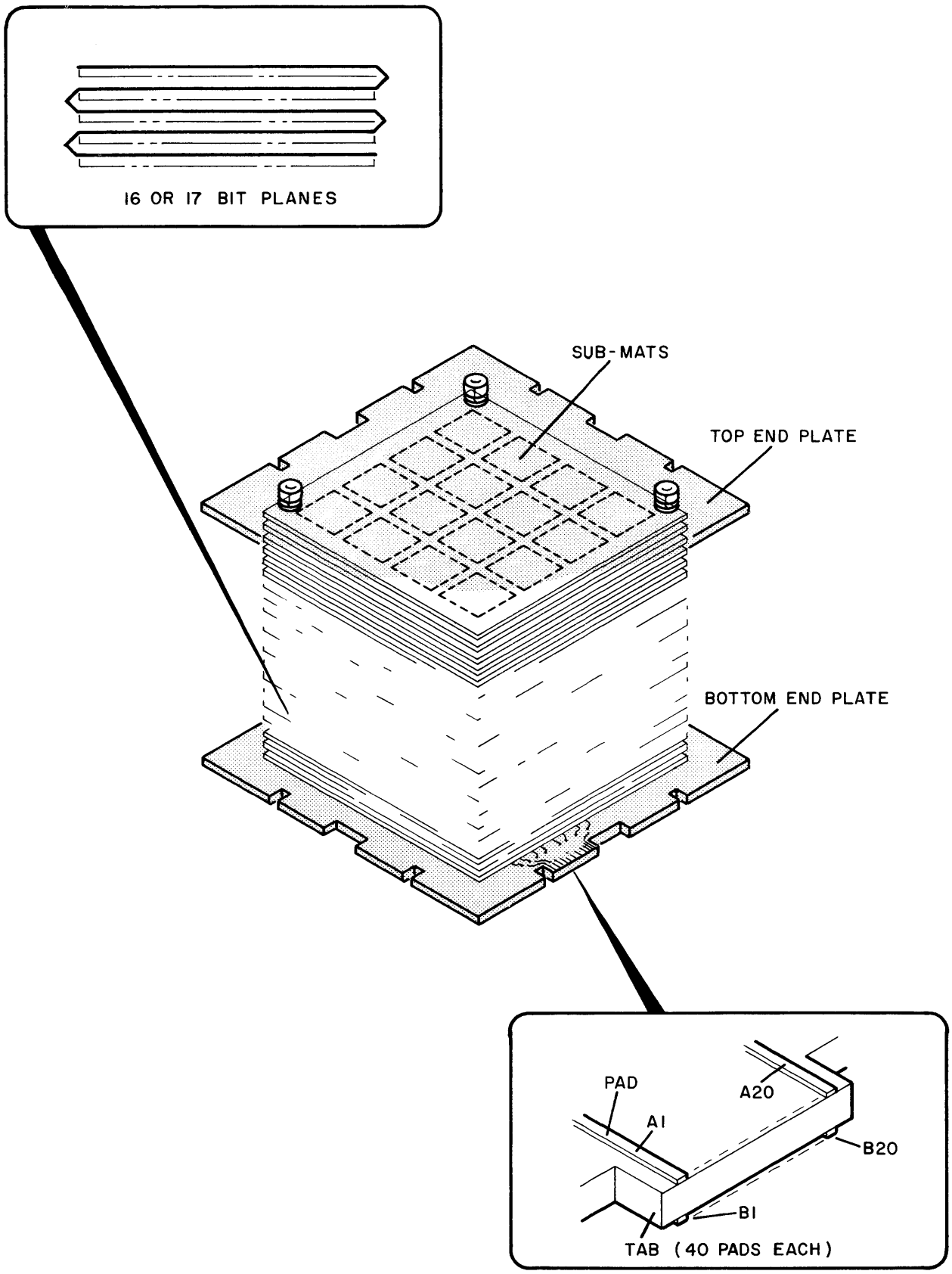


Figure 5-26. 70/55 Main Memory Stack

The sense lines thread the cores in a "bow-tie" configuration and run parallel to the direction of the Y-wires. The pairs of sense wires are transposed at the middle and ends of every sub-mat. The number of X, Y, inhibit and sense windings on each bit-plane are as follows: 128 X-windings each thread 136 cores; 136 Y-windings each thread 128 cores; and 8 inhibit windings each thread 2,176 cores. Each inhibit winding threads 1,088 cores within the top eight or bottom eight rows of each sub-mat. The 4 sense windings each thread 4,352 cores of a bit-plane. Four sub-mats from different mat-rows and mat-columns form a sense winding.

5.6.3 WIRING TERMINATION

The X-lines are connected to short printed strips located close to the two vertical edges of the insulated board. A printed "through" hole on this printed strip is used to form two serial connections of two adjacent planes. Serial connections are made by direct soldering of the line terminating pin. The interconnection of the Y-lines on every plane is done in the same manner as the X-lines. Two sense windings are terminated on the middle of the one vertical edge of the board. The other two sense windings are terminated on the opposite vertical edge of the board. The eight inhibit windings are terminated at the four corners of the board; two inhibit windings are terminated at each corner of the board.

5.6.4 DRIVE LINE CONNECTORS

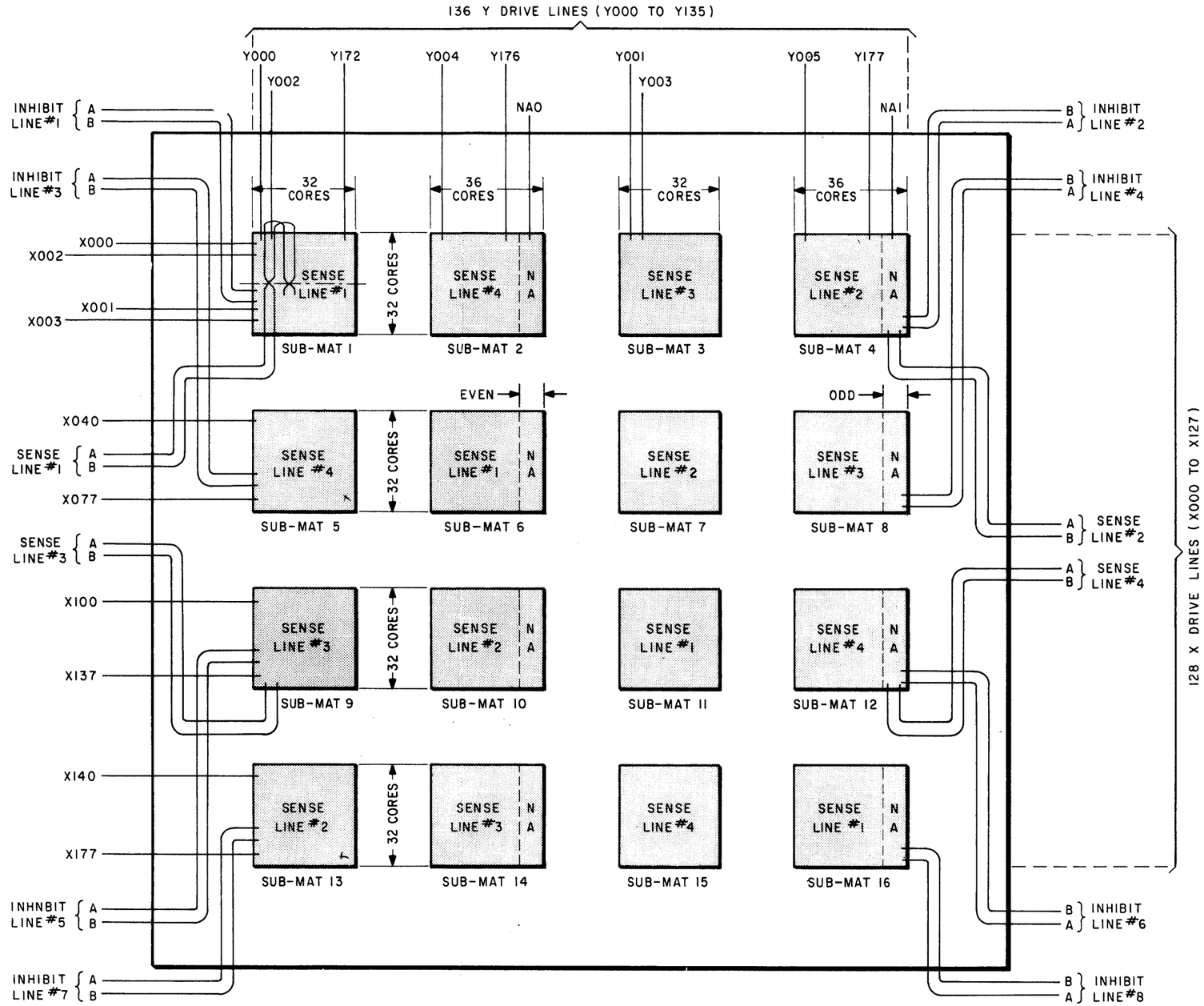
An end plate is used on the top and bottom sides of the stack. Printed circuit strips or pads are located on the rim of the upper and lower end plates and all X and Y lines are terminated on these pads. Edge connectors or tabs are used to bring X and Y lines to the corresponding pins located at the back of the platter. The edge connectors or tabs are designated J7 through J22. Each tab has 40 pads, 20 on the top (or A) side and 20 on the bottom (or B) side. Facing any tab (looking toward the center of the stack) the pads are numbered 1 through 20. If it is necessary to refer to a specific drive line, list both the connector (tab) and the pad numbers, e.g. J13-B5, J8-A19, etc. (See Figure 5-29.)

5.6.5 INHIBIT AND SENSE WINDING CONNECTORS

The pin numbers for the inhibit winding and sense winding connectors are illustrated in Figure 5-29. The locations of the 75-pin sense winding connectors, J5 and J6 and the 75-pin inhibit winding connectors, J1 through J4 are illustrated in Figure 5-30. This illustration shows a stack mounted on a MM1SR platter.

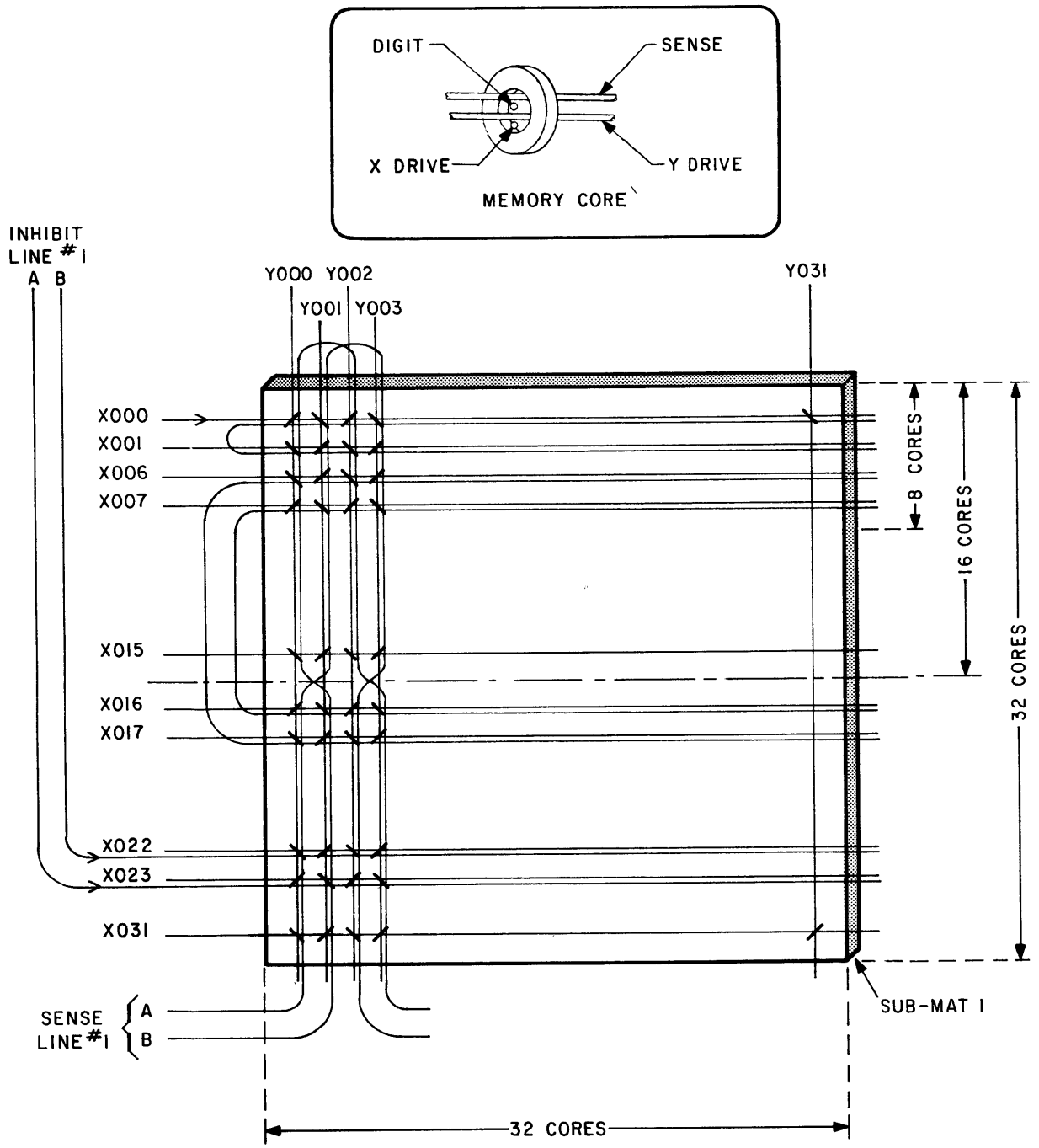
5.6.6 DRIVE LINE SELECTION

Tables 5-14 and 5-15 relate the sequential X and Y drive lines to the corresponding sequential address decoding code. For example, if sequential Y007 line, (the eighth Y address line from the left side of the stack) is addressed, the sequential address decoding code is 032 (Y voltage switch 03 and Y current switch 2). In the X decoding system, if sequential X line, X007 (the eighth X address line from the top) is addressed, the sequential address decoding code is 034 (X voltage switch is 03 but the X current switch must be decoded with the use of Table 5-9).



NOTE: REFERENCE NUMBERS OF X AND Y DRIVE LINES ARE SEQUENTIAL ADDRESS DECODING NUMBERS.

Figure 5-27. 70/55 Main Memory Plane



NOTE: THE X AND Y NUMBERS REPRESENT THE SEQUENTIAL NUMBERS OF THE DRIVE LINES.

Figure 5-28. Typical Sub-Mat of 70/55 Memory Plane

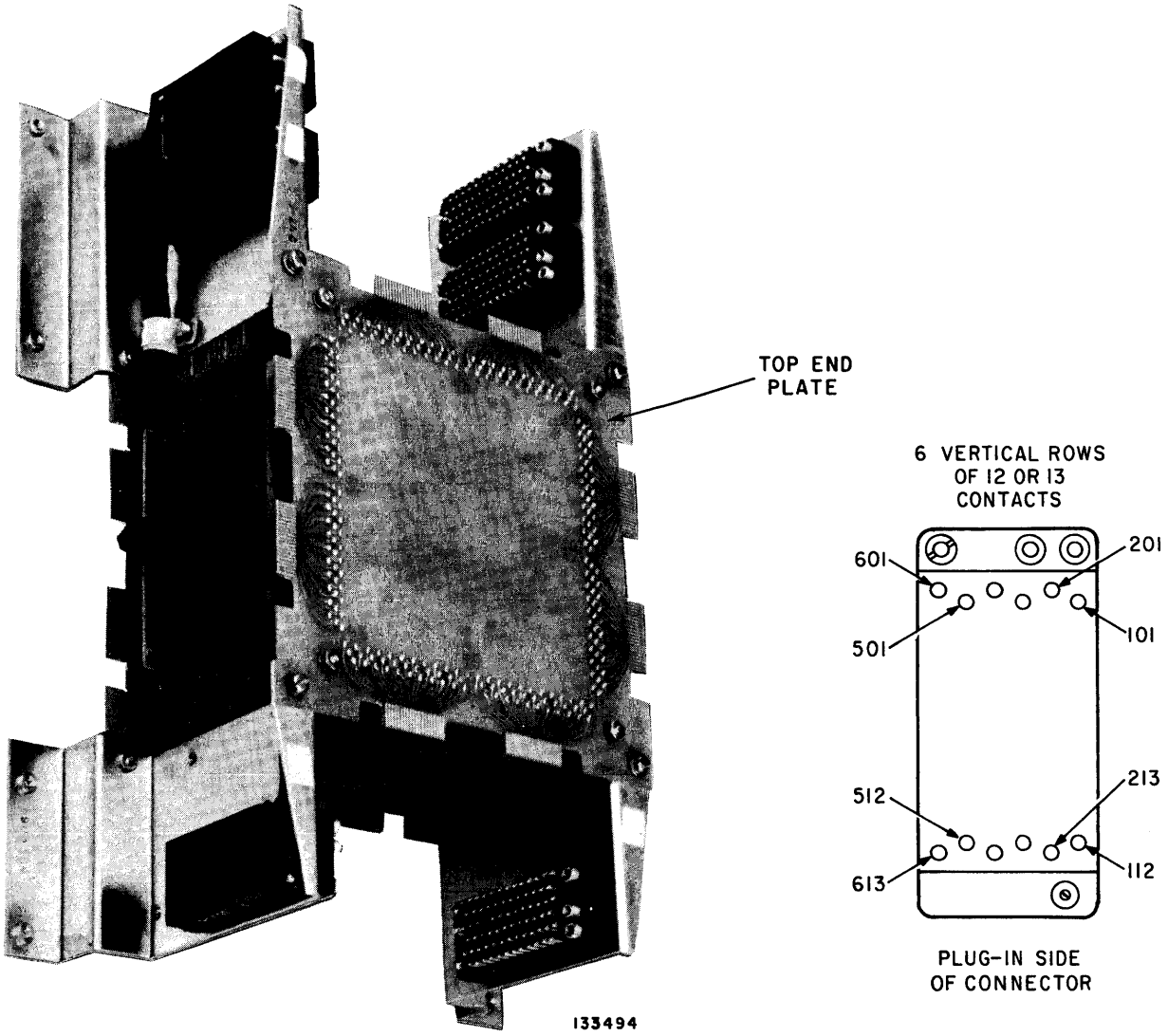


Figure 5-29. 70/55 Main Memory Stack and Mounting Hardware

Addressing of the stack drive lines are staggered as indicated by the sequential address decoding numbers of Table 5-15. In the X system, the first line addressed is X000, the second line addressed is sequential address decoding line X001 or the 17th X drive line, the third line addressed is sequential address decoding line X002 or the 9th X drive line, etc. See Table 5-15 for the Y selections. Because of the staggered addressing of the drive lines, the first sequential X drive line current enters the stack at J21 and leaves at J22 (Figure 5-30); for the second X drive line, the current enters the stack at J11 and leaves at J12, etc. The voltage excursion of the drive lines as a result of the drive currents can be measured at the end plates of the stack; the voltage waveform is very similar to Figure 5-56 except for the X system the first pulse is approximately 75 nanoseconds minimum. Sequential X drive line X000 can be measured at the upper left side of the stack (J21), X drive line X001 can be measured at the upper right side of the stack (J11), X drive line X002 can be measured at the upper left

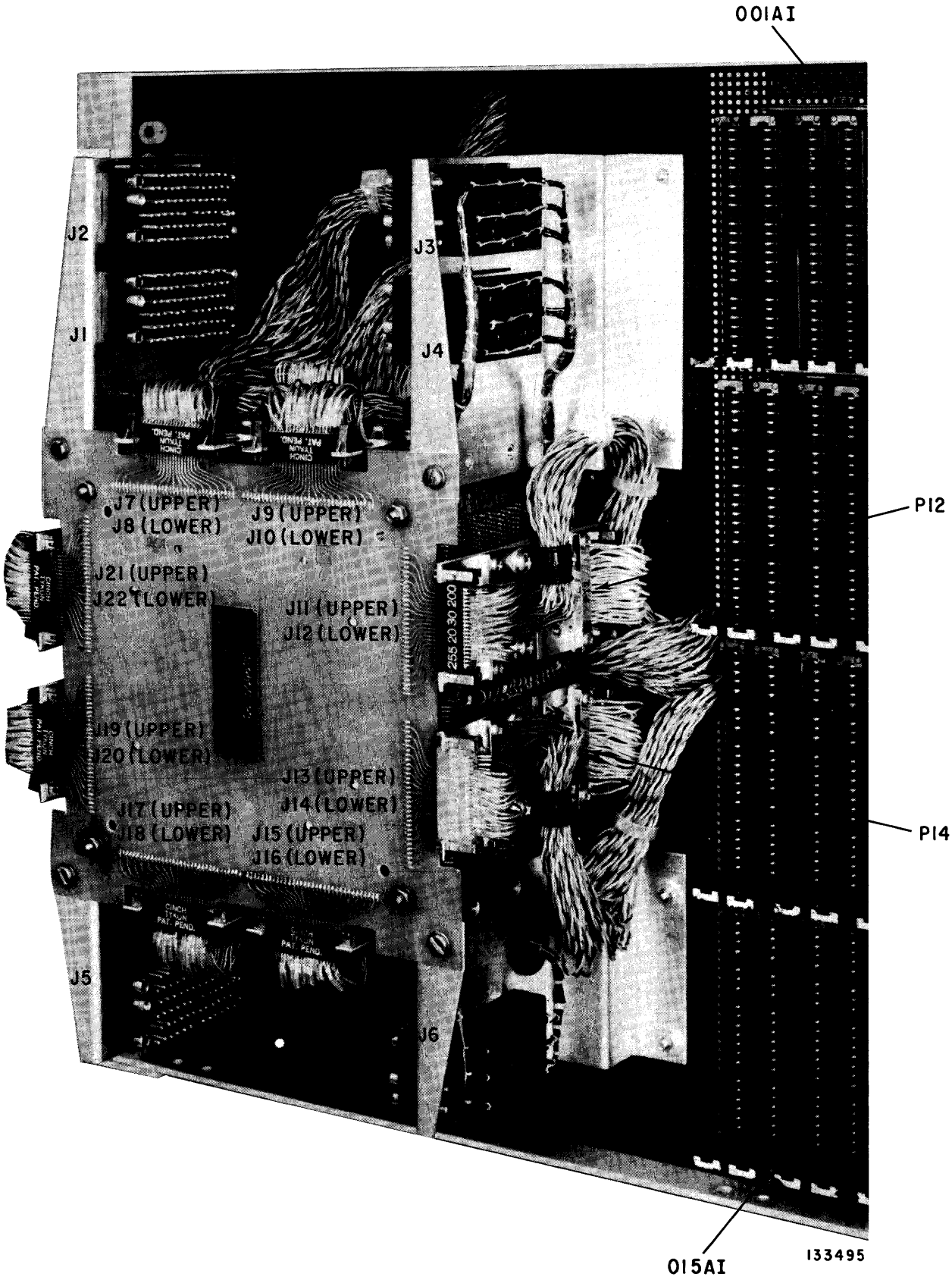


Figure 5-30. 70/55 Main Memory Stack Mounted on Platter

Table 5-14. X Drive Line Selections

Sequential X Line Number	Sub-mats 1,2,3,4 X Address (MAR) 05	06	07	12	13	14	15	INH	Sequential Address Decoding Code
000	0	0	0	0	0	0	0		000
001	↑	↑	↑	1	0	↑	↑		010
002			↓	0	1				020
003			0	1	1			1	030
004			1	0	0				004
005			↑	1	0				014
006		↓	↓	0	1				024
007		0	1	1	1				034
008		1	0	0	0				002
009		↑	↑	1	0				012
010			↓	0	1				022
011			0	1	1			2	032
012			1	0	0				006
013			↑	1	0				016
014		↓	↓	0	1				026
015	↓	1	1	1	1				036
016	1	0	0	0	0				001
017	↑	↑	↑	1	0				011
018			↓	0	1				021
019			0	1	1			1	031
020			1	0	0				005
021			↑	1	0				015
022		↓	↓	0	1				025
023		0	1	1	1				035
024		1	0	0	0				003
025		↑	↑	1	0				013
026			↓	0	1				023
027			0	1	1			2	033
028			1	0	0				007
029			↑	1	0				017
030		↓	↓	0	1				027
031	↓	1	1	1	1	0	0		037

Sequential X Line Number	Sub-mats 5,6,7,8 X Address (MAR) 05	06	07	12	13	14	15	INH	Sequential Address Decoding Code
032	0	0	0	0	0	1	0		040
033	↑	↑	↑	1	0	↑	↑		050
034			↓	0	1				060
035			0	1	1			3	070
036			1	0	0				044
037			↑	1	0				054
038		↓	↓	0	1				064
039		0	1	1	1				074
040		1	0	0	0				042
041		↑	↑	1	0				052
042			↓	0	1				062
043			0	1	1			4	072
044			1	0	0				046
045			↑	1	0				056
046	↓	↓	↓	0	1				066
047	0	1	1	1	1				076
048	1	0	0	0	0				041
049	↑	↑	↑	1	0				051
050			↓	0	1				061
051			0	1	1			3	071
052			1	0	0				045
053			↑	1	0				055
054		↓	↓	0	1				065
055		0	1	1	1				075
056		1	0	0	0				043
057		↑	↑	1	0				053
058			↓	0	1				063
059			0	1	1			4	073
060			1	0	0				047
061			↑	1	0				057
062	↓	↓	↓	0	1	↓	↓		067
063	1	1	1	1	1	1	0		077

Table 5-14. X Drive Line Selections (Continued)

Sequential X Line Number	Sub-mats 9,10,11,12 X Address (MAR) 05	06	07	12	13	14	15	INH	Sequential Address Decoding Code
064	0	0	0	0	0	0	1		100
065	↑	↑	↕	1	0	↑	↑		110
066			↓	0	1				120
067			0	1	1			5	130
068			1	0	0				104
069			↑	1	0				114
070		↓	↓	0	1				124
071		0	1	1	1				134
072		1	0	0	0				102
073		↑	↕	1	0				112
074			↓	0	1				122
075			0	1	1			6	132
076			1	0	0				106
077			↑	1	0				116
078	↓	↓	↓	0	1				126
079	0	1	1	1	1				136
080	1	0	0	0	0				101
081	↑	↑	↕	10	0				111
082			↓	0	1				121
083			0	1	1			5	131
084			1	0	0				105
085			↑	1	0				115
086		↓	↓	0	1				125
087		0	1	1	1				135
088		1	0	0	0				103
089		↑	↕	1	0				113
090			↓	0	1				123
091			0	1	1			6	133
092			1	0	0				107
093			↑	1	0				117
094	↓	↓	↓	0	1	↓	↓		127
095	1	1	1	1	1	0	1		137

Sequential X Line Number	Sub-mats 13,14,15,16 X Address (MAR) 05	06	07	12	13	14	15	INH	Sequential Address Decoding Code
096	0	0	0	0	0	1	1		140
097	↑	↑	↕	1	0	↑	↑		150
098			↓	0	1				160
099			0	1	1			7	170
100			1	0	0				144
101			↑	1	0				154
102		↓	↓	0	1				164
103		0	1	1	1				174
104		1	0	0	0				142
105		↑	↕	1	0				152
106			↓	0	1				162
107			0	1	1			8	172
103			1	0	0				146
109			↑	1	0				156
110	↓	↓	↓	0	1				166
111	0	1	1	1	1				176
112	1	0	0	0	0				141
113	↑	↑	↕	1	0				151
114			↓	0	1				161
115			0	1	1			7	171
116			1	0	0				145
117			↑	1	0				155
118		↓	↓	0	1				165
119		0	1	1	1				175
120		1	0	0	0				143
121		↑	↕	1	0				153
122			↓	0	1				163
123			0	1	1			8	173
124			1	0	0				147
125			↑	1	0				157
126	↓	↓	↓	0	1	↓	↓		167
127	1	1	1	1	1	1	1		177

Table 5-15. Y Drive Line Selections

Sequential Y Line Number	Sub-mats 1,5,9,13 Y Address (MAR) 02	03	04	08	09	10	11	NA	Sequential Address Decoding Code
000	0	0	0	0	0	0	0	0	000
001		0		1					010
002		1		0					002
003		1		1	0				012
004		0		0	1				020
005		0		1					030
006		1		0					022
007		1		1	1	0			032
008		0		0	0	1			040
009		0		1					050
010		1		0					042
011		1		1	0				052
012		0		0	1				060
013		0		1					070
014		1		0					062
015		1		1	1	1	0		072
016		0		0	0	0	1		100
017		0		1					110
018		1		0					102
019		1		1	0				112
020		0		0	1				120
021		0		1					130
022		1		0					122
023		1		1	1	0			132
024		0		0	0	1			140
025		0		1					150
026		1		0					142
027		1		1	0				152
028		0		0	1				160
029		0		1					170
030		1		0					162
031	0	1	0	1	1	1	1	0	172

Sequential Y Line Number	Sub-mats 2,6,10,14 Y Address (MAR) 02	03	04	08	09	10	11	NA	Sequential Address Decoding Code
032	0	0	1	0	0	0	0	0	004
033		0		1					014
034		1		0					006
035		1		1	0				016
036		0		0	1				024
037		0		1					034
038		1		0					026
039		1		1	1	0			036
040		0		0	0	1			044
041		0		1					054
042		1		0					046
043		1		1	0				056
044		0		0	1				064
045		0		1					074
046		1		0					066
047		1		1	1	1	0		076
048		0		0	0	0	1		104
049		0		1					114
050		1		0					106
051		1		1	0				116
052		0		0	1				124
053		0		1					134
054		1		0					124
055		1		1	1	0			136
056		0		0	0	1			144
057		0		1					154
058		1		0					146
059		1		1	0				156
060		0		0	1				164
061		0		1					174
062		1		0					166
063		1	1	1	1	1	1	0	176
064		0	0						NA0
065		0	1						NA4
066		1	0						NA2
067	0	1	1						NA6

Table 5-15. Y Drive Line Selections (Continued)

Sequential Y Line Number	Sub-mats 3,7,11,15 Y Address (MAR) 02	03	04	08	09	10	11	NA	Sequential Address Decoding Code
068	1	0	0	0	0	0	0	0	001
069		0		1					011
070		1		0					003
071		1		1	0				013
072		0		0	1				021
073		0		1					031
074		1		0					023
075		1		1	1	0			033
076		0		0	0	1			041
077		0		1					051
078		1		0					043
079		1		1	0				053
080		0		0	1				061
081		0		1					071
082		1		0					063
083		1		1	1	1	0		073
084		0		0	0	0	1		101
085		0		1					111
086		1		0					103
087		1		1	0				113
088		0		0	1				121
089		0		1					131
090		1		0					123
091		1		1	1	0			133
092		0		0	0	1			141
093		0		1					151
094		1		0					143
095		1		1	0				153
096		0		0	1				161
097		0		1					171
098		1		0					163
099	1	1	0	1	1	1	1	0	173

Sequential Y Line Number	Sub-mats 4,8,12,16 Y Address (MAR) 02	03	04	08	09	10	11	NA	Sequential Address Decoding Code
100	1	0	1	0	0	0	0	0	005
101		0		1					015
102		1		0					007
103		1		1	0				017
104		0		0	1				025
105		0		1					035
106		1		0					027
107		1		1	1	0			037
108		0		0	0	1			045
109		0		1					055
110		1		0					047
111		1		1	0				057
112		0		0	1				065
113		0		1					075
114		1		0					067
115		1		1	1	1	0		077
116		0		0	0	0	1		105
117		0		1					115
118		1		0					107
119		1		1	0				117
120		0		0	1				125
121		0		1					135
122		1		0					127
123		1		1	1	0			137
124		0		0	0	1			145
125		0		1					155
126		1		0					147
127		1		1	0				157
128		0		0	1				165
129		0		1					175
130		1		0					167
131	1	1	1	1	1	1	1	0	177
132	1	0	0					1	NA1
133	1	0	1					1	NA5
134	1	1	0					1	NA3
135	1	1	1					1	NA7

side of the stack and the second drive line down, etc. The currents are also staggered for the Y system with Y000 being at the upper left side of the stack (J7) and Y001 at the lower left side of the stack. Y drive lines are counted from left to right.

Each column in Table 5-14 reflects a mat row and each column in Table 5-15 reflects a mat column (see Figure 5-27). The Non-Addressable areas are located in the mat columns or Y selections.

5.7 MAINTENANCE

5.7.1 DRIVE CURRENT SETTING

With the processor stopped in the General Reset condition, connect the leads of a digital voltmeter (DVM) to the test jacks on the 8M31 plug-in. See Figure 5-23 for the locations of the test points. Connect the signal ground of the digital voltmeter to TP1 and the red jack of the digital voltmeter to TP2. Adjust the potentiometer on the plug-ins for the X and Y drive systems to obtain a reading of 560mV, ±2mV on the DVM.

CAUTION

Do not connect the signal ground of the DVM to chassis ground. The signal ground must be "floating".

5.7.2 MARGINAL CHECK

After reading in the Main Memory Noise Test (MLT #705) and adjusting the program to recycle, set the marginal check button for the bank under test (i.e. BK1).

With the marginal check voltage reading zero, start the program and adjust the marginal check potentiometer to reduce the reading in 0.5 volt steps (toward -10). Allow the program to complete one cycle through the memory addresses for each 0.5 volt increment. When an error occurs, readjust the test voltage to the preceding step, restart the program, and, using smaller increments, determine the lowest voltage at which the memory is operable to the nearest 0.5 volt step. Repeat this procedure to determine the highest operable voltage (toward +10). The range should be at least -2.5V to +5.5V. Since the range of the non-addressable main memory portion cannot be checked by this program, a repeat function of store and read "0" and "1" are required for this area. The range of this test should be at least -4.0V and +4.5V.

5.7.3 STROBE TIMING ADJUSTMENTS

Relative strobe position (rsp) adjustments in the main memory are divided into seven separate delay adjustments. See Table 5-16 for the location of the delay lines for the rsp controls for any bank of memory.

Table 5-16. Delay Line Location of RSP Controls

Stack Type	Data Bits	Strobe Early 9AK-D10, D12	Strobe Late 9AK-D7, D9	1st HALF BANK		2nd HALF BANK		Main Strobe 9AK-D4,D5
				X READ 12 6AG-D7,D9	X READ 11 6AG-D10,D12	X READ 22 6AG-D1,D3	X READ 21 6AG,D4,D6	
D	00	X		X		X		X
	01	X		X		X		X
	02	X		X		X		X
	03	X		X		X		X
	04	X		X		X		X
	05		X	X		X		X
	06		X	X		X		X
	07		X	X		X		X
	08		X	X		X		X
	09		X	X		X		X
	10		X	X		X		X
	11		X	X		X		X
	12		X	X		X		X
	13	X		X		X		X
	14	X		X		X		X
	15	X		X		X		X
	16	X		X		X		X
C	17	X			X		X	X
	18	X			X		X	X
	19	X			X		X	X
	20	X			X		X	X
	21		X		X		X	X
	22		X		X		X	X
	23		X		X		X	X
	24		X		X		X	X
	25		X		X		X	X
	26		X		X		X	X
	27		X		X		X	X
	28		X		X		X	X
	29	X			X		X	X
	30	X			X		X	X
	31	X			X		X	X
	32	X			X		X	X

NOTE: X indicates that the bit is affected.

Figure 5-31 shows the nominally correct position of the strobe with relation to the output core signals. Each memory bank should be considered as an independent memory unit insofar as strobe position is concerned because every bank has its own rsp delays.

5.7.3.1 Preliminary Test For RSP

If the conditions listed below are satisfied, then the rsp should be very close to the correct position and the memory should be operational:

1. While regenerating all "zeros" the first pickup error should not occur at a marginal voltage above +4.0 volts (-6.0 volts on the maintenance panel meter). See section 5.7.5 for the procedure used to write and read from the memory.

2. Correct the error address of (1) by writing into the failed address, the bit that had caused the error. For example, only the parity bit (bit 32) should have been read from the memory but because of the pick-up failure, bits 04 and 32 were read, then write bit 04 into the address that had failed.

   Continue regenerating all "zeros". The second pickup error should not be more than one-half to one volt away from the marginal voltage reading of the first error.

3. While regenerating "ones", the first drop error should not occur at a marginal voltage below +16.0 volts (+6.0 volts on the maintenance panel meter). See (2) for the procedure for correcting the error, however the error bit must be omitted in this case rather than added.

4. Continue regenerating "ones". The second drop error should not be more than one-half volt to one volt away from the marginal voltage reading of the first error.

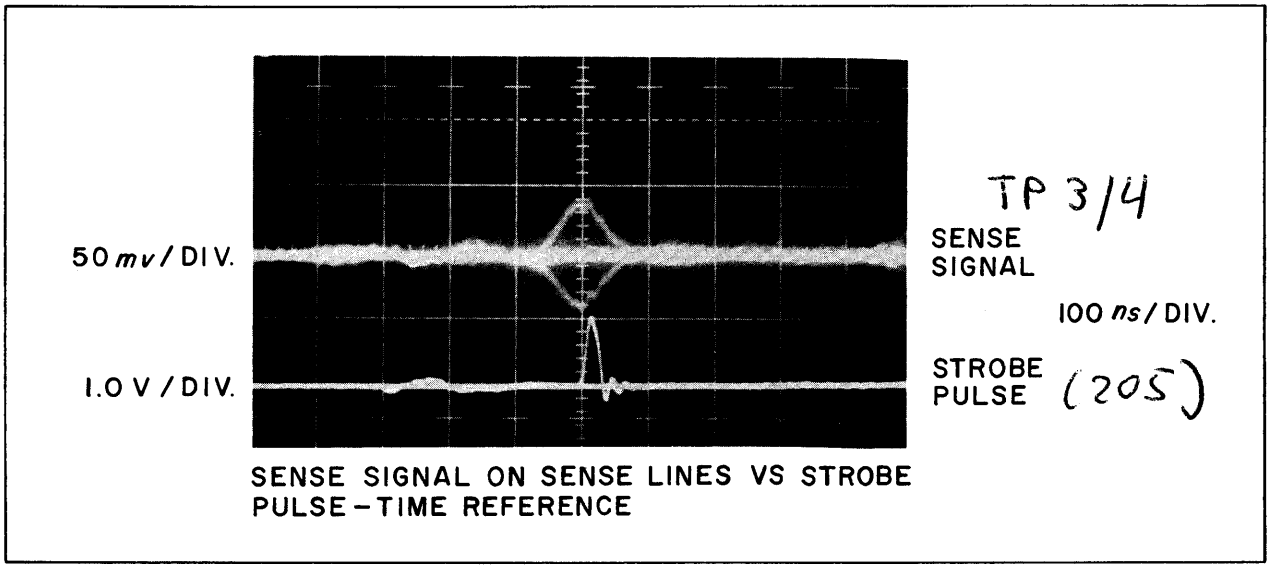


Figure 5-31. Sense Signal/Strobe Pulse

5. The high end (drop) and the low end (pickup) error should be in the same rsp control groups; that is, both errors should be early strobe errors or late strobe errors and the failures should be in the same memory stack (X READ command).

CAUTION

Two restrictions of the X READ command delay lines settings are as follows: X READ 21 and/or X READ 22 delay setting(s) should be zero nanoseconds; and the maximum delay setting for any X READ command should not be greater than 10 nanoseconds.

5.7.3.2 Memory Operating Margin Specification

The main memory must operate without errors while being exercised by library tape block 705 over a marginal voltage range from +7.0 through +14.5 volts (approximately -3.0 through +4.5 volts on the maintenance panel meter).

5.7.4.0 General Troubleshooting Guide

The Troubleshooting Flow Chart, Figure 5-32 shows a general procedure for determining the causes of malfunctions in the Main Memory. Any suspected memory malfunction must be examined from the data and address problems that are evident. Any memory problem should easily be traced to the bank number and then, in almost all cases, to the half bank level. An open sense line is one case in which a bit in one half bank could affect the operation of that same bit in the other half bank.

Every branch block of the Troubleshooting Flow Chart is numbered. The number corresponds to a brief descriptive explanation of the problem in the following text of the Troubleshooting Guide section. Blocks are again subdivided on the following pages so that maintenance personnel can follow their particular problems with a minimum amount of effort.

5.7.4.0.1 Examine Error Pattern

A "drop" error pattern can be determined by writing "ones" into the memory and then operating the memory in a continuous read mode while slowly turning the marginal check voltage in the increasing voltage direction until a drop error occurs. Record the error and the address then begin reading from the address following the failure. Record the error and the address of the second failure and begin reading from the address following the second failure. This procedure can be continued until an error pattern becomes apparent. The same procedure can be used to determine a "pick-up" error pattern, however, write "zeros" into the memory rather than "ones", then slowly decrease the marginal check voltage during the continuous read mode of operation.

Table 5-17 shows a sample test sequence that can be used to determine an error pattern. The next higher address was selected as the starting

5. The high end (drop) and the low end (pickup) error should be in the same rsp control groups; that is, both errors should be early strobe errors or late strobe errors and the failures should be in the same memory stack (X READ command).

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Table 5-17 shows a sample test sequence that can be used to determine an error pattern. The next higher address was selected as the starting

address for the second sequence (bits 00 and 01 have no meaning in the memory insofar as addressing is concerned). Note that in the second test sequence, a second X current switch (controlled by address bits 05, 06 and 07) successfully read the same Y current switch (controlled by address bits 02, 03 and 04) locations that the first X current switch read. The third test sequence, then, was selected to investigate the Y voltage switches (MAR bits 08-11). The address of the second error shows that the second Y voltage switch successfully read all locations (at least as many as had been tried) that the first voltage switch read. The fourth test sequence was selected to investigate the X voltage switches in the same manner as the Y voltage switches.

Examination of Table 5-17 shows that MAR bits 03 and 04 are common to all the error addresses and in all cases, a half word, bits 00-16, was dropped. Refer to the decoding tables of the memory address in section 5.4 to determine the selection resulting from common MAR bits involved in the errors. Table 5-8 shows that Y current switch six is defective. The read or/and write switch or switches could be causing the problem. The error pattern that was developed indicates that the error is associated with a half word (bits 00-16) and is common to a Y current switch.

A second sample illustration is shown in Table 5-18. The first error shows that the memory successfully read from all the Y current switches but not all the X switches. The second test sequence, just as above, is started from the next memory address. Examination of the memory word error, pickup bit 19, and the common MAR bit, 06, indicates that an X current switch (MAR05, 06 and 07) or an inhibit driver (MAR 06, 14 and 15) might be involved in the error. A third test sequence selecting another current switch shows that the error is not associated with a current switch. The fourth test sequence should select a different inhibit driver line. An error in a low address of the memory (the memory had completed one pass through all addresses and is once again starting from the beginning) indicates that all of the inhibit lines are good except the one selected by MAR bit 06. The error pattern that was developed indicates that the error is associated with a single bit in a half bank at multiple addresses associated with an inhibit line.

The sample test sequences illustrated present a pattern that can be followed by maintenance personnel in developing an error pattern. The Memory Address Decoding section should be freely used to aid the maintenance man in determining the starting address that should be used after an error has occurred.

5.7.4.1 Random Bit And/Or Random Address Problem

Multiple drops occur which do not appear to have any correlation to the address. This type of problem can best be determined by following the steps outlined below:

1. Depress the marginal voltage switch located on the maintenance panel to the bank which is suspected of being bad.

2. Adjust the marginal voltage to read approximately +4.0 volts on the marginal check meter on the maintenance panel.

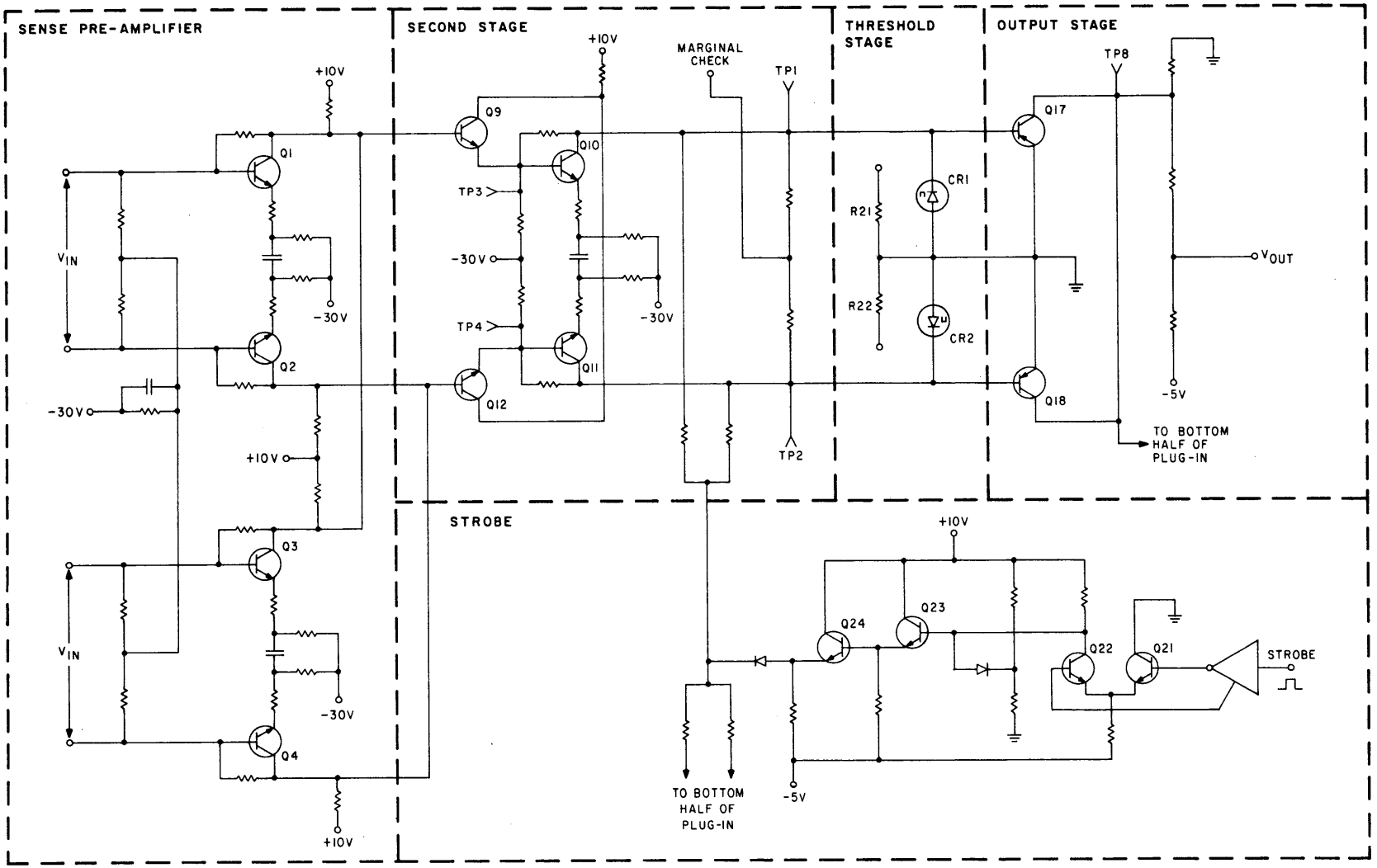


Figure 5-25. Sense Amplifier, Simplified Schematic Diagram

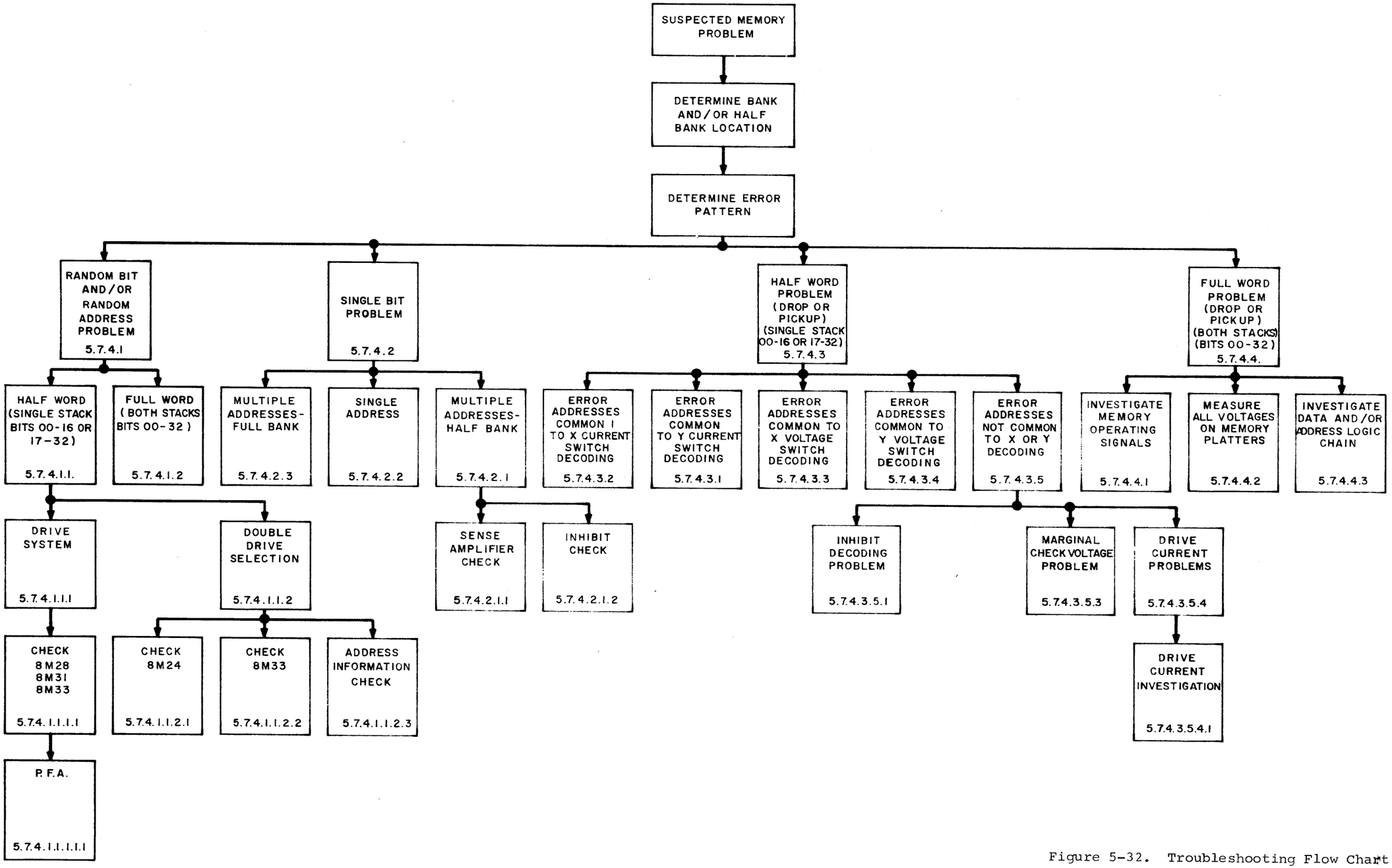


Figure 5-32. Troubleshooting Flow Chart ■

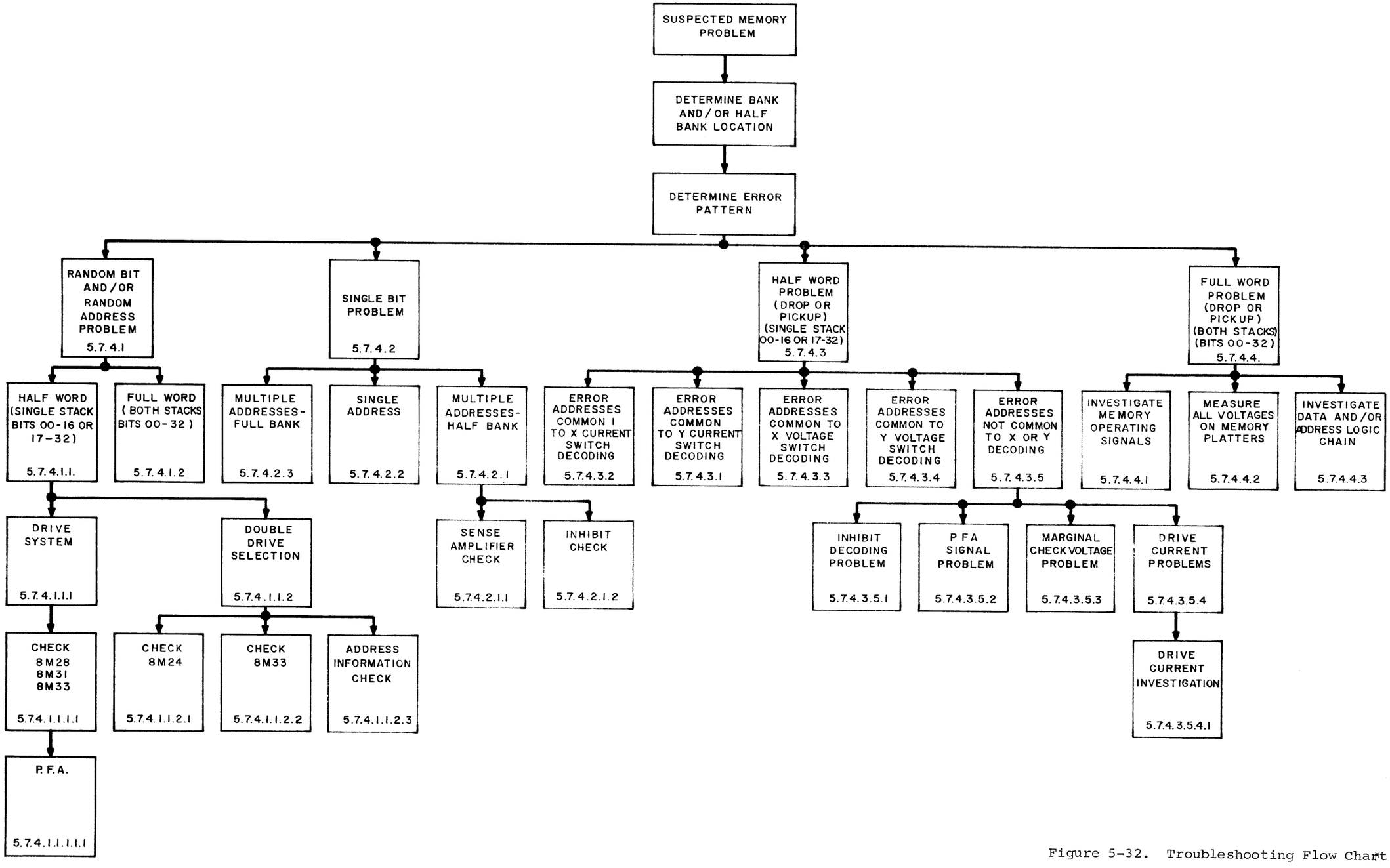


Figure 5-32. Troubleshooting Flow Chart

Table 5-17. Error Pattern For a Half Word Problem

Test Sequence	Read Cycle Start Address	Error Address	Bank	Half Bank	Error Drop	MAR Bits in Error Address	Common MAR Bits	Common MR Bits
1	0000	0018	I	1st	00-16	03,04	03,04	00-16
2	001C	0038	I	1st	00-16	03,04,05		
3	0100	0018	I	1st	00-16	03,04,08		
4	1000	1018	I	1st	00-16	03,04,12		

Table 5-18. Error Pattern For a Single Bit Problem

Test Sequence	Read Cycle Start Address	Error Address	Bank	Half Bank	Error Pickup	MAR Bits in Error Address	Common MAR Bits	Common MR Bits
1	0000	0040	II	1st	19	06	06	19
2	0044	0044	II	1st	19	02,06		
3	0060	0060	II	1st	19	05,06		
4	4000	0040	II	1st	19	06		

3. Write "ones" into the memory. Read back the information that was written.

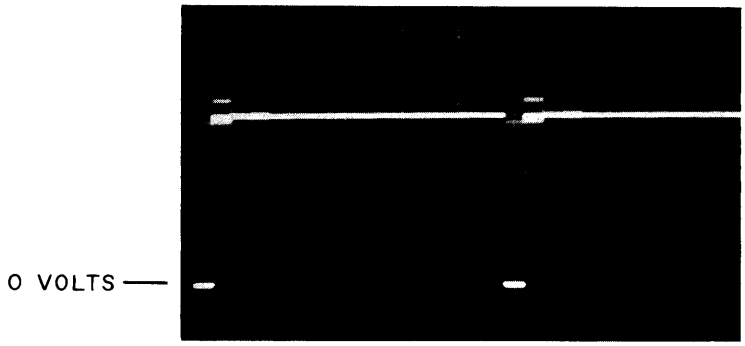
If at least eight bits of the half word or full word drop at multiple addresses, then the random bit and/or random address problem should be investigated. Usually at least one or two bits are dropped at the nominal marginal voltage setting of 0 volts on the panel meter.

5.7.4.1.1 Half Word

If all the error bits determined in test 5.7.4.1 are located in a single stack (bits 00 through 16 for one stack or bits 17 through 32 in the second stack), then the half word problem should be investigated.

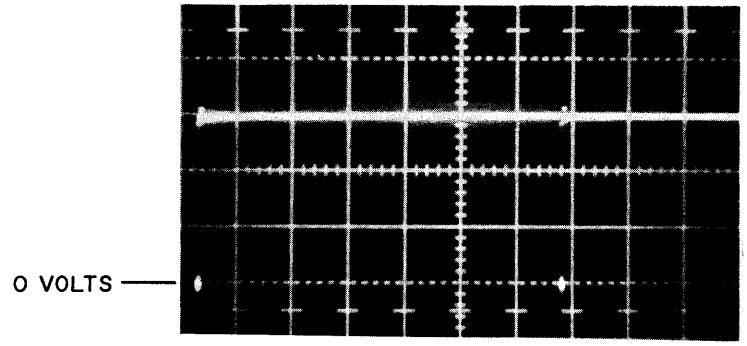
5.7.4.1.1.1 Drive System Investigation

Check the voltage settings on both X and Y 8M31 plug-ins with a digital voltmeter (see Section 5.7.1). If any one of the voltages is off by more than five millivolts, check the +50 volt and +30 volt supplies on the memory cabinet for a maximum of a 1.0% variation from nominal; readjust if necessary. If the +50 volt and +30 volt supplies are within the specified tolerance and the 8M31 voltage is still not within five millivolts of the 560mv, then probably the 8M31 and/or one or more 8M28 plug-ins are bad. After replacing the defective plug-in(s), readjust the voltage on the 8M31 plug-in to 560mv and check the 8M33 plug-ins driving the stack. See Figures 5-33 and 5-34 for specified 8M33 output voltage waveforms. Figures 5-35 and 5-36 show the results of breakdown of the voltage switch transistors.



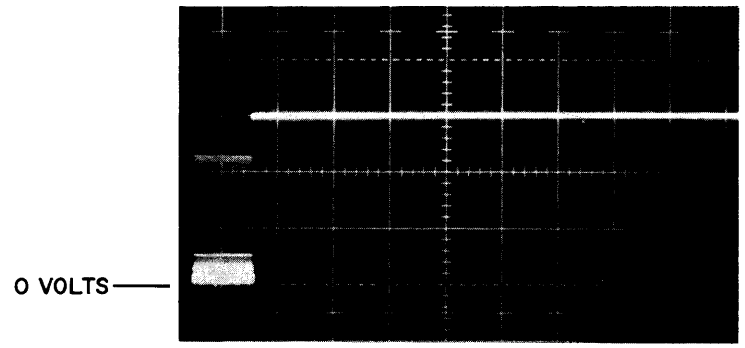
NORMAL TIMING OUTPUT FOR Y VOLTAGE SWITCH
(VOLTAGE SWITCH SHOULD ALWAYS RETURN TO AT LEAST +27 VOLTS)

Figure 5-33. Y Voltage Switch Output



NORMAL TIMING OUTPUT FOR X VOLTAGE SWITCH
(VOLTAGE SWITCH SHOULD ALWAYS RETURN TO AT LEAST +27 VOLTS)

Figure 5-34. X Voltage Switch Output



X VOLTAGE SWITCH NOT RECOVERING

Figure 5-35. Defective X Voltage Switch

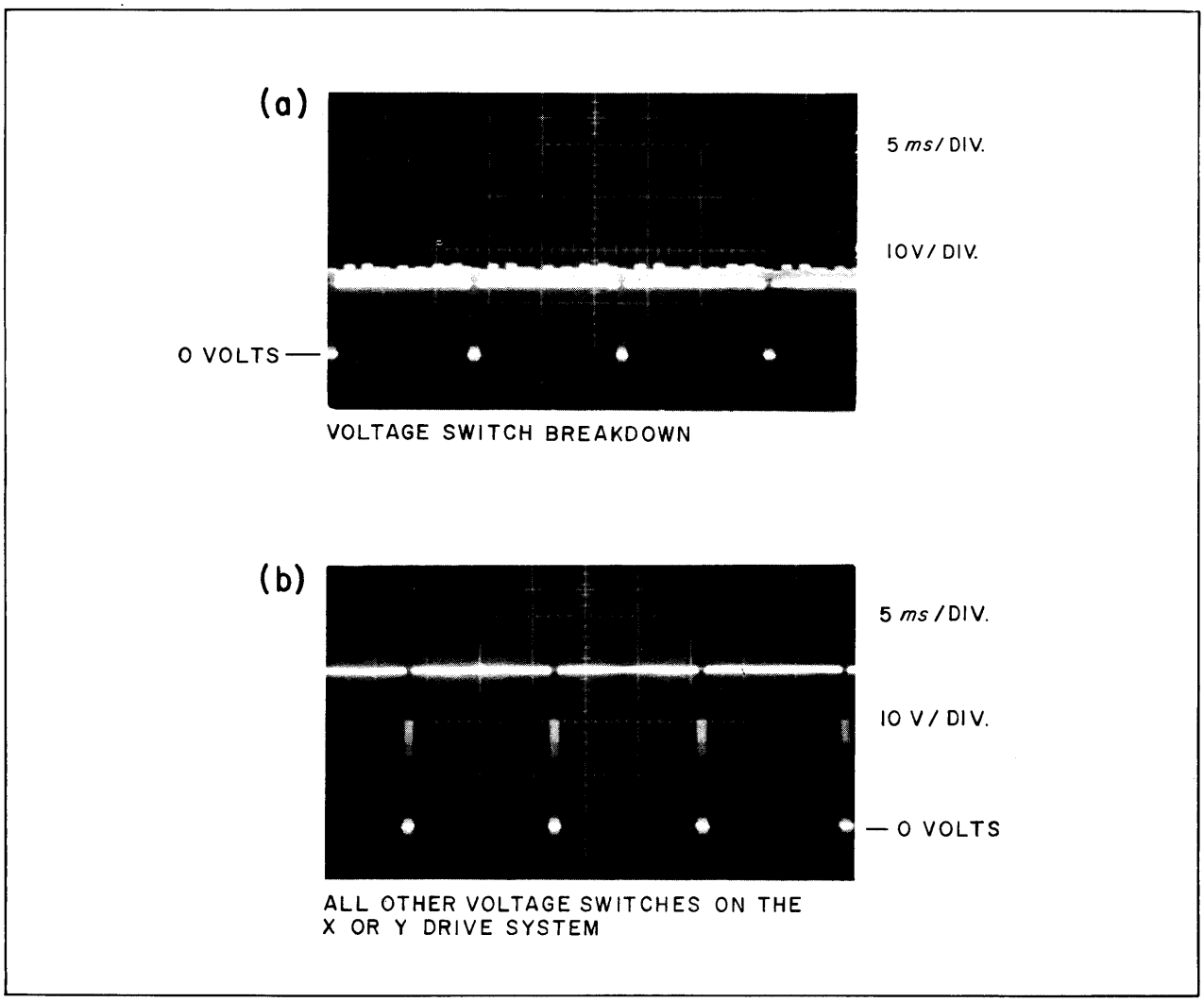


Figure 5-36. Voltage Switch Waveforms

5.7.4.1.1.1.1 Check 8M31, 8M33 & 8M28

If the d-c condition of the 8M31 of step 5.7.4.1.1.1 cannot be satisfied, stop the memory from being addressed, cycle down power and remove the 8M31 plug-in. Measure the resistance between the collector-to-emitter junction of the transistor mounted in the heat sink on every 8M28 plug-in being driven by the 8M31 plug-in involved. Use a Simpson Model 260 volt-ohmmeter on the RX10,000 scale. The meter should read a short circuit in one direction and a resistance in excess of 2 megohms in the opposite direction. If any 8M28 does not satisfy the above test, it should be replaced.

NOTE: The metal part of the meter test leads should not be touched with the hands because the meter readings will be affected.

After the 8M28 plug-ins are checked as described above (defective plug-ins replaced), the 8M33 plug-ins (voltage switches) should then be investigated. In the event the first half bank of the first bank is being investigated, it should be pointed out that the 8M25-7 (pull-down plug-in) contains the non-addressable voltage switch. An 8M25-5 can be used in place of an 8M25-7 for testing purposes. Apply power to the memory before installing the 8M31 and perform a continuous write to all addresses of the memory. Observe all voltage switch outputs and compare them with the waveforms specified in Figure 5-37. If all voltage switches satisfy the conditions in Figure 5-37 then the memory is ready for the 8M31 plug-in. Retest the "ones" and "zeros" ranges of the memory.

Caution should be exercised in investigating any drive system problems because a defective 8M31 plug-in could cause a "blow out" of the drive system even after it has been repaired. Therefore, the 8M31 should be checked for shorts with a Simpson Model 260 volt-ohmmeter or equivalent as follows:

Table 5-19. Evaluation of Current Source, 8M31

Measure Between	Scale	Approximate Reading
Q11 emitter* to Q11 base	X1 ohms	40 ohms
Q11 collector* to Q11 base	X1 ohms	40 ohms
Q11 collector* to Q11 emitter	X1 ohms	15 ohms
Q11 emitter* to Q11 collector	X1 ohms	over 500 ohms
Q1 emitter* to Q1 collector	X1 ohms	over 500 ohms
Q1 collector* to Q1 emitter	X1 ohms	over 200 ohms
Q6 emitter* to Q6 collector	X1 ohms	over 500 ohms
Q6 collector* to Q6 emitter	X1 ohms	over 200 ohms

* Indicates the plus lead of the meter.

If any measurement is not correct, replace the 8M31 plug-in or repair it.

Install a good 8M31 in the drive system and retest the "ones" and "zeros" range. If the problem still persists, observe the output voltage waveforms at the output of the current source. On the MM1SR platter the Y current source is located at 3AC (8M31, pin 206) and the X current source at 9AC (8M31, pin 206). On the MM1SL platter the Y current source is located at 3BQ (8M31, pin 206) and the X current source at 9BQ (8M31, pin 206). See Figures 5-38 through 5-41 for satisfactory output voltage waveforms. Also observe all of the voltage switch outputs while they are conducting maximum currents. See Figures 5-42 and 5-43 for specified voltage switch output waveforms.

5.7.4.1.1.1.1.1 PFA

The Power Failure Alarm signal is a d-c voltage of approximately ten volts and it is generated by the power supply. The PFA signal is routed to all 8M31 plug-ins through pin 226. If the voltage is not present the memory will not be capable of reading or writing "ones".

After the 8M28 plug-ins are checked as described above (defective plug-ins replaced), the 8M33 plug-ins (voltage switches) should then be investigated. In the event the first half bank of the first bank is being investigated, it should be pointed out that the 8M25-7 (pull-down plug-in) contains the non-addressable voltage switch. An 8M25-5 can be used in place of an 8M25-7 for testing purposes. Apply power to the memory before installing the 8M31 and perform a continuous write to all addresses of the memory. Observe all voltage switch outputs and compare them with the waveforms specified in Figure 5-37. If all voltage switches satisfy the conditions in Figure 5-37 then the memory is ready for the 8M31 plug-in. Retest the "ones" and "zeros" ranges of the memory.

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Q11 collector* to Q11 emitter	X1 ohms	15 ohms
Q11 emitter* to Q11 collector	X1 ohms	over 500 ohms
Q1 emitter* to Q1 collector	X1 ohms	over 500 ohms
Q1 collector* to Q1 emitter	X1 ohms	over 200 ohms
Q6 emitter* to Q6 collector	X1 ohms	over 500 ohms
Q6 collector* to Q6 emitter	X1 ohms	over 200 ohms

* Indicates the plus lead of the meter.

If any measurement is not correct, replace the 8M31 plug-in or repair it.

Install a good 8M31 in the drive system and retest the "ones" and "zeros" range. If the problem still persists, observe the output voltage waveforms at the output of the current source. On the MM1SR platter the Y current source is located at 3AC (8M31, pin 206) and the X current source at 9AC (8M31, pin 206). On the MM1SL platter the Y current source is located at 3BQ (8M31, pin 206) and the X current source at 9BQ (8M31, pin 206). See Figures 5-38 through 5-41 for satisfactory output voltage waveforms. Also observe all of the voltage switch outputs while they are conducting maximum currents. See Figures 5-42 and 5-43 for specified voltage switch output waveforms.

5.7.4.1.1.1.1.1 MDPR

The Memory Delay Power Reset signal (MDPR) is a momentary signal from K2 in the power supply to the memory (see Figure 5-66B).

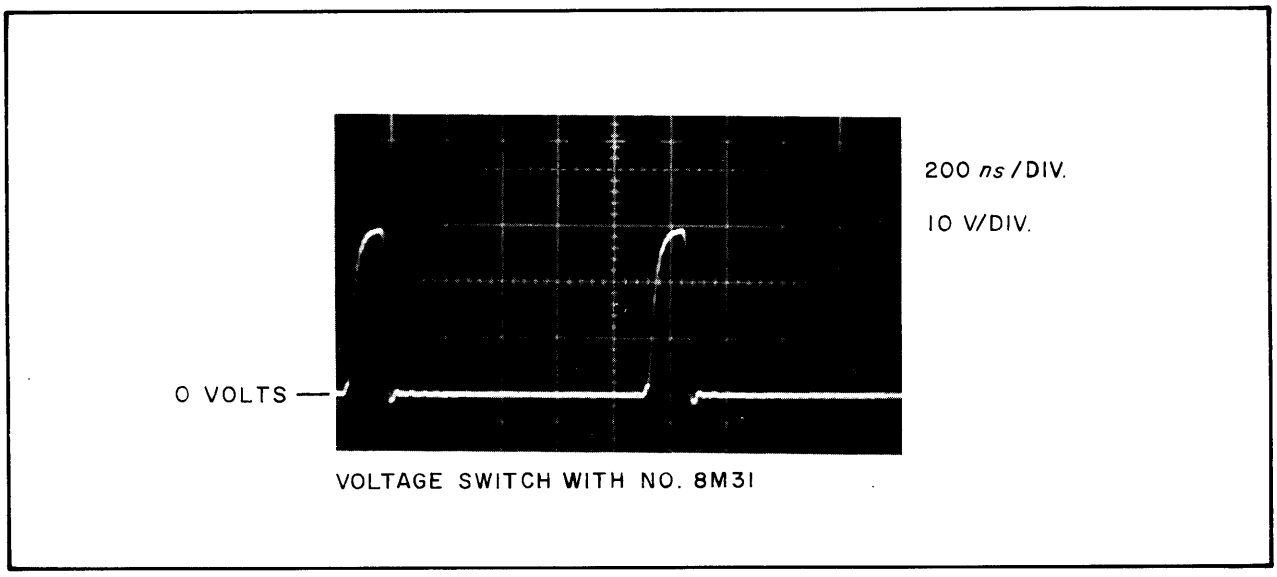


Figure 5-37. Voltage Switch Output

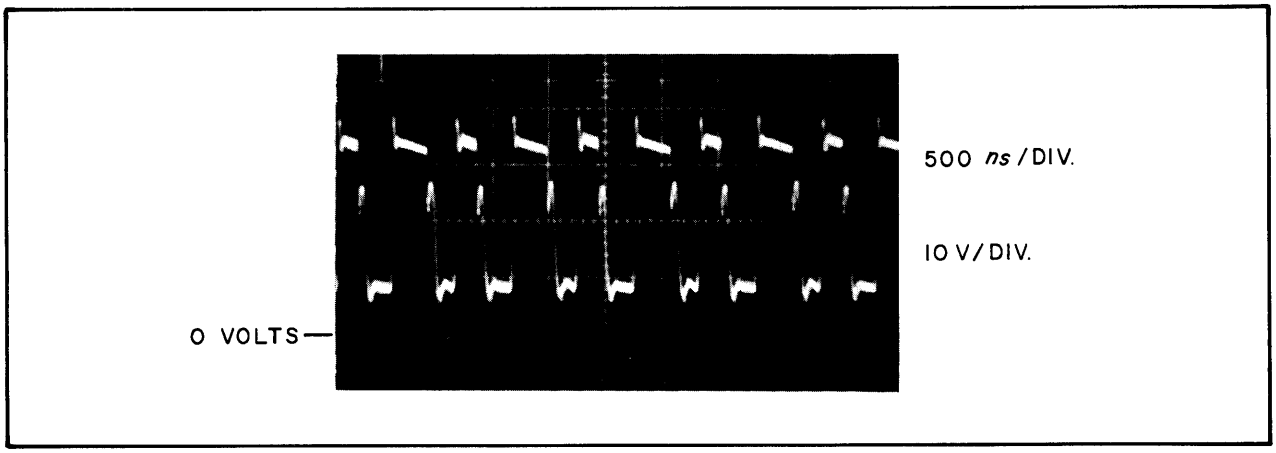


Figure 5-38. Y Current Source Output

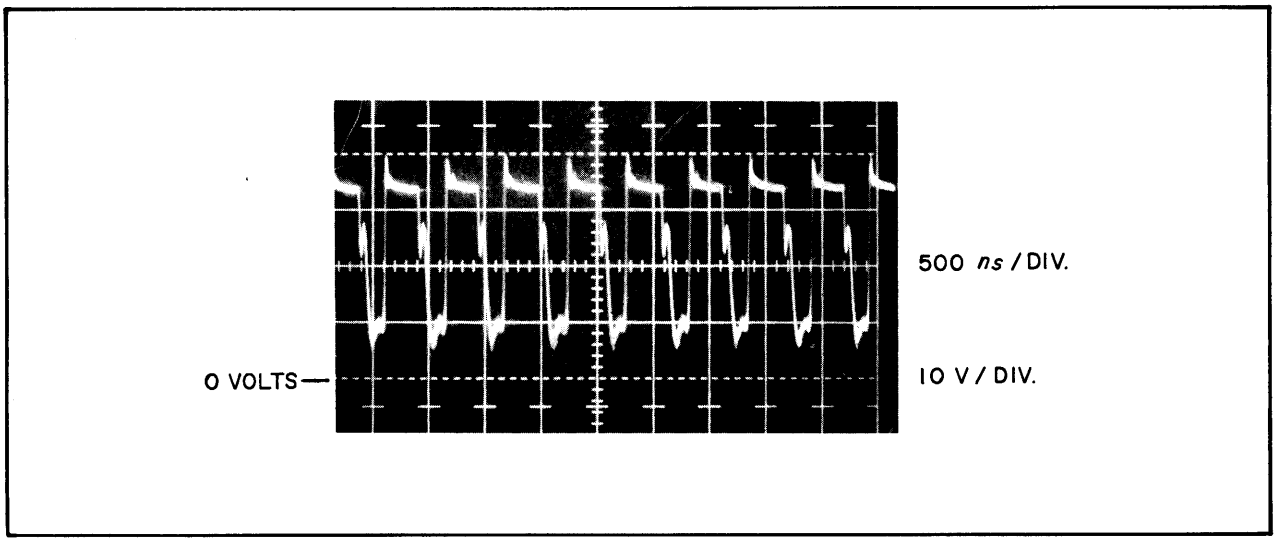


Figure 5-39. X Current Source Output

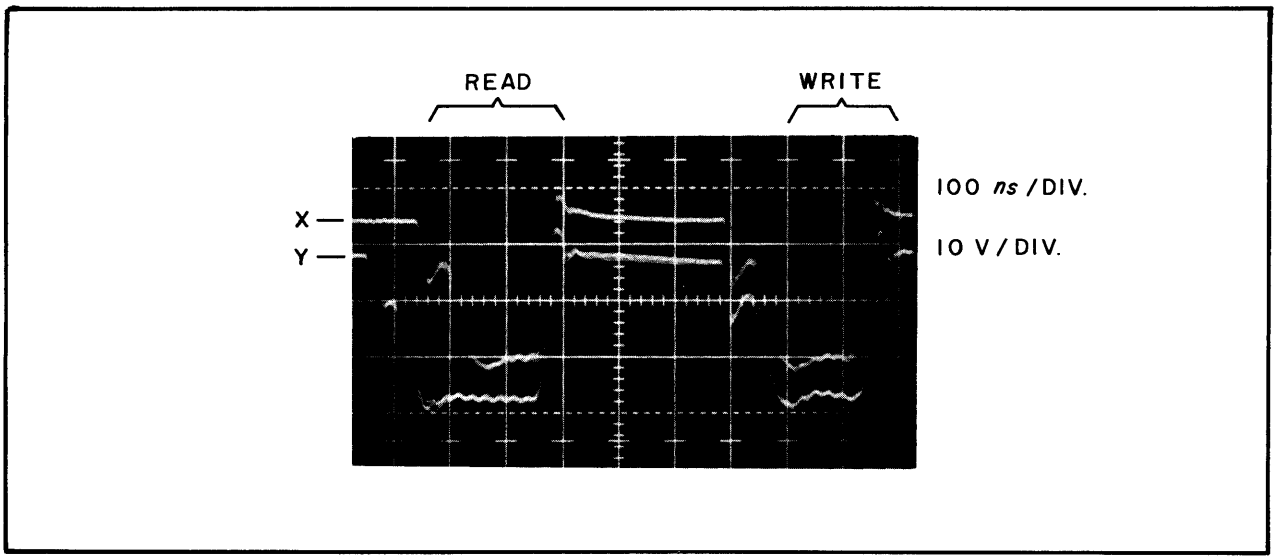


Figure 5-40. Expanded View of X and Y Current Sources

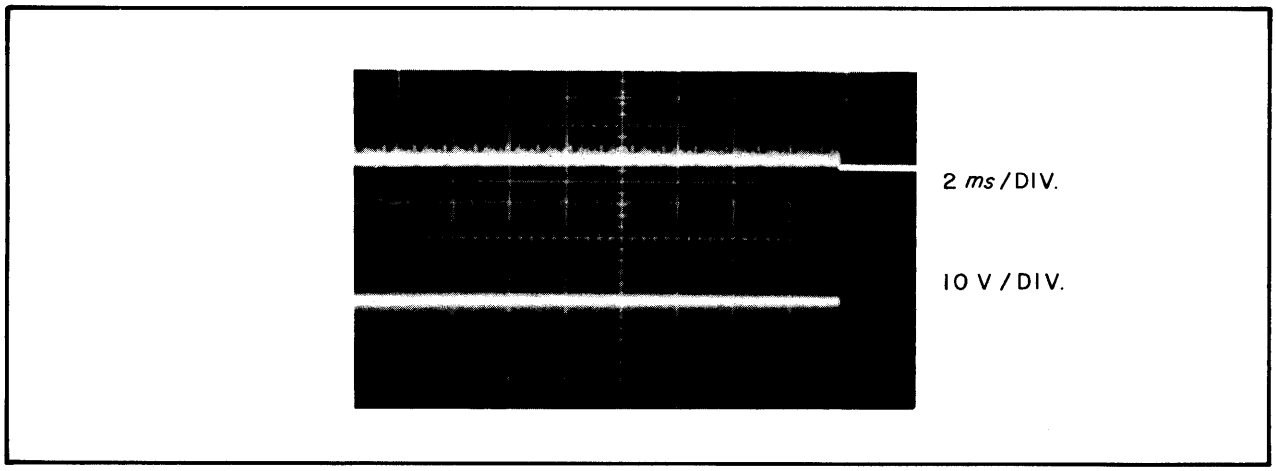


Figure 5-41. Y Current Source - Full Time View

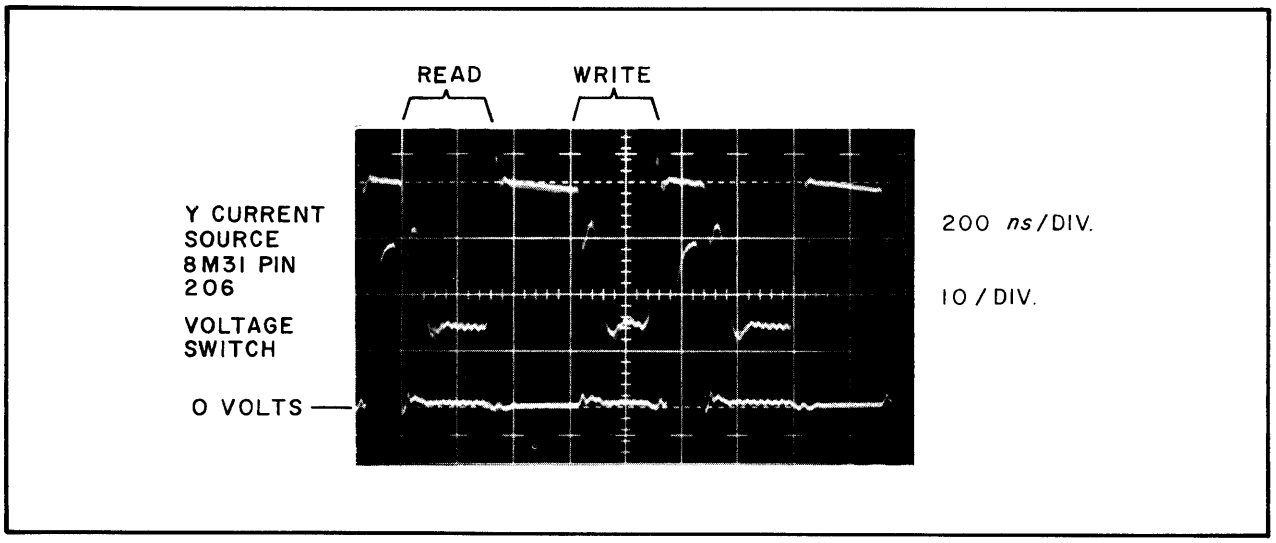


Figure 5-42. Y Voltage Switch and Y Current Source Timing

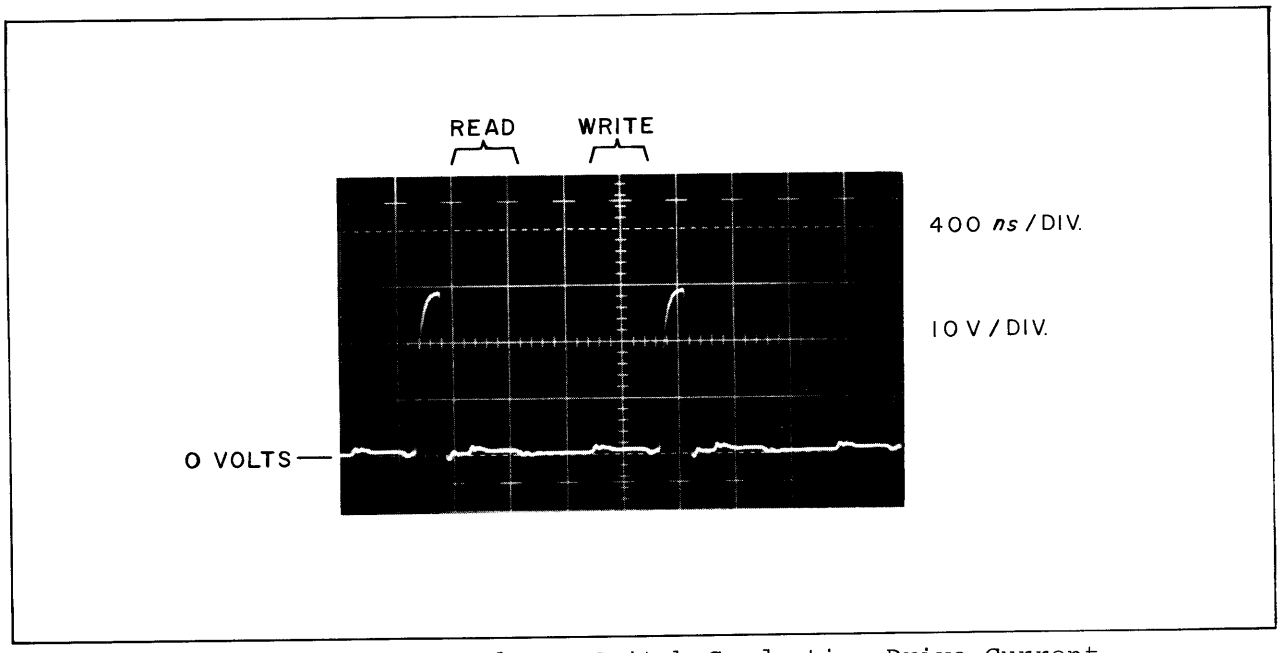


Figure 5-43. X Voltage Switch Conducting Drive Current

If for any reason noise on the signal line causes the PFA voltage to fall below 5.0 volts, the drive current could be interrupted causing intermittent troubles in any particular stack or in the entire memory.

If the PFA signal is strongly suspected as being a problem, the serviceman can disconnect the PFA signal from the memory stack involved and use the +10.0 volt supply available on the platter as the PFA signal.

5.7.4.1.1.2 Double Drive Selection

A stack addressing problem could be caused by a problem in the 8M24 (current switch decoder) or in the 8M33 (which contains the voltage switch decoding as well as the voltage switches) or by the absence of the memory address bits at the MM1S platters. An addressing problem will result in a double selection of the current and/or voltage switches.

5.7.4.1.1.2.1 Check 8M24

A double selection of the current switches will not, in most cases, be detected while observing the current source output at pin 206 of the 8M31. The output of the 8M24, current switch decoder can be observed at pin 36 of the 8M28 plug-ins. Figures 5-44 and 5-45 show the specified waveform which should be observed at the 8M28 inputs. Because of the decoding scheme used to select the 8M28's, CS00 and CS04 have different waveforms.

Pulse A of Figures 5-44 and 5-45 generate the read current and Pulse B generate the write current. A missing pulse A can be caused by the absence of the read pulse from pin 10 of the 8M24 plug-in when current switches 00, 01, 02, and 03, are being observed, or from pin 23 when current switches 04, 05, 06 and 07 are being observed. Absence of an A pulse from any set observed indicates an open circuit in the transformer circuit of one of the 8M28 plug-ins (between pins 33 and 36). Absence of the gating pulse indicates a bad output from the 8M24 plug-in. See listing below:

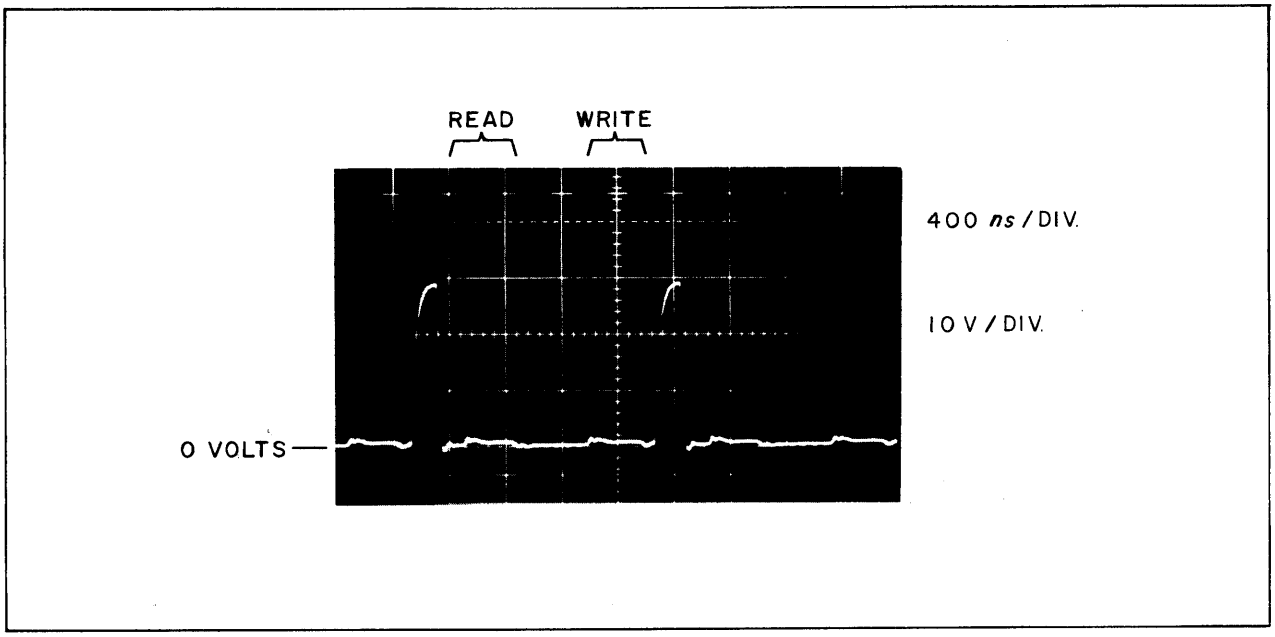


Figure 5-43. X Voltage Switch Conducting Drive Current

5.7.4.1.1.2 Double Drive Selection

A stack addressing problem could be caused by a problem in the 8M24 (current switch decoder) or in the 8M33 (which contains the voltage switch decoding as well as the voltage switches) or by the absence of the memory address bits at the MM1S platters. An addressing problem will result in a double selection of the current and/or voltage switches.

5.7.4.1.1.2.1 Check 8M24

A double selection of the current switches will not, in most cases, be detected while observing the current source output at pin 206 of the 8M31. The output of the 8M24, current switch decoder can be observed at pin 36 of the 8M28 plug-ins. Figures 5-44 and 5-45 show the specified waveform which should be observed at the 8M28 inputs. Because of the decoding scheme used to select the 8M28's, CS00 and CS04 have different waveforms.

Pulse A of Figures 5-44 and 5-45 generate the read current and Pulse B generate the write current. A missing pulse A can be caused by the absence of the read pulse from pin 10 of the 8M24 plug-in when current switches 00, 01, 02, and 03, are being observed, or from pin 23 when current switches 04, 05, 06 and 07 are being observed. Absence of an A pulse from any set observed indicates an open circuit in the transformer circuit of one of the 8M28 plug-ins (between pins 33 and 36). Absence of the gating pulse indicates a bad output from the 8M24 plug-in. See listing below:

CS Selected	Pin on 8M24 Selected
00, 04	30
01, 05	35
02, 06	27
03, 07	24

Before replacing an 8M24 plug-in that is suspected of being defective, see Section 5.7.4.1.1.2.3 for an addressing problem.

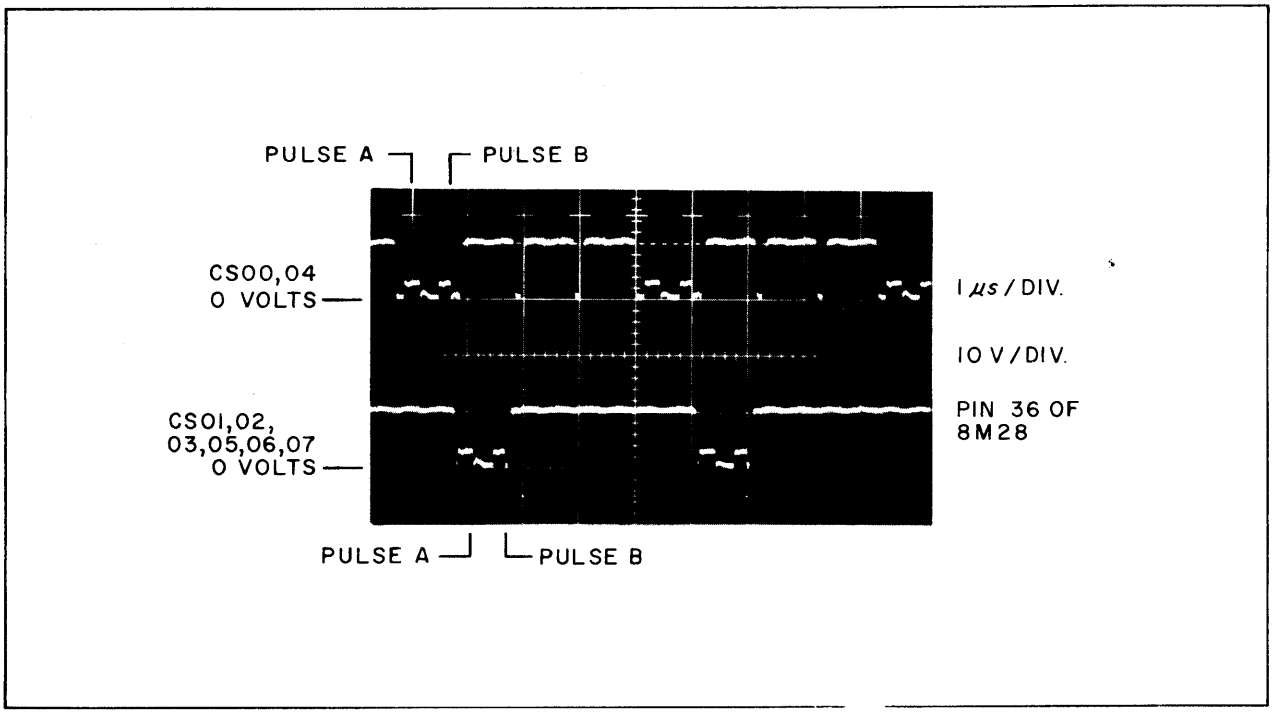


Figure 5-44. Y Current Switch Decoding

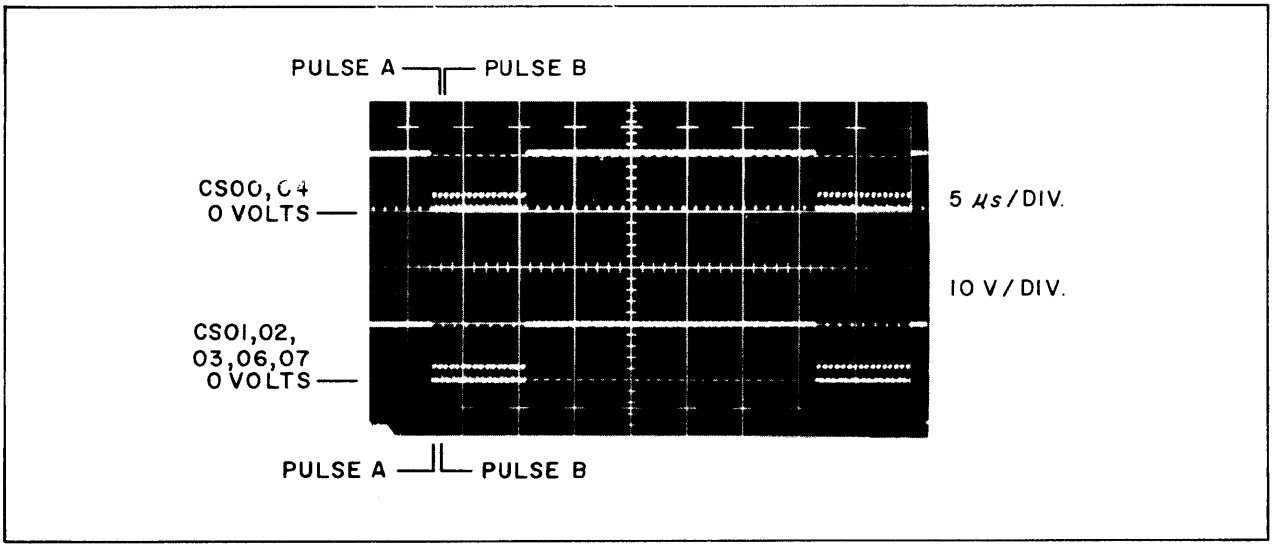


Figure 5-45. X Current Switch Decoding

5.7.4.1.1.2.2 Check 8M33

A double selection of the voltage switches will not, in most cases, be detected while observing the current source output at pin 206 of the 8M31. The output of each voltage switch is connected to two pins of the 8M33 plug-in. Common pin pairs are 3 and 22, 4 and 21, 12 and 23, 19 and 30. Because the top and bottom parts of the plug-in have identical signal pins, the output voltage switch pins can be thought of as the one hundred series or the two hundred series; i.e., 103 or 203. Therefore, assuming there is no connection problem or seating problem with the plug-in, each voltage switch output could be observed on any one of the two pins. See the logic sheets for the pins that are actually wires to the current switches.

Figures 5-42 and 5-43 show the correct timing for the voltage switch selection while writing information into the memory. For a partial scan of memory the timing will change accordingly. A comparison of voltage switches between stacks could be used as a guide by the serviceman for timing comparisons.

Before replacing an 8M33 plug-in that is suspected of being defective, see Section 5.7.4.1.1.2.3 for the addressing check.

5.7.4.1.1.2.3 Addressing Information Problem

A problem involving addressing of the memory word drive lines will not, in most cases, be detected while observing the current source output at pin 206 of the 8M31.

Begin the observations for presence of the addressing information at the input pins to the 8M24 and 8M33 plug-ins on the MM1S platters and the 8M20 and 8M22 on the MM5C platters. Missing address bits should be located by a series of observations beginning at the input of the memory address registers.

5.7.4.1.2 Full Word

A full word problem can be caused by the following conditions:

1. Absence of the +30 and/or +50 volt supplies at the bus distribution bar of the door containing the memory stacks (drop error).

2. Failure of the PFA signal at pin 226 of the 8M31 plug-ins (drop error). Also see Section 5.7.4.1.1.1.1.1.

3. Absence of the marginal check voltage from the MM3C and MM4C platters (pick-up error).

4. Absence of the inhibit command from the MM5C platter (pick-up error).

5. Absence of the X read, X write, Y read, or Y write commands from the MM1S platters (drop error).

6. Absence of the strobe commands at the sense amplifier pins 205 (drop error).

The PFA signal originates in the power supply and the marginal check voltage originates on the maintenance panel.

5.7.4.2 Single Bit Problem

Determine if the error is caused by a single bit or several bits. If the errors are caused by a single bit, determine if the errors are associated with a single address or multiple addresses in a full bank or half bank. If the errors are not caused by a single bit, then determine if the errors are associated with a half word or full word. Or determine whether the bits are random and/or failing at random addresses.

5.7.4.2.1 Multiple Addresses Half Bank

Determine if the error is associated with sense amplifier decoding or inhibit decoding. See section 5.4 for decoding information. A sense amplifier can be involved with a "pickup" or "drop" problem but an inhibit driver is usually involved with a "pickup" problem only.

5.7.4.2.1.1 Sense Amplifier/Sense Lines

Replace the sense amplifier if the symptoms indicate a weak or bad sense pre-amplifier. If the problem still persists, measure all the sense line pairs of both sense amplifiers of the problem bit. The possibility exists that an open or partially open sense line in one half bank can cause errors (especially "pickup") in the other half bank. The sense lines should measure approximately 27.0 ohms on a Simpson 260 volt-ohmmeter on the RX1 scale. A comparison of readings of the sense lines in the same bank regardless of the bit, should not vary by more than one or two ohms. (The specifications for the sense lines specify a resistance of 27.5 ohms, $\pm$13%. The one-to-two ohm variation in resistance and the 27.0 ohm nominal value are rule of thumb resistance values for the sense lines. Make rule of thumb measurements with the sense amplifier installed)

A high or low sense line reading is a problem. If the sense line reading is low, there is a possibility that the sense line is shorted to an inhibit line or drive line in the stack. If the sense line reading is high, the probable cause could be a 75-pin connector (P5 or P6) problem on the stack. The wires coming from the stack to the 75-pin connector might not be making a good connection. If any wire-to-pin connection on the 75-pin connector does not form a short circuit connection, the wire should be soldered to the pin. To improve the connection, the insulation of the wire can be removed by holding a hot soldering iron against the wire for a few seconds and melting solder on the wire and the pin. This is an emergency repair which should be reported to the site manager. If a solder connection from the wire to the pin does not repair the open or high resistance sense lines, then the problem is not repairable in the field; the stack should be replaced.

A sense line with a high resistance short to an inhibit or drive line cannot always be detected by a resistance measurement. The sense line or sense lines suspected should be observed with a scope equipped with a differential preamplifier to detect any excess noise present on the sense lines. See Figures 5-46 and 5-47 for normal waveforms. Excessive noise coupling into the sense lines can best be determined by observing the "zeros" signal

on the sense lines while writing all "zeros" into the memory. Figure 5-47 shows the typical noise pattern that is expected while viewing the sense lines with a differential measuring scope. If the noise pattern is high, check the balance of the measuring instruments by connecting both scope probes on the same sense line pin. An excessive amount of noise on the scope (a noise pattern greater than Figure 5-47) indicates an unbalance in the scope or in the scope probes used.

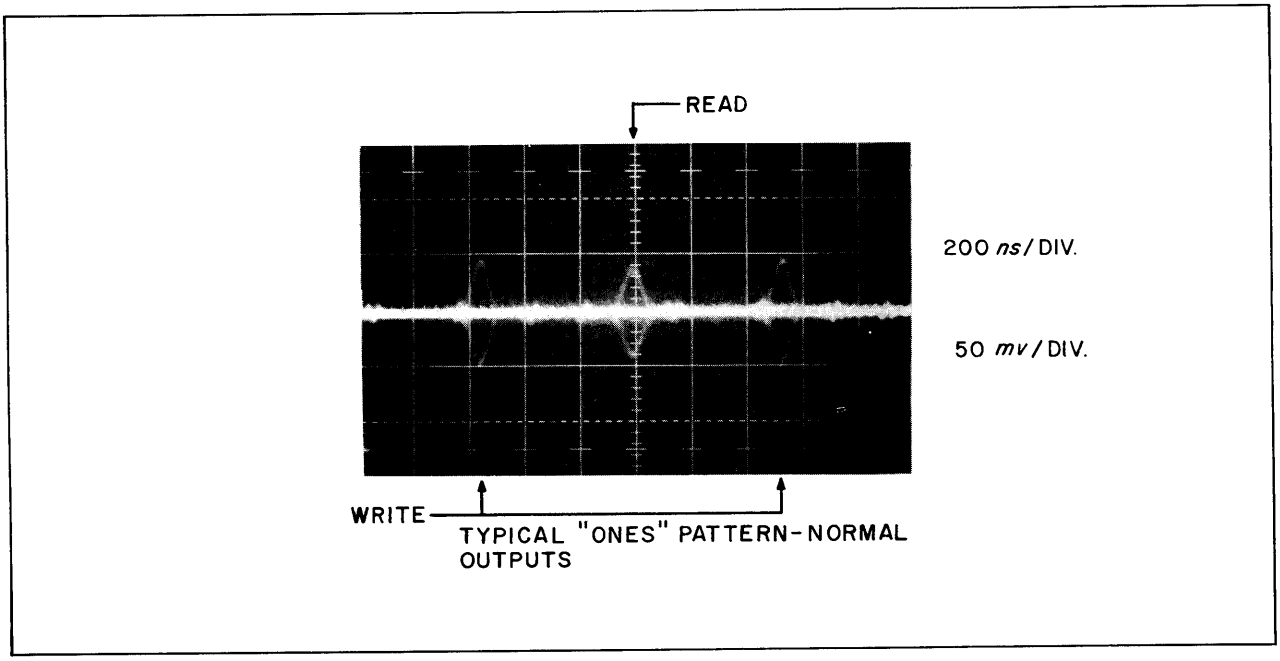


Figure 5-46. Sense Signal (Ones)

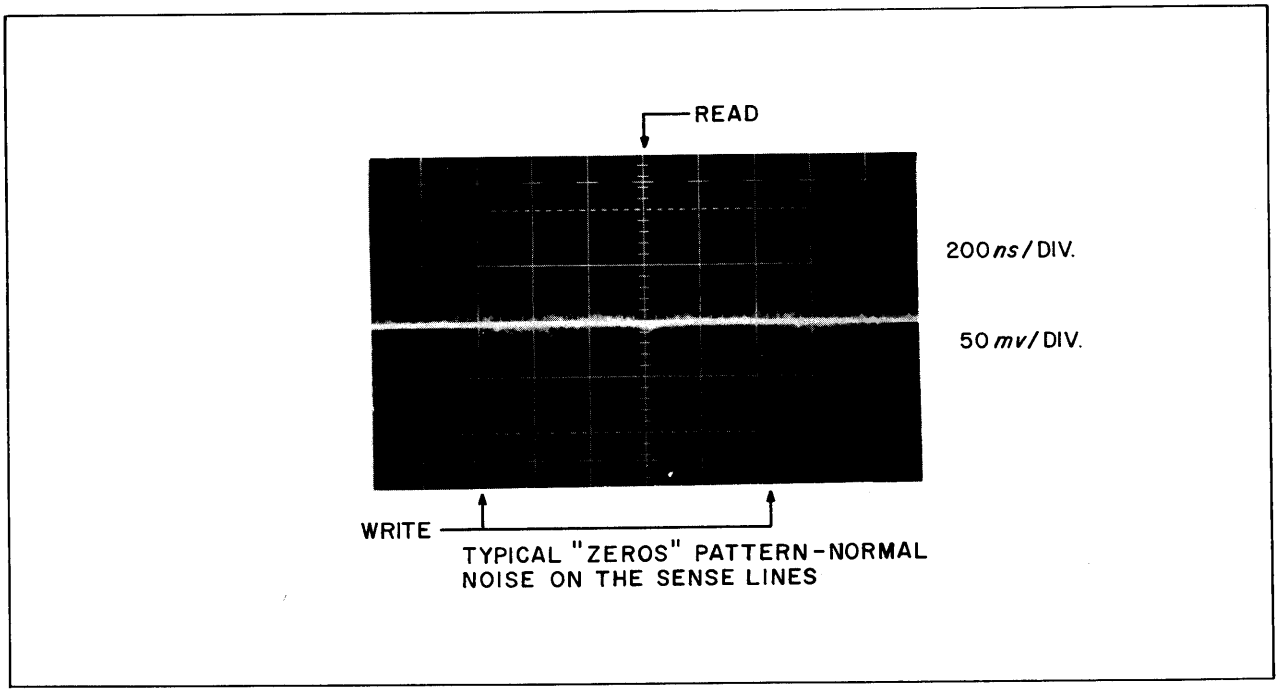


Figure 5-47. Sense Signal (Zeros)

Noise coupling can be caused by the inhibit currents (coupling during the write part of the cycle), Y read currents (coupling during the read part of the cycle, approximately 75 nanoseconds before the normal core output), X read currents (coupling during the read part of the cycle and during the normal core output time) and X and Y write currents (coupling during the write part of the cycle).

5.7.4.2.1.2 Inhibit Check

Observe all inhibit (eight total) outputs for the bit involved. If all four inhibit lines ar at d-c ground for any one plug-in, then the +30 volt fuse on the plug-in is open -- change the fuse. A bad output indicates a bad 8M21 plug-in. See Figures 5-48 and 5-50 for the normal voltage waveform for an inhibit output pin. An open inhibit line will be detected by a square wave pulse from +30 volts to ground. See Figure 5-49 for an inhibit voltage waveform resulting from an open inhibit line. If an open inhibit line is traced to a memory stack, then the stack should be replaced.

5.7.4.2.2 Single Address

A single address error of a single bit indicates a bad core output. Perform a continuous write "ones" into the failed address and observe the core output using a differential preamp on the scope. Trigger the scope from some internal signal in the memory such as MM3C 12AD-6 (RD1-RD2-P) and compare the problem bit with another bit. If the bit is even then it should be compared with even bits and vice versa because the polarities will be the same. The peak of the cores should not be more than 12 or 13 nanoseconds apart and the core amplitude should not be below 22 millivolts. No output will be observed if the core is missing.

A stack that has marginal range problems because of out-of-specification cores should be replaced.

5.7.4.2.3 Multiple Addresses Full Bank Problem

This type of problem should be traced to the same numbered sense lines in both half banks which are common to the same sense amplifier. The most likely problem would be a bad or weak sense amplifier. Determine the bad sense amplifier plug-in (see decoding in Section 5.4) and change it. If the problem is still present, see Section 5.7.4.2.1.1.

5.7.4.3 Half Word Problem

Determine if the problem is associated with X or Y current or voltage switches. See Section 5.4 for decoding information.

A random half word drop problem; i.e., a half word drop which alternates between stacks and/or half banks could be associated with a problem in the PFA signal. In such a case see paragraph 5.7.4.1.1.1.1.1 of this section.

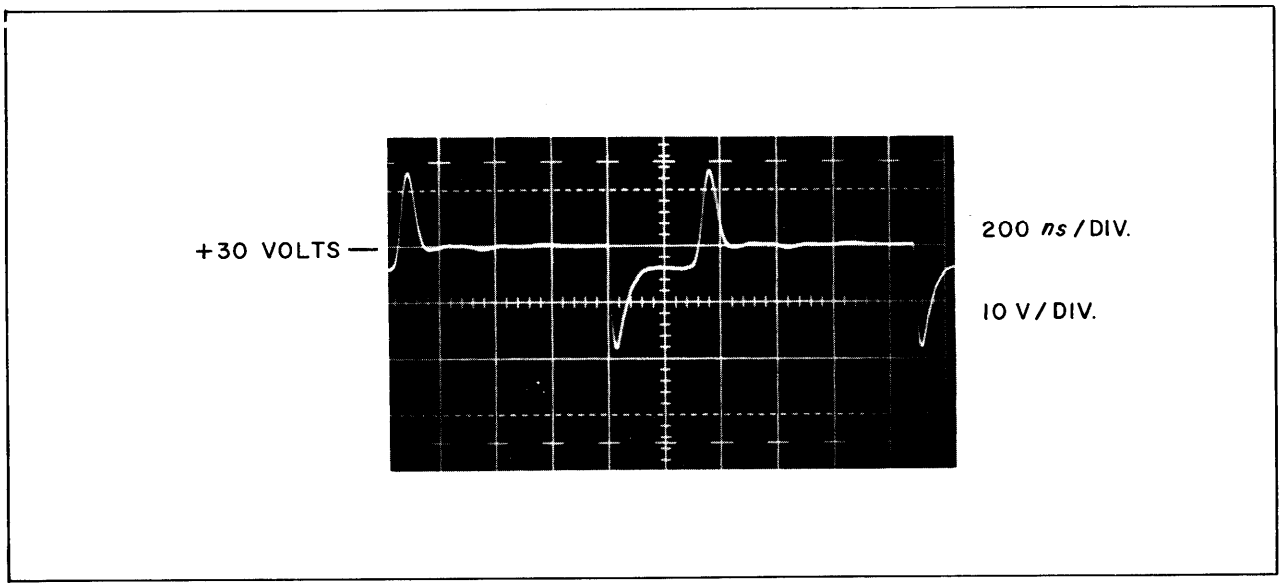


Figure 5-48. Inhibit Voltage - Normal

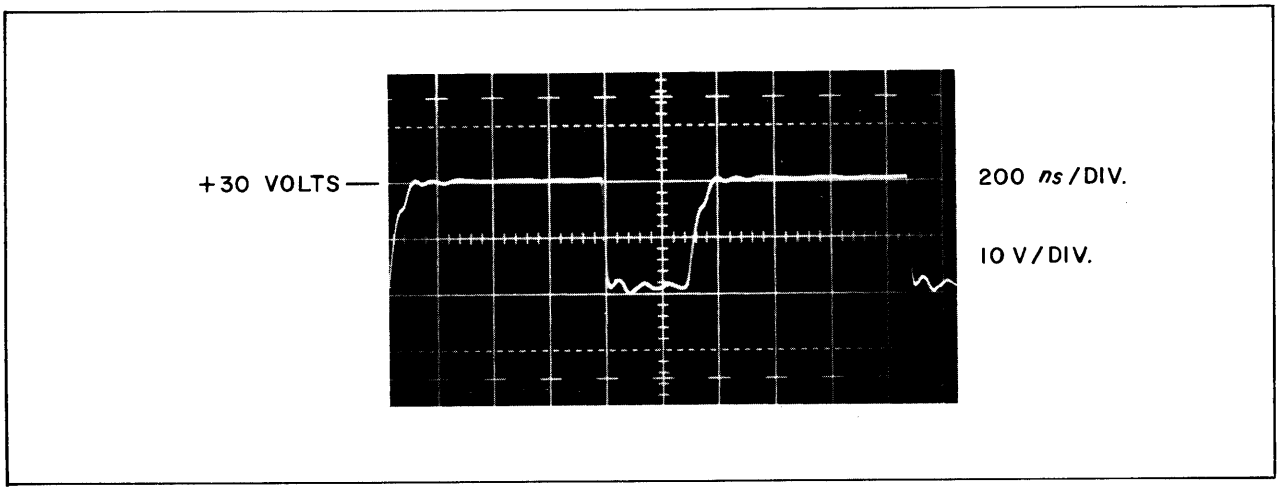


Figure 5-49. Inhibit Voltage - Open Inhibit Line

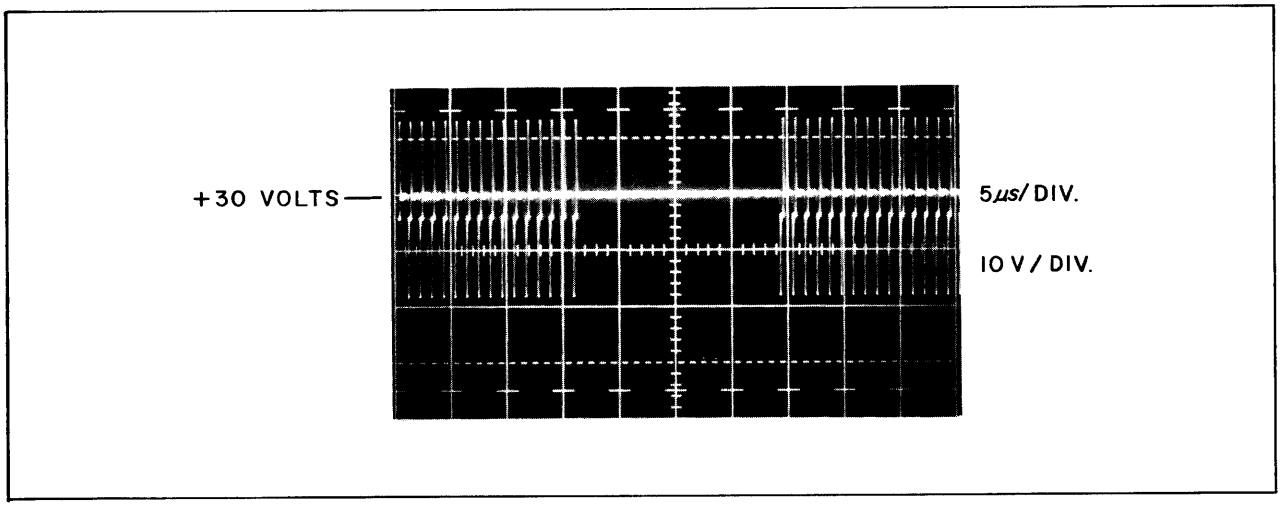


Figure 5-50. Inhibit Voltage - Normal

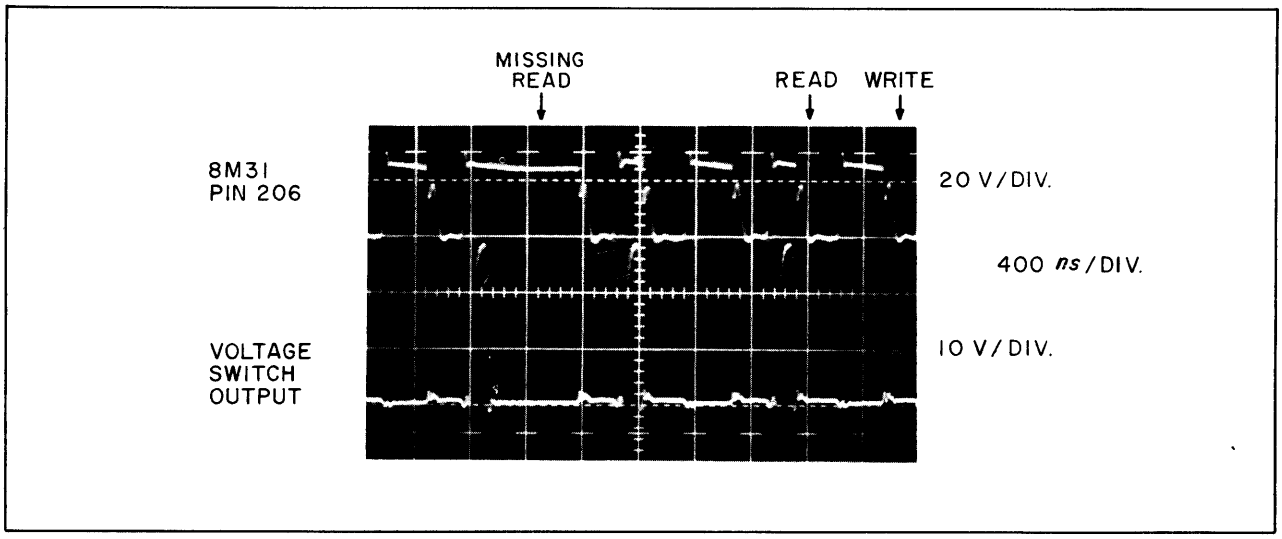


Figure 5-51. Missing Y Read Current Pulse

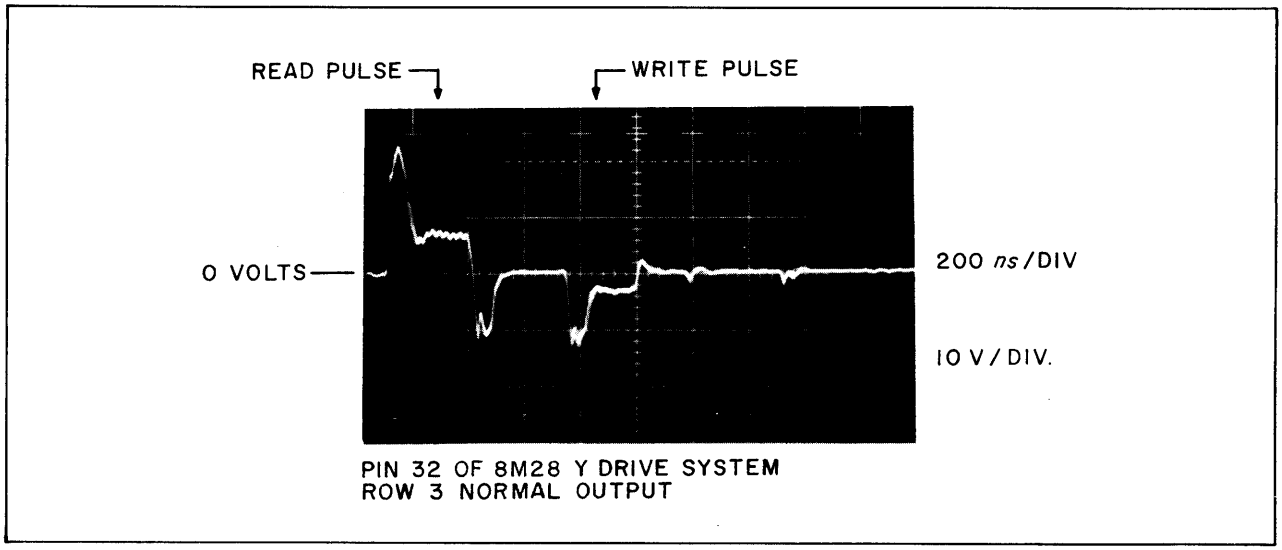


Figure 5-52. Normal Output of Y Current Switch

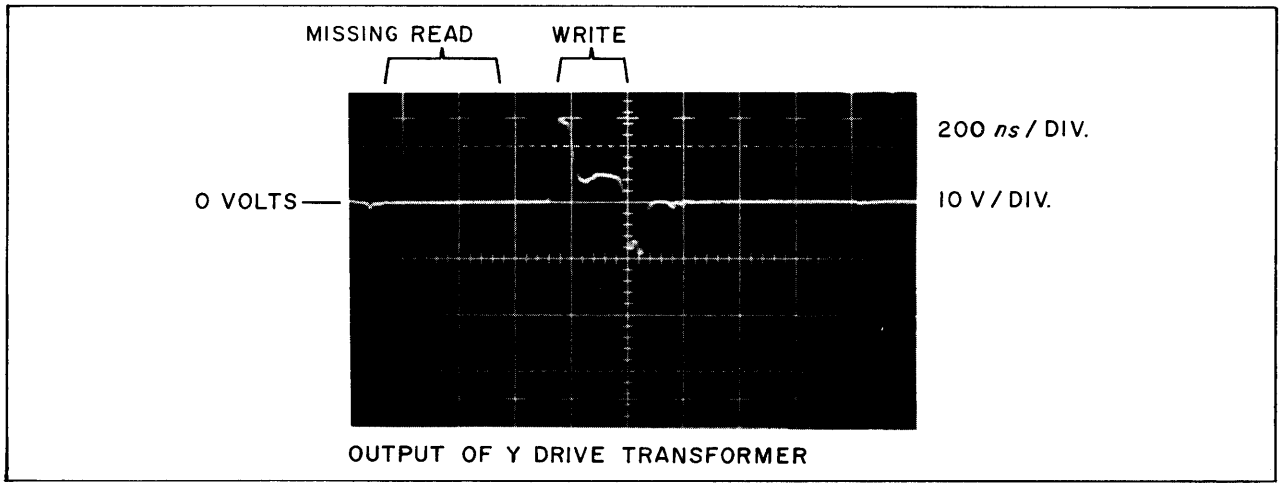


Figure 5-53. Missing Y Read Current Pulse

5.7.4.3.1 Error Addresses Common To Y Current Switch Decoding

Observe the voltage waveform at the output of the Y current source (8M31 plug-in, pin 206). Absence of the read or write pulse indicates a bad 8M28 plug-in, see Figure 5-51. To determine the defective 8M28 plug-in, internally sync the scope and observe the output of the 8M28 plug-ins on pin 32 of row three. Figure 5-52 shows a normal output for the Y drive system. Absence of the read pulses indicates a defective 8M28 in row three or an open circuit from pin 32 of row three to pin five of row six. Absence of the write pulses indicates a defective 8M28 in row six or an open circuit from pin 32 in row six to pin five in row three. Figure 5-53 shows a missing Y read current at the 8M28 drive transformer output.

If a waveform such as Figure 5-54 is observed, then the problem is an open drive line or a defective 8M28 plug-in. Figure 5-55 shows an open Y drive line as viewed from pin 206 of the 8M31 plug-in (scope triggered by a voltage switch). Figure 5-56 shows the normal voltage waveform at the output of the 8M28 Y drive transformers and Figure 5-57 shows an open Y drive line.

The Y drive system is different from the X drive system in two ways: The Y read pulse is approximately 75 nanoseconds wider than the X read pulse; and the computer programs all eight Y current switches for every one X current switch. As a result of the difference in the programming of the X and Y current switches, every X current switch will be displayed for eight consecutive counts in contrast to the one-of-eight display of the Y current switches.

5.7.4.3.2 Error Addresses Common To X Current Switch Decoding

Observe the voltage waveform at the output of the X current source (8M31 plug-in, pin 206). Absence of the read or write pulse indicates a bad 8M28 plug-in, see Figures 5-58 and 5-59. To determine the 8M28 plug-in involved, internally trigger on the scope and observe the output of the 8M28 plug-ins on pin 32 of row nine. Absence of the read pulses indicate a defective 8M28 in row nine or an open circuit from pin 32 of row nine to pin five or row twelve. Absence of the write pulses indicate a defective 8M28 in row twelve or an open circuit from pin 32 in row twelve to pin five in row nine. Figure 5-59 shows a missing X read pulse.

If a waveform such as Figure 5-54 is observed, then the problem is an open drive line or a defective 8M28 plug-in. Observe the voltage at the outputs of all the drive transformers of the 8M28 being observed and the plug-in in the row below. Figure 5-60 shows an open X drive line.

5.7.4.3.3 Error Addresses Common To X Voltage Switch Decoding

Observe all voltage switch outputs. See Figures 5-34 and 5-43 for typical X voltage switch outputs. Replace any defective plug-ins. Keep in mind that platter connections are not beyond suspicion; if no problem is found, make certain that voltage switch outputs are at the 8M28 current switch pins.

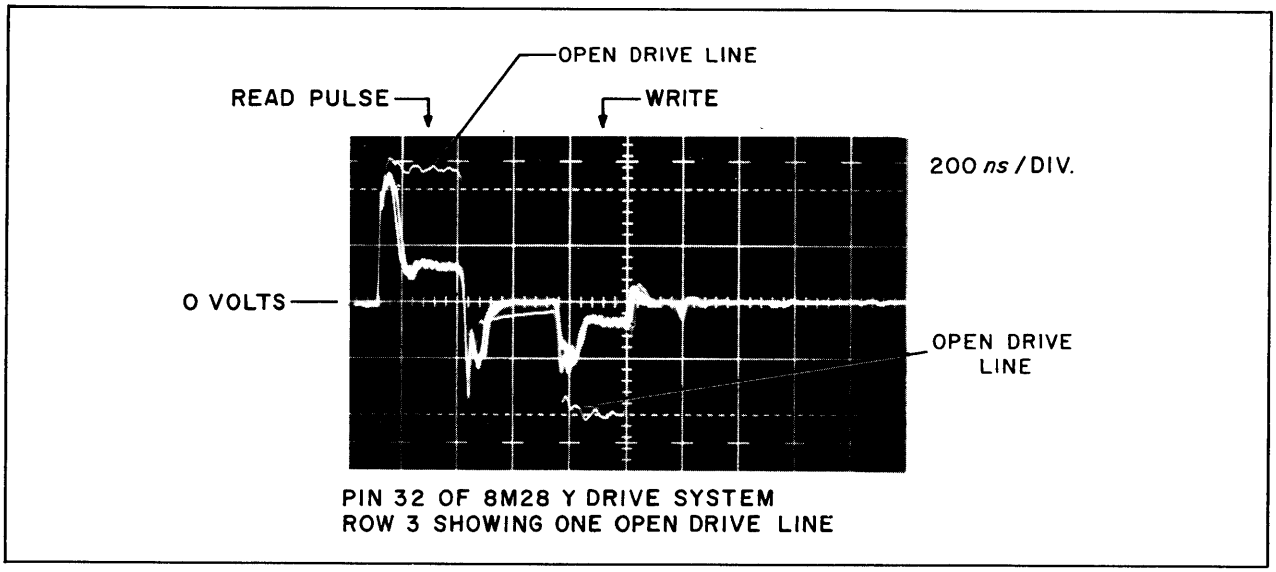


Figure 5-54. Open Y Drive Line

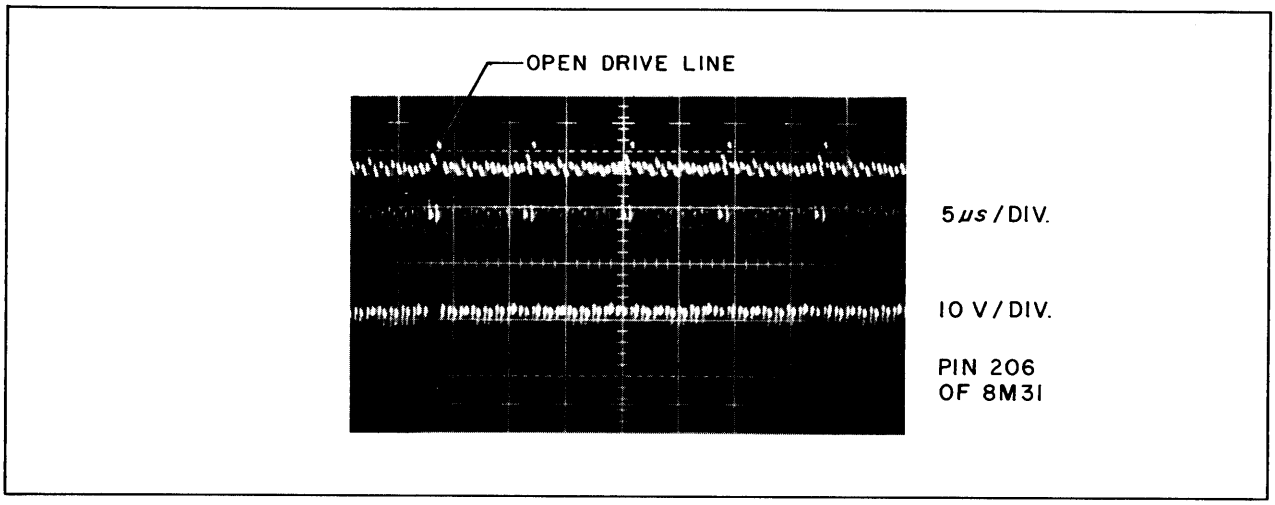


Figure 5-55. Open Y Drive Line

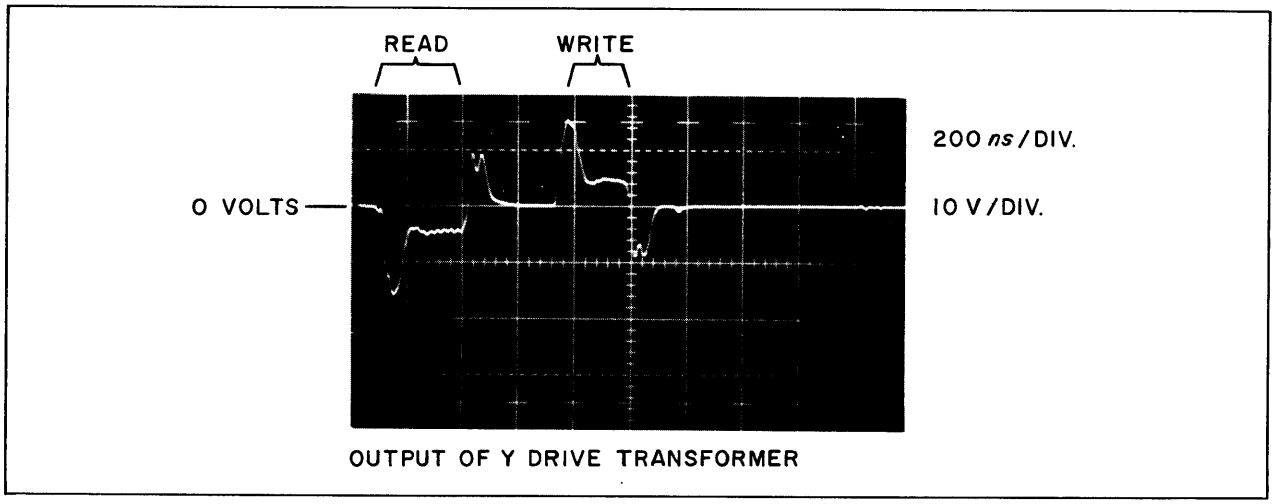


Figure 5-56. Normal Y Read/Write Current Pulses

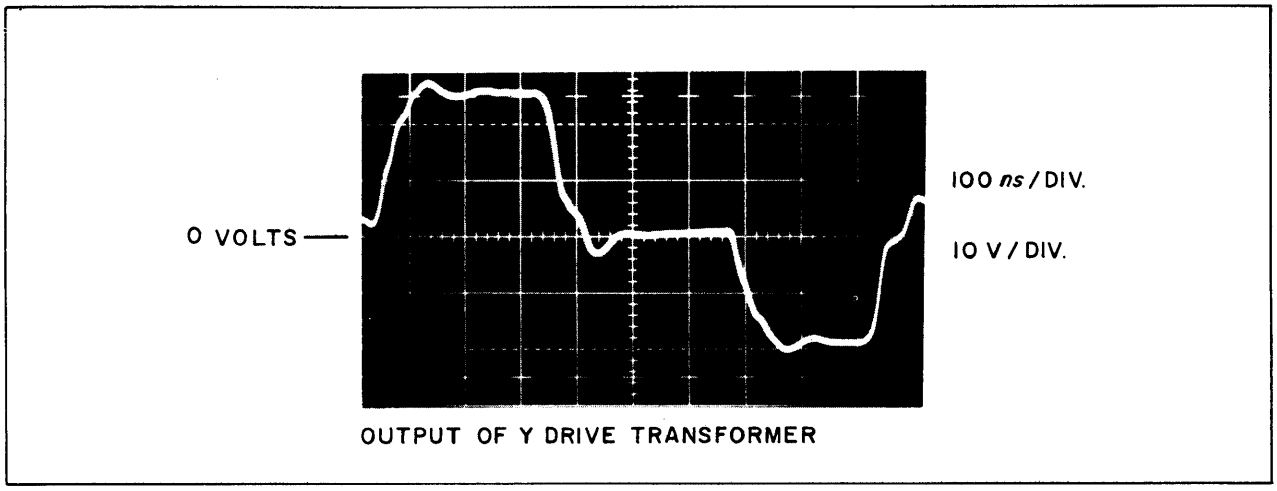


Figure 5-57. Open Y Drive Line

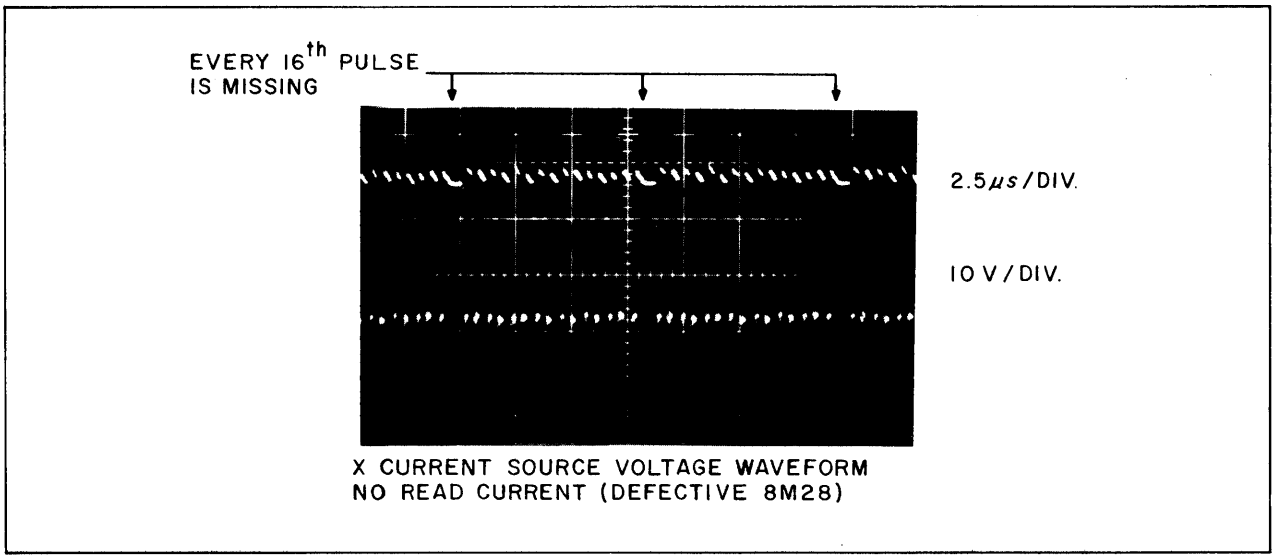


Figure 5-58. Missing X Read Current Pulse

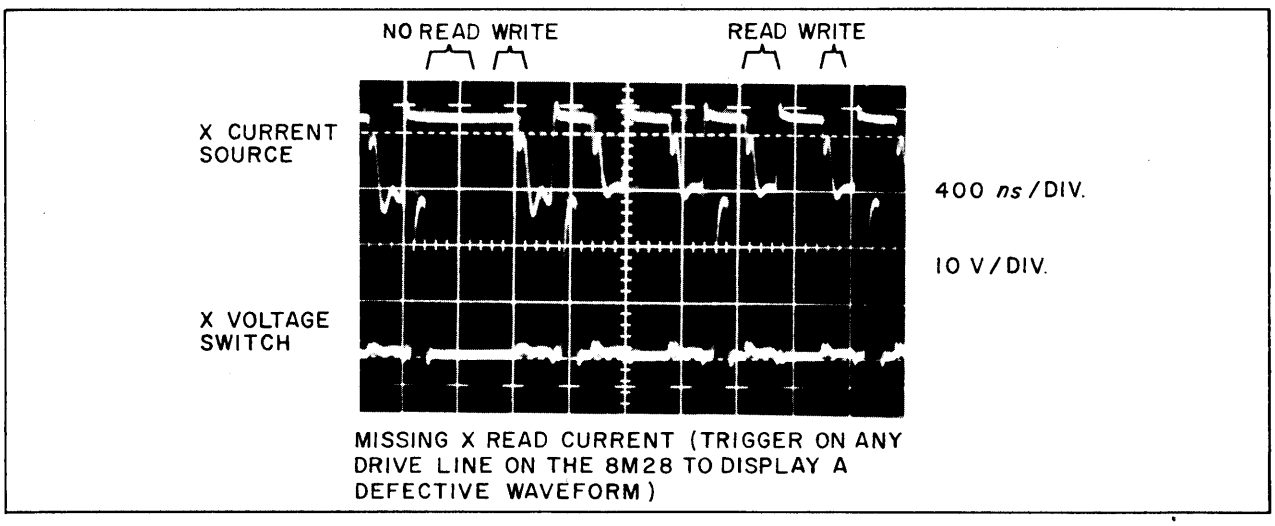


Figure 5-59. Missing X Read Current Pulse

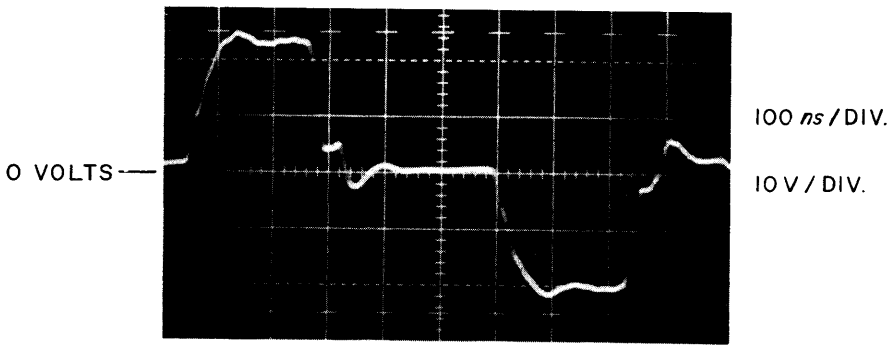


Figure 5-60. Open X Drive Line

5.7.4.3.4 Error Addresses Common To Y Voltage Switch Decoding

Observe all voltage switch outputs. See Figures 5-33 and 5-42 for typical Y voltage switch outputs. Replace any defective plug-ins. Keep in mind that platter connections are not beyond suspicion; if no problem is found, make certain that voltage switch outputs are at the 8M28 current switch pins.

5.7.4.3.5 Error Addresses Not Common To X Or Y Decoding

Investigate the addresses where the errors occur to determine that none of the current or voltage switches are involved.

5.7.4.3.5.1 Inhibit Decoding Problem

The error could be a full word or half-word and a pickup or drop problem. In addition, the error might be difficult to detect insofar as inhibit decoding is concerned. The inhibit command could be missing causing a constant pickup or drop, depending upon the logic voltage level at the MM5C platter. See Figures 5-48 and 5-50 for the normal inhibit voltage waveform at the 8M21 plug-ins. Figure 5-49 shows an inhibit voltage waveform resulting from an open inhibit line.

Investigate memory address and inhibit command inputs to and the outputs from the inhibit decoders. The addressing bits are decoded by the 8M20 plug-ins and the inhibit commands and data are decoded by the 8M22 plug-ins. See Figures 5-61 through 5-66 for decoder output signals while driving the Inhibit Driver plug-ins (8M21).

5.7.4.3.5.2 PFA Signal Problem

See Section 5.7.4.1.1.1.1.1 for a description of the Power Failure Alarm problem.

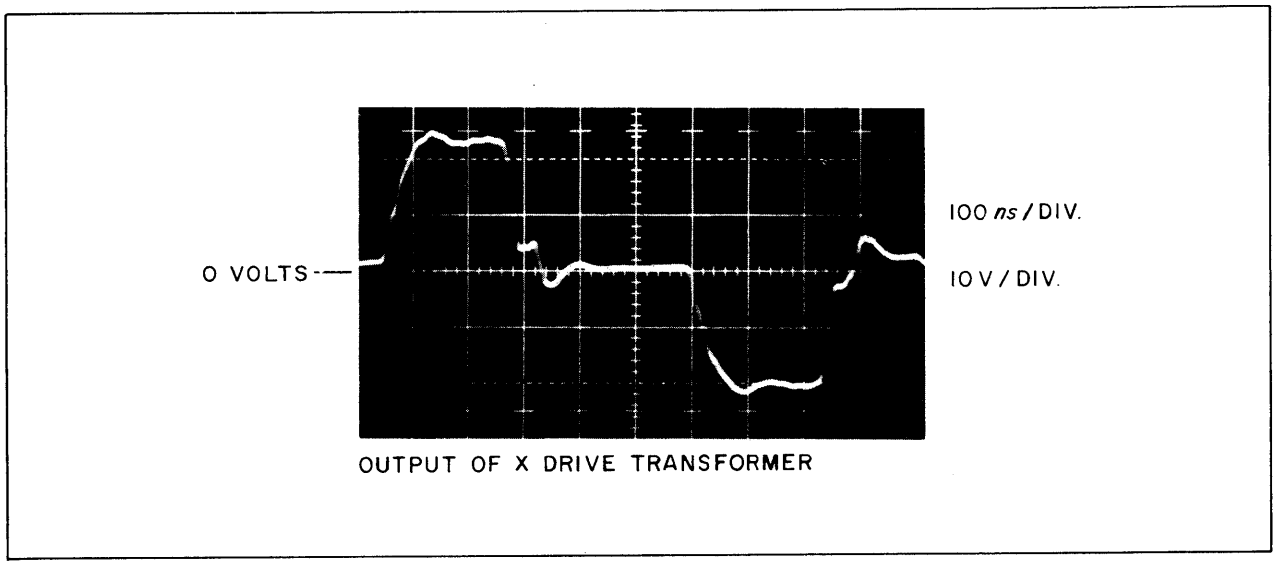


Figure 5-60. Open X Drive Line

5.7.4.3.4 Error Addresses Common To Y Voltage Switch Decoding

Observe all voltage switch outputs. See Figures 5-33 and 5-42 for typical Y voltage switch outputs. Replace any defective plug-ins. Keep in mind that platter connections are not beyond suspicion; if no problem is found, make certain that voltage switch outputs are at the 8M28 current switch pins.

5.7.4.3.5 Error Addresses Not Common To X Or Y Decoding

Investigate the addresses where the errors occur to determine that none of the current or voltage switches are involved.

5.7.4.3.5.1 Inhibit Decoding Problem

The error could be a full word or half-word and a pickup or drop problem. In addition, the error might be difficult to detect insofar as inhibit decoding is concerned. The inhibit command could be missing causing a constant pickup or drop, depending upon the logic voltage level at the MM5C platter. See Figures 5-48 and 5-50 for the normal inhibit voltage waveform at the 8M21 plug-ins. Figure 5-49 shows an inhibit voltage waveform resulting from an open inhibit line.

Investigate memory address and inhibit command inputs to and the outputs from the inhibit decoders. The addressing bits are decoded by the 8M20 plug-ins and the inhibit commands and data are decoded by the 8M22 plug-ins. See Figures 5-61 through 5-66 for decoder output signals while driving the Inhibit Driver plug-ins (8M21).

5.7.4.3.5.2 (Deleted)

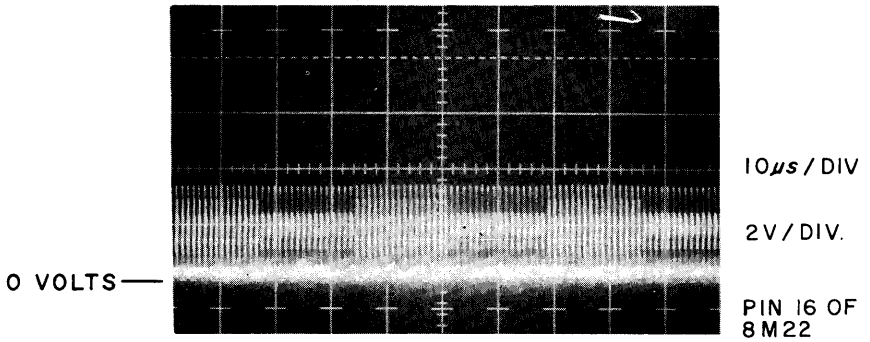


Figure 5-61. Inhibit Emitter Decoder (INE)

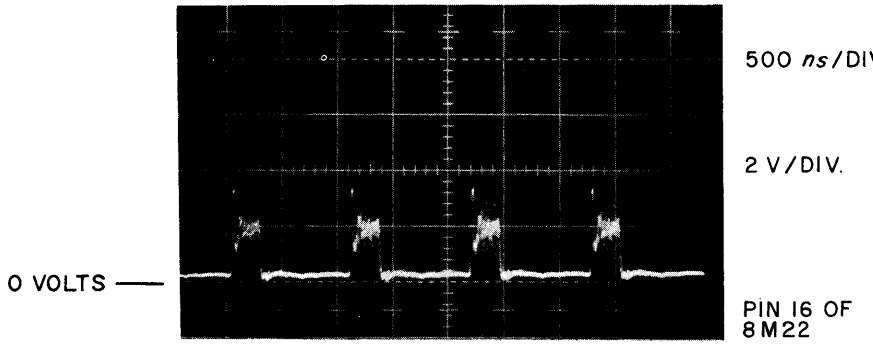


Figure 5-62. Inhibit Emitter Decoder (INE)

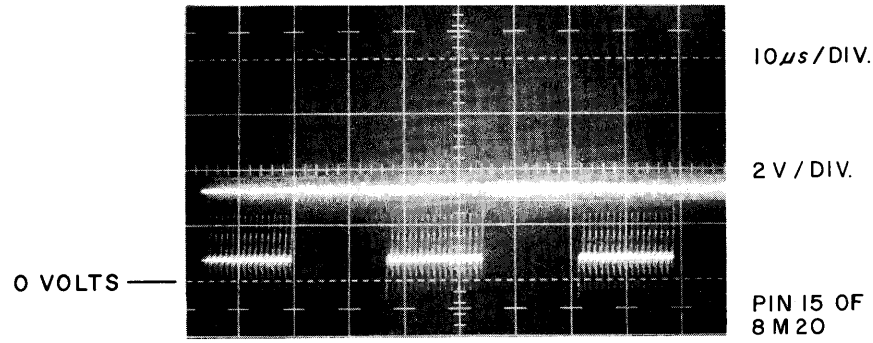


Figure 5-63. Inhibit Base Decoder (INB)

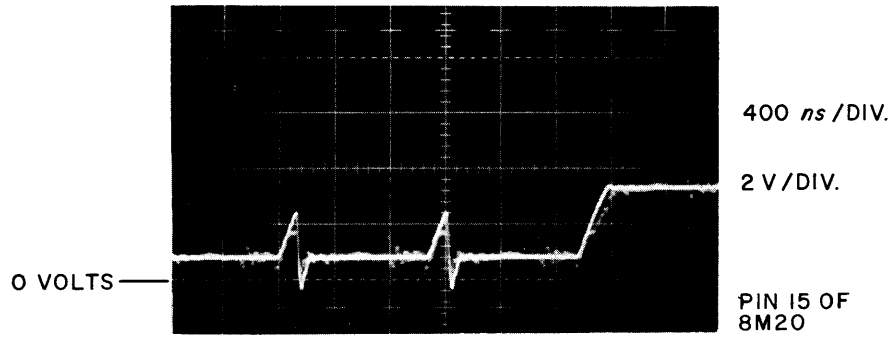


Figure 5-64. Inhibit Base Decoder (INB)

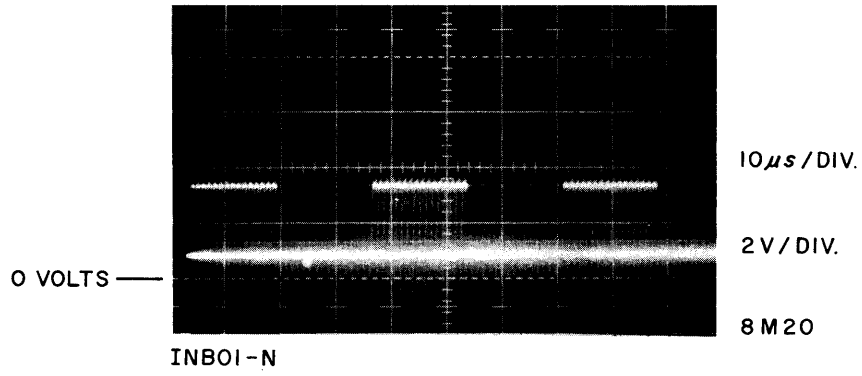


Figure 5-65. Inhibit Base Decoder (INB)

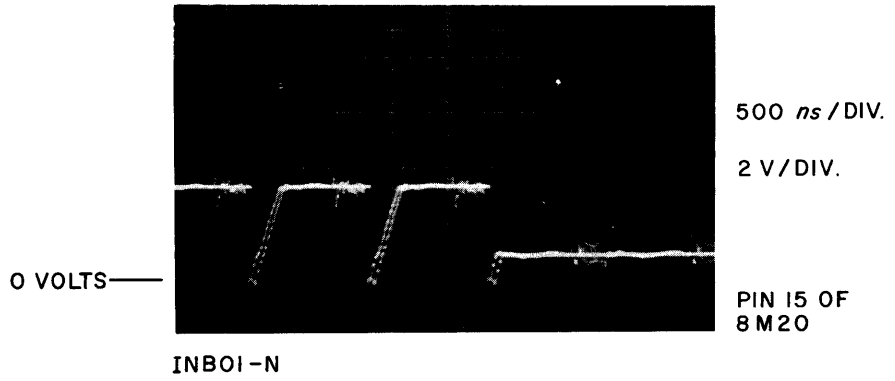


Figure 5-66. Inhibit Base Decoder (INB)

5.7.4.3.5.3 Marginal Check Voltage Problem

The MM3C and MM4C platters have the same marginal check voltages. However, the voltages must be routed through edge connectors on each platter. In the event the marginal check voltage is not present on any one platter, the bits associated with that platter (00 through 16 for the MM4C and 17 through 32 for the MM3C) will have a tendency to pick-up bits at the nominal marginal voltage (+10.0 volts). The best place to test for the marginal voltage is pin 135 of the 8M32 plug-ins on the platter involved.

5.7.4.3.5.4 Drive Current Problems

Drive current problems are the result of two primary causes: defective plug-ins in the drive system and open drive lines.

5.7.4.3.5.4.1 Drive Current Investigation

Observe the output voltage waveforms of the 8M31 current sources of the stack involved. On the MM1SR platter the Y current source is located at 3AC (8M31, pin 206) and the X current source at 9AC (8M31, pin 206). On the MM1SL platter the Y current source is located at 3BQ (8M31, pin 206) and the X current source at 9BQ (8M31, pin 206). See Figures 5-38 through 5-41 for satisfactory output voltage waveforms. Figure 5-55 shows an open Y drive line as viewed at the current source and Figure 5-54 shows the same open Y drive line as viewed at pin 32 of an 8M28 plug-in. If several pulses are distorted and/or missing from the 8M31 output, see Sections 5.7.4.1.1.1 and 5.7.4.1.1.1.1 for an investigative procedure of the drive system.

5.7.4.4 Full Word Problem

A full word problem, either drop or pickup, is usually associated with a d-c voltage, addressing or control logic problems.

5.7.4.4.1 Investigate Memory Operating Signals

The BPU requires "accept (ACP1-P)" and "memory present (MP1-P)" signals each time an "execute (EX1-P)" command is sent. If the BPU fails to receive either one of the required signals, then a malfunction will occur. The regeneration (REG1-P) signal from the BPU permits the memory to write whatever information is present in the memory register. Absence of the "regenerate" signal or failure of the logic chain in the memory could cause a full word problem. Also, absence of the "permit strobe (PS-1)" signal will cause a full word problem error.

See Section 5.3 for the complete listing of the BPU Memory interface signals.

5.7.4.4.2 Measure All D.C. Platter Voltages

Measure all voltages on the memory platters to be certain that all voltage connections are secure. Measure the PFA signal, see Section 5.7.4.1.1.1.1.1.

5.7.4.4.3 Investigate Data And/Or Address Logic Chain

See Section 5.4 for data and memory address interface information.

5.7.5 WRITING AND/OR READING MEMORY DATA

To preset, clear or read Main Memory.

1. Set MESP Switch
2. Set ICSP Switch
3. Set CC Switch
4. Press GEN RES Switch
5. Press STL Reset Switch
6. Set DIS SPA Switch
7. Set SPA Display Equal to $(0D)_{16}$
8. Reset DIS SPA Switch
9. Set STL Display Equal to $(25)_{16}$
10. Set "N" Counter (Least) Equal to $(01)_{16}$
11. Set OPR Equal to $(D0)_{16}$ for Write and $(D8)_{16}$ for Read, also set GPM & GPL $\neq 0$
12. Write data to be written into Main Memory into Fast Memory location $(01)_{16}$

    In the case of a Read F.M. LOC (01) will contain the data from the previous read.
13. Write the Main Memory starting address into F.M. location $(07)_{16}$ - usually zero.
14. Press Start

NOTES: The Processor will stop when the whole memory has been cycled once, except when AMI switch is set. In this case only one word address will be read/written and SFSP Switch must be set to stop the machine.

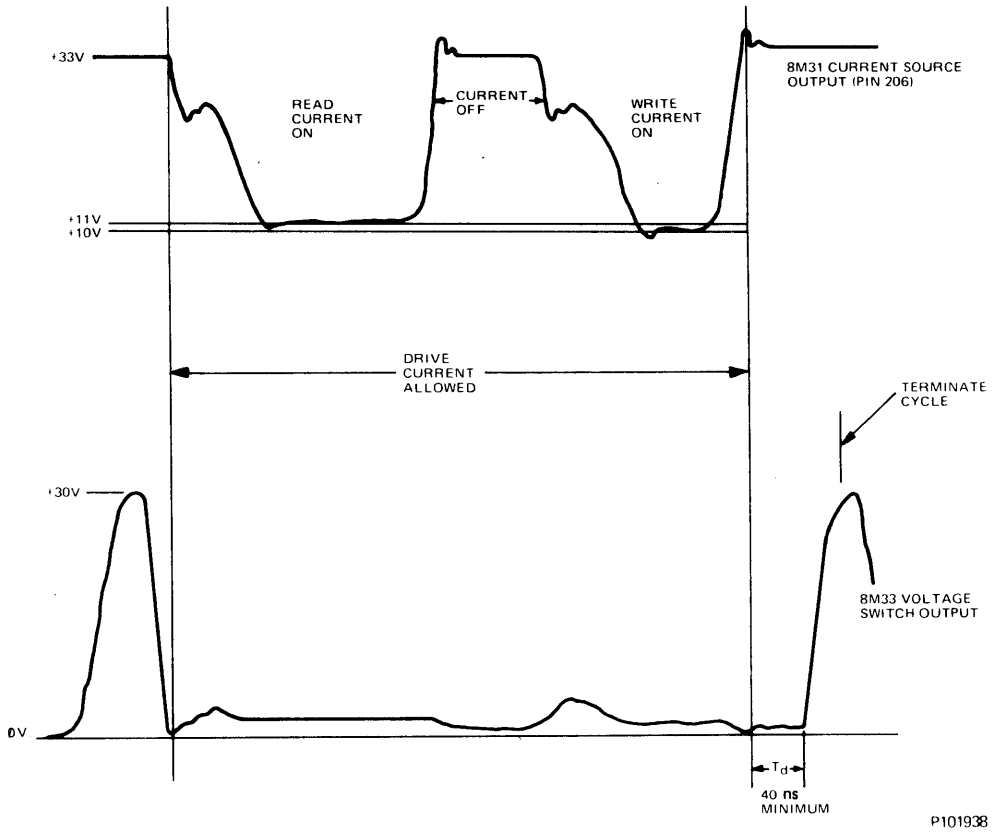


Figure 5-66A. Current Source and Voltage Switch Output

5.7.4.4 Full Word Problem

A full word problem, either drop or pickup, is usually associated with a d-c voltage, addressing or control logic problems.

5.7.4.4.1 Investigate Memory Operating Signals

The BPU requires "accept (ACP1-P)" and "memory present (MP1-P)" signals each time an "execute (EX1-P)" command is sent. If the BPU fails to receive either one of the required signals, then a malfunction will occur. The regeneration (REG1-P) signal from the BPU permits the memory to write whatever information is present in the memory register. Absence of the "regenerate" signal or failure of the logic chain in the memory could cause a full word problem. Also, absence of the "permit strobe (PS-1)" signal will cause a full word problem error.

See Section 5.3 for the complete listing of the BPU Memory interface signals.

5.7.4.4.2 Measure All D.C. Platter Voltages

Measure all voltages on the memory platters to be certain that all voltage connections are secure.

5.7.4.4.3 Investigate Data And/Or Address Logic Chain

See Section 5.4 for data and memory address interface information.

5.7.4.5 8M32-2 Causes Main Memory Parity Errors

The 8M32-2 Sense Amplifiers plug-ins may cause MMPE's. A visual check of these plug-ins will detect if the Sense Amplifier is the cause of MMPE's. The following procedure should be used when inspecting the 8M32-2 plug-ins:

1. Power down the Processor.

2. Remove one of the 8M32-2 plug-ins from the first bank.

3. Using a Jewelers Loupe (937347), visually ensure that the connections for resistors R6 and R16 are mechanically and electrically secure and that the solder has flowed through the connections correctly. The connections in question are those closest to the bottom edge of the board for resistors R6 and R16.

4. If the resistor connections do not appear to be soldered correctly (i.e. solder has not flowed, cold solder joint, etc.) solder the connections as per TIP General #43, Section 7.2.4.

5. Reinsert the plug-in in its original location. (Be sure plug-in is seated properly

6. Repeat procedure for the next 8M32-2 plug-in.

7. At the completion of inspection and/or soldering of all 8M32-2 plug-ins, power up Processor and run the appropriate memory diagnostic to check system.

   NOTE: All spare 8M32-2 plug-ins on site should also be inspected for correct soldering of R6 and R16.

5.7.5 WRITING AND/OR READING MEMORY DATA

To preset, clear or read Main Memory.

1. Set MESP switch.

2. Set ICSP switch.

3. Set CC switch.

4. Set INHADX switch if continuous cycling is desired.

5. Set AMI switch if continuous cycling of one word location is desired.

6. Press GEN RES switch.

7. Press STL Reset switch.

NOTES: (Continued)

If a Main Memory Parity Error (MMPE) is detected, during a read, the machine will stop and the memory address in error will be located in MAR (Reg. Select Switch) and the data in MR.

To recycle the machine after a MMPE, steps 4 through 14 must be repeated.

5.7.6 STACK REPLACEMENT

The main memory stack is the only component requiring special replacement instructions. It is NOT necessary to remove the MM1S platter to change the stack.

5.7.6.1 Removal

All cables to the stack must be disconnected before the stack can be removed. First, disconnect the four 75-pin connectors for the Inhibit windings (P1-P4) second, disconnect the two 75-pin connectors for the sense lines (P5 & P6), and third, carefully remove the sixteen drive line connectors (P7 to P22). Access to P19 through P22 is made available by removing the access plate on the side of the door. After all the cables are disconnected, remove the eight mounting bolts that hold the stack to the MM1S platter.

5.7.6.2 Replacement

Install a stack by reversing the procedure of 5.7.6.1 above. Note that P19 through P22 should be replaced before bolting in the stack where the access plate is not available.

5.7.6.3 Electrical Test

Test the stack by exercising it with Library Tape Block 705. See the Memory Margin Determination and Expansion Procedure for the marginal range requirements.

5.8 MEMORY MARGIN DETERMINATION AND EXPANSION PROCEDURE

5.8.1 EXERCISE MEMORY WITH LIBRARY TAPE BLOCK 705

The memory must operate without errors while being exercised by library tape block 705 over the voltage margins specified below. Each bank has its own set of relative strobe position (rsp) controls, therefore, each bank must be treated independently of any other bank. Refer to Figure 5-67.

5.8.2 SPECIFIED MARGIN VOLTAGE LIMITS

The voltage margins should be +7.0 through +14.5 volts (approximately -3.0 through +4.5 volts on the maintenance panel meter). Record the error address, bit and/or bits and the margin voltage at which the memory failed for both the high and the low end of the memory margin range.

2. If the stack to be replaced has provisions on it for a handle, unscrew the handle from the new stack and screw it onto the one in the frame. This provides a handle to hold the old stack. If the stack to be replaced is an older type and has no holes provided for a handle, you will have to use the palm of your hand to gently brace it while it is being removed. (Do not squeeze the planes of the stack together with your fingers.)

3. Carefully remove the connectors, being especially careful of the X and Y line connectors before loosening the mounting bolts.

4. Loosen the mounting bolts holding the stack onto the platter, and gently set the stack on a table (or on the floor away from the system, so that it won't be accidentally kicked, dropped, or mishandled.

5. Remove the handle and place it on the new stack.

6. Hold the new stack by the handle, and carefully remove it from the tote tray and set it in place on the platter.

7. Tighten the mounting bolts so that the stack is supported on the platter. Carefully insert the X and Y connectors, being sure they are well seated, and then install the Sense and Inhibit connectors.

8. Remove the handle from the newly installed stack. Retain the handle for future use, do not return with defective stack.

9. Run maintenance programs and check the bias. Record bias points and failed addresses for future reference. If the stack is in bank 1, run PB 700 series. For banks other than 1, PB 3010, 3020, 3030, and 3040 for the 70/55 are preferred. These program blocks will provide more information for troubleshooting.

10. If PB's run successfully, no further action is required; otherwise make the necessary adjustments accordingly.

5.7.7 DEFECTIVE WIRE-WOUND RESISTORS

Paragraphs 5.7.7.1 through 5.7.7.5 provide information on locating defective wire-wound resistors and obtaining replacement resistors.

5.7.7.1 General

Wire-wound resistors (drawing no. 8542350) with RCL markings may increase in resistance and cause circuit problems in 70/55 Processors. These resistors are identified by their dark color, axial leads, resistor bodies tapered from their center to their leads, and their RCL markings.

Other wire-wound resistors (drawing no. 8542350) without the RCL markings, used in the same processor circuits, have not caused many problems in the 70/55 Processors.

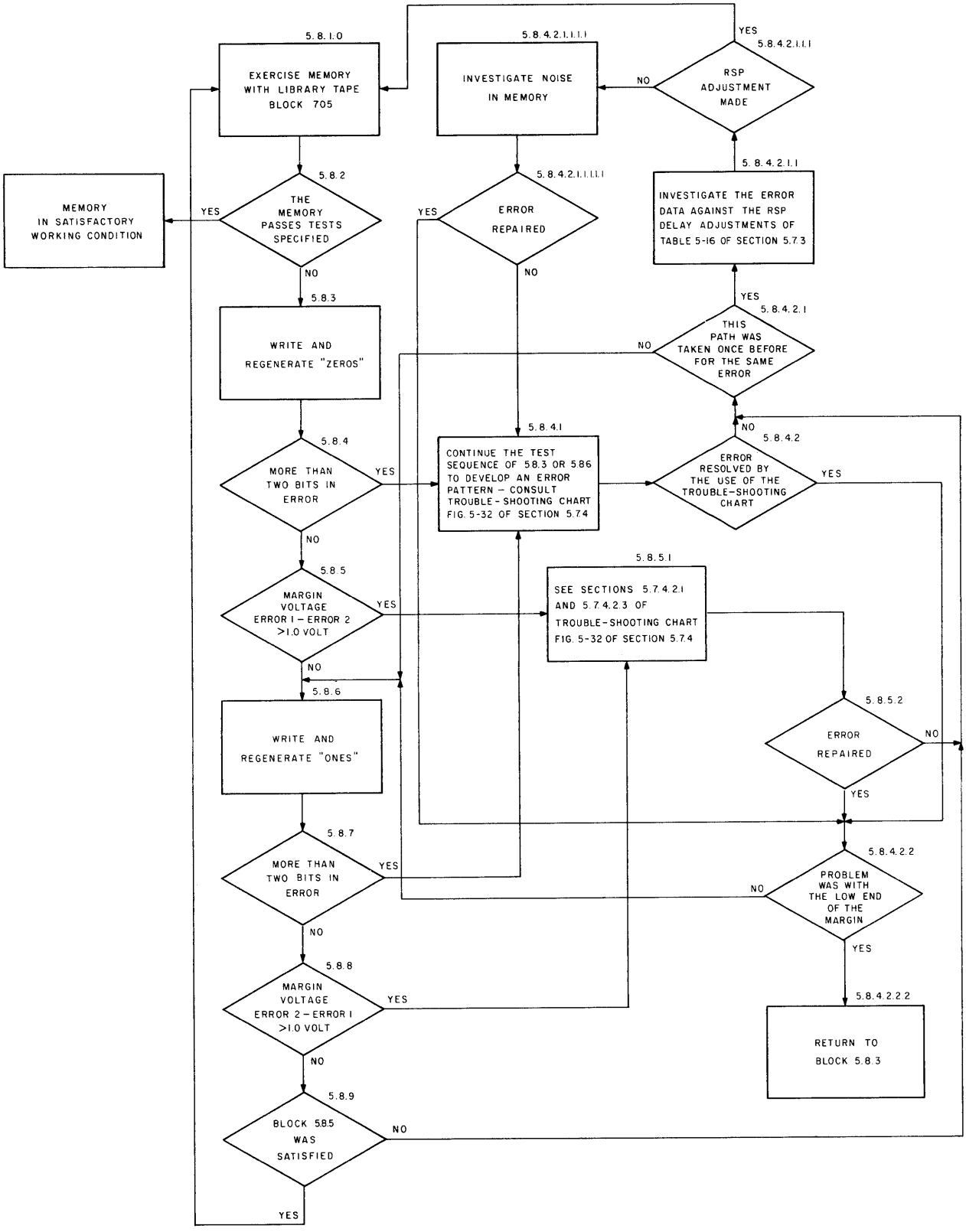


Figure 5-67. Marginal Range Expansion Flow Chart

faulty resistors which have doubled in value may be detected by an equally abnormal increase in the amplitudes of the signals from both the positive and negative drive line outputs, or by close examination for distortion of the signal output at pin 32 of the 8M28 plug-in assembly.

If resistor R2 or R25 on an 8M28 plug-in assembly is defective, the result is a hazy and distorted output on pin 32 when observed on an oscilloscope.

At the completion of the dynamic checks, power down the processor and remove all questionable plug-in assemblies.

Resistance measurements are now performed using a Simpson 260 multimeter or equivalent.

The following table showing the relationship between the drive line output pin numbers and their associated wire-wound resistors plus the 8M28 Data Sheets is used to determine the locations of questionable resistors.

PIN NUMBERS	ASSOCIATED RESISTORS
6, 8	R19, R20
7, 10	R17, R18
9, 11	R15, R16
13, 14	R13, R14
15, 16	R11, R12
17, 18	R9, R10
24, 25	R7, R8
26, 27	R5, R6
28, 29	R3, R4

A nominal reading of 75 ohms (two 150-ohm resistors in parallel) is normal; whereas, a reading of 100 or 150 ohms indicates that at least one of the resistors is defective.

NOTE

Any defective resistor found during these checks should be replaced immediately. Do not use resistors marked with the letters RCL as replacements.

All 8542350 resistors with RCL markings mounted on spare, unused plug-in assemblies should be removed and replaced by 8542350 resistors not having RCL markings. In addition, all 8542350 resistors having RCL markings should be removed from stock and discarded.

5.7.7.3 Ordering Replacement 8542350 Resistors

If replacements are required for defective 8542350 wire-wound resistors, they must be ordered from Parts and Accessories only, using the applicable stock number. Do not attempt to purchase replacement resistors locally.

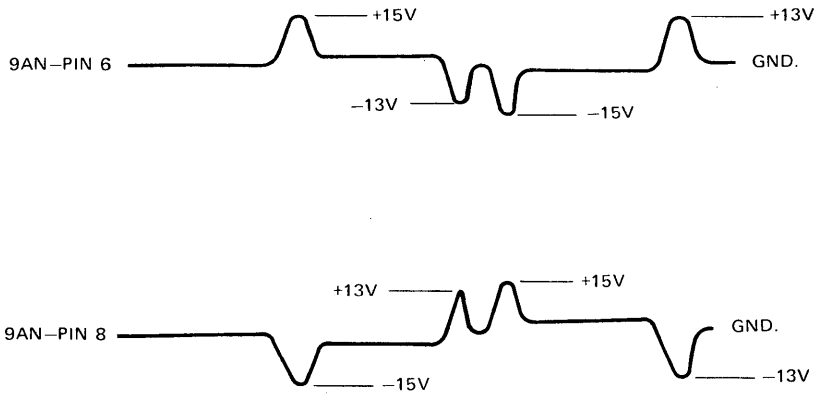


Figure 5-66C. Good Output of Current Switch (8M28 Plug-In Assembly)

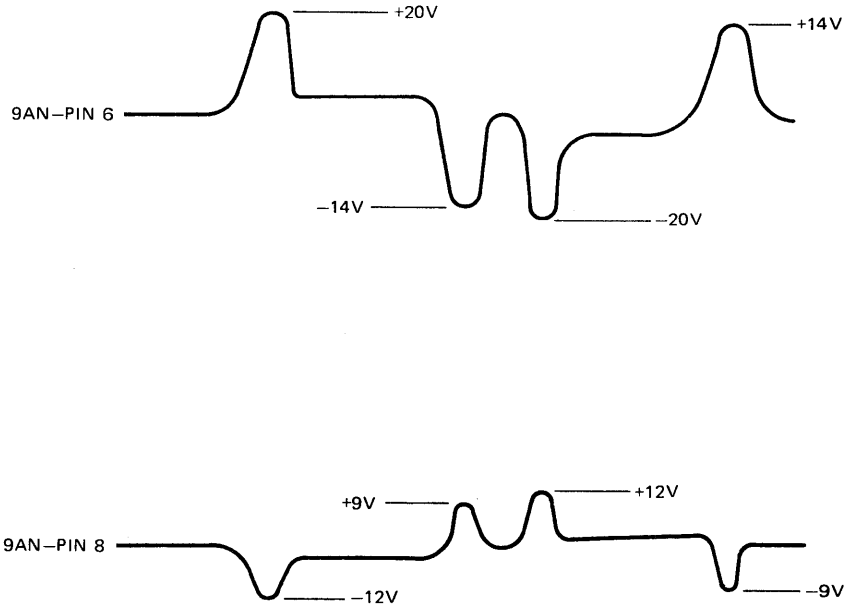


Figure 5-66D. Defective Output of Current Switch (8M28 Plug-In Assembly)

Because of the special bifilar construction of these wire-wound resistors, they must be replaced by exact duplicates or serious deterioration of equipment operation may result.

The following list can be used as an aid in ordering replacement resistors from Parts and Accessories. The list contains the stock numbers of all wire-wound resistors under the basic drawing no. 8542350 used in Spectra 70 equipment.

STOCK NO. FOR ALL DWG NO. 8542350 RESISTORS

PART NO.	STOCK NO.	RESISTANCE (Ohms)
-0006	263834	1
-0023	267054	1.5
-0073	263835	4.99
-0086	267055	6.81
-0115	305817	12.4
-0189	267056	73.2
-0192	267057	78.7
-0202	267058	90.9
-0206	264178	100
-0210	267059	110
-0211	263836	113
-0223	264104	150
-0224	264177	151
-0234	267060	196
-0235	264105	200
-0242	263837	237
-0265	263838	412
-0267	267507	432
-0268	267506	442
-0269	267505	453
-0271	301931	475
-0273	267504	499
-0274	264176	511
-0279	267061	576
-0283	265746	634
-0287	264209	698
-0295	301932	845
-0302	267503	909
-0306	267435	1000
-0313	265745	1180
-0323	267286	1500
-0333	304566	1910
-0335	267502	2000
-0338	304567	2150
-0361	304645	3740
-0369	267287	4530
-0370	267228	4640
-0372	267500	4870
-0374	267434	5110
-0377	267501	5490
-0378	267499	5620
-0379	367498	5760

R10

MAIN MEMORY

PART NO.	STOCK NO.	RESISTANCE (Ohms)
-0381	267497	6040
-0386	267289	6810
-0631	304646	18.2
-0694	304647	82.5
-0781	263348	604

5.7.7.4 Plug-In Assemblies Using 8542350 Resistors

Although most failures of these resistors have occurred on 8M28 plug-in assemblies, the resistors are used on many other plug-in assemblies. The following listing identifies the plug-in assemblies in which the 8542350 resistors are used.

Series 2:

2L221	2V176	2V261	2V351	2V441
2V173	2V212	2V262	2V352	2V661

Series 3:

3L171

Series 8:

8AD42	8M184	8M222	8M255	8M286
8A043	8M185	8M223	8M262	8M287
8F184	8M186	8M232	8M282	8M288
8F185	8M187	8M242	8M283	8M312
8M182	8M212	8M243	8M284	8M313
8M183	8M213	8M252	8M285	8M332

5.7.7.5 Cracked or Chipped Wire-Wound Resistor Castings

During factory assembly of Series 8 plug-in assemblies, 8542350 wire-wound resistors were mounted in a manner which occasionally resulted in cracked or broken casings. Although the problem has been corrected in manufacturing, problems still remain in some Series 8 boards in the field.

Electrical short circuits can occur between the exposed resistor windings and the circuit board printed wiring. This can result in intermittent problems, component damage, or equipment malfunctions.

Whenever an intermittent equipment problem is encountered involving Series 8 plug-in assemblies, the CSR should first examine these plug-in assemblies for cracked or chipped wire-wound resistor casings. All suspect resistors should be immediately replaced. Since wire-wound, one-percent tolerance resistors are used extensively in the processor memory plug-in assemblies (8MXX), these plug-in assemblies should be checked for damaged resistor casings when memory problems are encountered.

5.8 MEMORY MARGIN DETERMINATION AND EXPANSION PROCEDURE

5.8.1 EXERCISE MEMORY WITH LIBRARY TAPE BLOCK 705

The memory must operate without errors while being exercised by library tape block 705 over the voltage margins specified below. Each bank has its own set of relative strobe position (rsp) controls, therefore, each bank must be treated independently of any other bank. Refer to Figure 5-67.

5.8.2 SPECIFIED MARGIN VOLTAGE LIMITS

The voltage margins should be +6.5 through +14.0 volts (approximately -3.0 through +4.5 volts on the maintenance panel meter). Record the error address, bit and/or bits and the margin voltage at which the memory failed for both the high and the low end of the memory margin range.

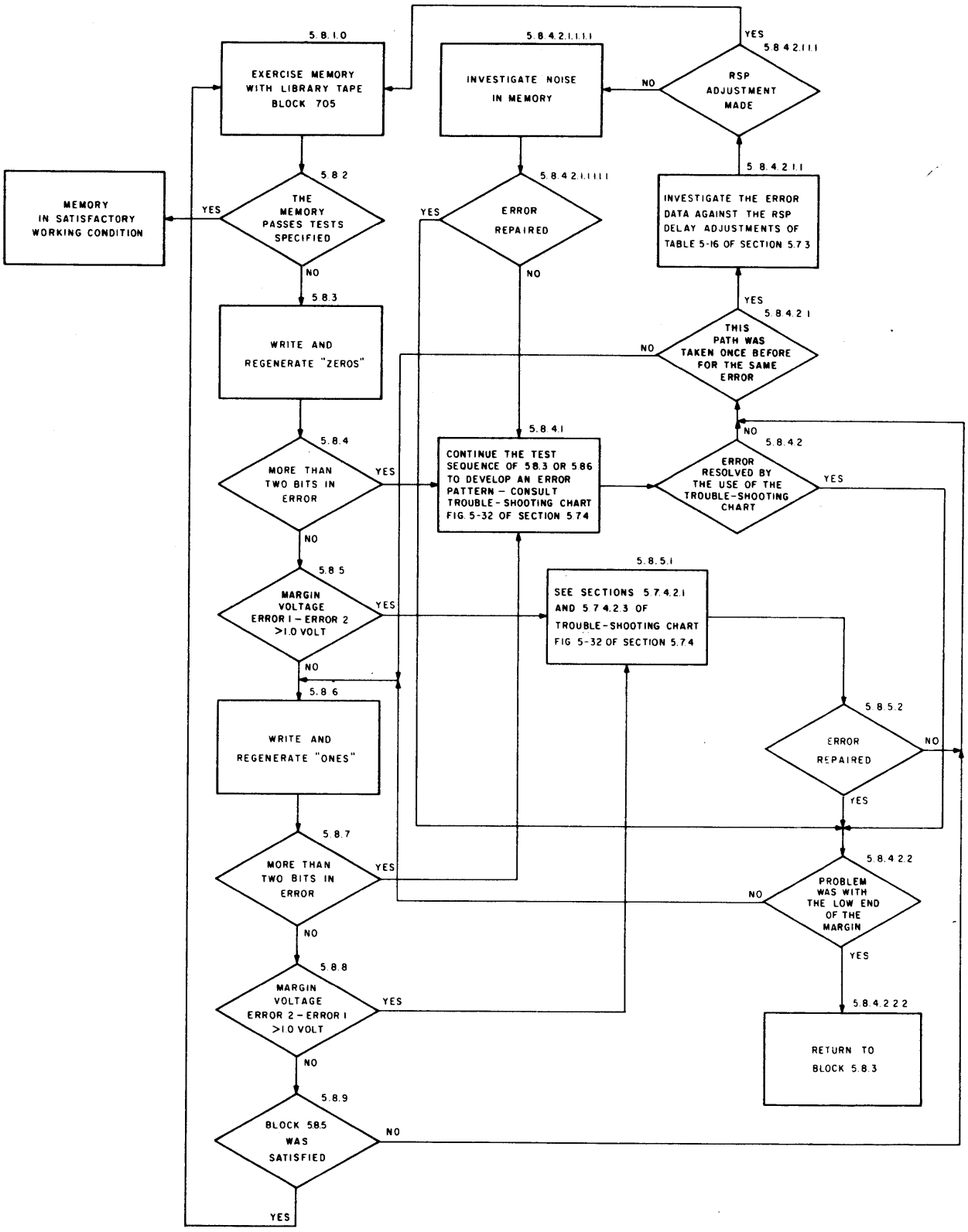


Figure 5-67. Marginal Range Expansion Flow Chart

Although these RCL-marked resistors are used on many Series 8 plug-in assemblies, the resistance problem is most prevalent with the type 8M28 plug-in assemblies used in the main memory of the processor.

The 8542350 resistors are bifilar wound (two windings) to produce negligible inductance. The two windings, which are identical in value, are also connected in parallel so that the overall resistance is one-half the value of one winding. These resistors have shown a tendency for one of the bifilar windings to open, and thus double the value of the resistor.

5.7.7.2 Locating Defective Wire-Wound Resistors

It is estimated that using an oscilloscope to check the 8M28 output voltages in one main memory stack can be accomplished by two people in approximately one-half hour.

There are two acceptable methods that can be used to locate defective resistors on 8M28 plug-in assemblies: (1) Observe the voltage outputs of the plug-in assemblies while the assemblies are being exercised in a memory system; and (2) simply measure the resistance across the wire-wound resistors using an ohmmeter. It is recommended that a combination of these two methods be used to check a main memory stack.

To check all 8M28 plug-in assemblies in the main memory stack, cycle main memory (all addresses) and observe all X and Y drive line outputs (both positive and negative) to the memory stack. Also check all current driver outputs at pin 32 of all 8M28 plug-in assemblies. If one of the wire-wound resistors, R3 through R20 (refer to Series 8 Data Sheets for 8M28 plug-in assembly circuits data), is defective, there is a noticeably unbalanced condition between the negative and positive drive line outputs to the memory stack, as when measured between 9AN-pin 6 (negative) and 9AN-pin 8 (positive). As viewed on an oscilloscope, one of the outputs has a greater peak-to-peak amplitude than the normal output and the other output has slightly less than the normal output. Normal drive line output voltage (8M28 output) is shown in Figure 5-66C.

When dynamically checking the 8M28 plug-in assemblies in the main memory, record the locations of all plug-in assemblies that have questionable outputs.

NOTE

If both terminating resistors across the secondary of an 8M28 plug-in assembly transformer are defective and double in value, the output waveforms do not have the same amplitudes shown in Figures 5-66C. and 5-66D. If both terminating resistors double, there is not an unbalanced condition in the amplitudes of the signal outputs of the drive line transformers. For this reason, an "added algebraically" oscilloscope preamp function should not be used to observe the positive and negative drive outputs. The presence of two

5.8.3 WRITE AND REGENERATE "ZEROS"

See Section 5.7.3.1, steps 1 and 2 for margin limits. Record the "pick-up" bit errors and addresses, but do not attempt to adjust any relative strobe position (rsp) delay line controls (see Table 5-16).

5.8.4 DECISION BLOCK FOR "ZEROS" ERRORS

Condition 1

If two different bits cause errors for the two trials made, then the possibility exists that the rsp is limiting the range on the lower end of the margin. If the two or more bits are at the same address, make one more trial run. A third error at the same address might indicate a problem in the memory. For the case that a different bit caused errors for each of the first two trials at the same or different addresses, go to block 5.8.5. For the case of three or more bits at the same address, go to block 5.8.4.1. For the case that the same bit caused errors in the first two trials, go to Condition 2.

Condition 2

If the same bit causes errors in both trials, then a third trial should be made. A third error caused by a different bit indicates that the rsp could be limiting the low end of the margin. If the same bit caused an error in all three trials, then write a "one" into that bit in every full word throughout all the addresses of the memory and "zeros" for all other bits. Regenerate all bits and again determine the (4th error) low margin voltage of the memory. Note the bit and address, then go to block 5.8.5.

5.8.4.1 Develop An Error Pattern

Continue sequence of block 5.8.3 or block 5.8.6 to develop an error pattern. See the troubleshooting section and repair the memory if a defective condition is detected, then proceed to block 4.2. If no defective condition is noted after a reasonable investigation of the memory has been conducted, then proceed to block 5.8.4.2 for a decision.

5.8.4.2 Decision Block For Investigation Results

If the problem was not resolved in block 5.8.4.1, then continue to block 5.8.4.2.1 for a decision. If a problem was detected and resolved in block 5.8.4.1, then proceed to block 5.8.4.2.2 for a decision as to where reentry into the test sequence should take place.

5.8.4.2.1 Decision Block For RSP Path

This block will always be entered two or more times. The first time the block is entered "zeros" are being investigated and nothing is known about the high end of the margin. The possibility exists that the rsp might be offset in such a way as to give a false impression that the memory is defective when the only discrepancy might be an rsp adjustment. Go to block 5.8.6 the first time block 5.8.4.2.1 is entered.

The second time and every other time the block is entered, the high and low margins of the memory are known; go to block 5.8.4.2.1.1.

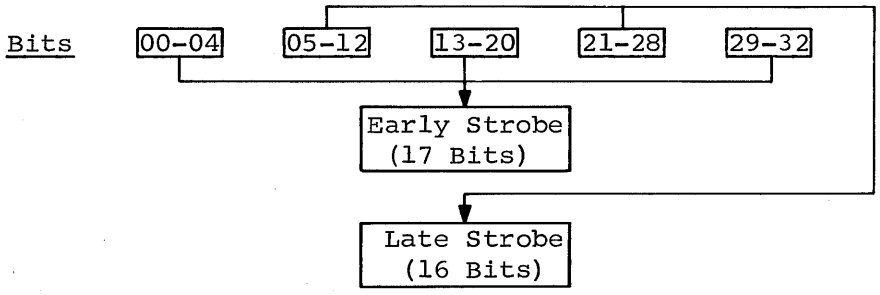
5.8.4.2.1.1 Investigate Error Data And Addresses

Obtain a minimum of four errors on the low end of the margin and four errors on the high end of the margin for each half bank of memory being investigated. Enough data must be obtained in order to determine the rsp adjustment that should be made.

5.8.4.2.1.1.1 Decision Block For RSP Adjustment

See Section 5.7.3 and Table 5-16 for a complete listing of the rsp delay line controls versus the data bits. A brief description of the seven rsp controls are listed below:

a. Early Strobe & Late Strobes



b. X READ

XR11 - bank 1 - bits 17-32
XR12 - bank 1 - bits 00-16
XR21 - bank 2 - bits 17-32
XR22 - bank 2 - bits 00-16

c. MAIN STROBE

The main strobe controls all bits of a full bank.

Each bank of memory has its own set of seven rsp controls and memory logic. Therefore, an rsp adjustment in bank 1 will not affect the range in bank 2 or any other bank and vice versa. A bank of memory which is operating at unsatisfactory limits might require two, three or more rsp adjustments before the bank finally meets the requirements of block 5.8.2. For example, the following sequence might be used to arrive at a satisfactory margin voltage operating condition:

SEQUENCE

RANGE PROBLEM: Pick-up bits 00 and 14 of first half bank @ 5.2V and 4.7V respectively.

ADJUSTMENT: Remove 5 ns from XR12

RANGE PROBLEM: Pick-up bits - 1st half 00, 04, 13, 15, 18, 29, 30

2nd half 01, 02, 13, 17, 19, 31

@ voltages between 4.6 and 4.1 volts.

ADJUSTMENT: Delay EARLY STROBE 5 ns

RANGE: Pick-up bits at voltages below 4.0 volts.

Only the bottom end of the range was used in the above example. Both the top and the bottom ends of the range must meet the specifications of block 5.8.2.

If an rsp adjustment is indicated from the error pattern, make the adjustment then go to block 5.8.2. If an rsp adjustment is not indicated from the error pattern, then go to block 5.8.4.2.1.1.1.1 for further investigations. The preliminary rsp adjustments are usually made with the "zeros" and "ones" tests; however since the noise test is more severe than either of the tests, the final rsp adjustment should be made using the noise test data only. It is possible to have the "ones" and "zeros" tests satisfied but not the noise test.

5.8.4.2.1.1.1.1 Investigate Noise in Memory

If no error pattern develops, noise in the memory might be a contributing factor to the errors recorded; investigate noise possibilities.

5.8.4.2.1.1.1.1.1 Decision For Noise Problem

If the cause of a noise problem was located and repaired in block 5.8.4.2.1.1.1.1, then go to block 5.8.4.2.2. If no noise problem was determined in block 5.8.4.2.1.1.1.1 or if the cause of the noise problem was located but the repair is not evident, go to block 5.8.4.1.

5.8.4.2.2 Decision For Re-Entry Into Margin Check

If the error or errors which were being pursued were with the low end of the margin range ("zeros") then go to block 5.8.3. If the error or errors were at the high end of the margin range, go to block 5.8.6.

5.8.5 DECISION FOR "ZERO" ERROR MARGIN DIFFERENCE

If ERROR 1 minus ERROR 2 is greater than 1.0 volt, go to block 5.8.5.1. But if the difference is less than 1.0 volt, then go to block 5.8.6. See Table 5-20 for determining ERROR 1 and ERROR 2 voltages.

5.8.5.1 Sensing And/Or Inhibit Defects

See Sections 5.7.4.2.1 and 5.7.4.2.3 of the Troubleshooting Flow Chart, Figure 5-32.

Table 5-20. Determination of Error Voltages

Conditions from which block was entered (See Block 4.0)	Error 1 Voltage	Error 2 Voltage		
	1st Error	2nd Error	3rd Error	4th Error
Condition 1	X	X		-
Condition 2	X	X	Different bit than 1st & 2nd Errors	-
Condition 2	X	Same bit as 1st Error	Same bit as 1st & 2nd Errors	X
X - indicates the margin voltage reading.				

5.8.5.2 Decision For Sense/Inhibit Repair

If a problem was determined and repaired in block 5.8.5.1, then go to block 5.8.4.2.2. However, if no problem was determined as a result of the investigations made in block 5.8.5.1 or if a problem was evident but a solution could not be determined, then go to block 5.8.4.2.1.

5.8.6 WRITE AND REGENERATE "ONES"

See Section 5.7.3.1, parts 3 and 4 for margin limits. Record the "drop" bit errors and addresses but do not attempt to adjust any relative strobe position delay line controls. (See Table 5-16.)

5.8.7 DECISION BLOCK FOR "ONES" ERRORS

Condition 1

If two different bits cause errors for the two trials made, then the possibility exists that the rsp is limiting the range on the upper end of the margin. If two or more bits are at the same address, make one more trial run. A third error at the same address might indicate a problem in the memory. For the case that a different bit caused errors for each of the first two trials at the same or different addresses, go to block 5.8.8. For the case of three or more bits at the same address, go to block 5.8.4.1. For the case that the same bit caused errors in the first two trials, go to Condition 2.

Condition 2

If the same bit causes errors in both trials, then a third trial should be made. A third error caused by a different bit indicates that the rsp could be limiting the high end of the margin. If the same bit caused an error in all three trials, then write a "zero" into that bit in every full word throughout all the addresses of the memory and "ones" for all other bits. Regenerate all bits and again determine the (4th error) high margin voltage of the memory. Note the bit and address then go to block 5.8.8.